

# Hardware implementation of digital memcomputing on small-size FPGAs

Dyk Chung Nguyen\*, Yuan-Hang Zhang<sup>†</sup>, Massimiliano Di Ventra<sup>†‡</sup> and Yuriy V. Pershin\*<sup>‡</sup>

\*Department of Physics and Astronomy

University of South Carolina, Columbia, South Carolina 29208, USA

<sup>†</sup>Department of Physics, University of California, San Diego, La Jolla, CA, 92093-0319, USA

<sup>‡</sup> Email: diventra@physics.ucsd.edu; pershin@physics.sc.edu

**Abstract**—Memcomputing is a novel computing paradigm beyond the von-Neumann one. Its digital version is designed for the efficient solution of combinatorial optimization problems, which emerge in various fields of science and technology. Previously, the performance of digital memcomputing machines (DMMs) was demonstrated using software simulations of their ordinary differential equations. Here, we present the first *hardware* realization of a DMM algorithm on a low-cost FPGA board. In this demonstration, we have implemented a Boolean satisfiability problem solver. To optimize the use of hardware resources, the algorithm was partially parallelized. The scalability of the present implementation is explored and our FPGA-based results are compared to those obtained using a python code running on a traditional (von-Neumann) computer, showing one to two orders of magnitude speed-up in time to solution. This initial small-scale implementation is projected to state-of-the-art FPGA boards anticipating further advantages of the hardware realization of DMMs over their software emulation.

**Index Terms**—Field programmable gate arrays, nonlinear dynamical systems, computing technology

## I. INTRODUCTION

During the past decade or so, the evolution of conventional computing devices has slowed down prompting the research community to shift its focus to alternative computing paradigms, such as neuromorphic, quantum, and stochastic computing, to name just a few. In many of such approaches, the computation is implemented beyond the von-Neumann paradigm, thus bypassing some of the most pressing issues (the von Neumann bottleneck, energy consumption, and further scaling) of our computing technology. It is then hoped that unconventional computing may boost or even revolutionize computing [1].

One such alternative approach is *memcomputing* [2]–[4], which relies on the ability of some physical systems to exploit memory (time non-locality) [5] to process information directly on the same physical platform where the computation result is ultimately stored. It is important to note here that time non-locality (e.g., the property that when the state of a physical system is perturbed, the perturbation affects the system’s state at a later time [4], [6]) is an essential feature to the computation. This is because time non-locality promotes spatial non-locality in the system [4]. This spatial non-locality, in the form of *dynamical long-range order*, can then be exploited to solve

computational problems efficiently. In this approach, then the massively-parallel dynamics of these physical systems at a dynamical long-range ordered state is essentially the process of computation. As the dynamics of such systems can be described by coupled ordinary differential equations (ODEs), finding the equilibrium point(s) of such a set of coupled ODEs is then equivalent to the physical computation [4], [7]. In particular, the digital memcomputing machines (DMMs) solving combinatorial optimization problems [8] can be designed so that their phase space has a single attractor corresponding to the problem solution (or multiple attractors if several solutions are possible). Additionally, the dynamics of these machines is deterministic, without periodic orbits or chaos [9], [10], and topologically robust against perturbations and noise [11], [12].

So far, all applications of DMMs have been based on software simulations of their ODEs, see, e.g., Refs. [4], [13], [14]. However, the hardware realization has well-recognized benefits including better scalability and faster execution time. Indeed, in contrast to prior work wherein DMMs have been simulated in a sequential fashion, in hardware, the DMM algorithms may be implemented in parallel. Therefore, we expect the hardware implementation of DMMs to provide additional benefits. In this work, we implement a 3-SAT solver using an entry-level FPGA board. Our goal is to understand the advantages and limitations of this implementation and to develop optimization strategies for the future deployment of memcomputing technologies on larger boards.

We emphasize that memcomputing is a *classical* (non-quantum) approach to computation in the sense that it does not rely on quantum features such as entanglement. Although “quantum supremacy” over traditional computers has been claimed recently using a superconducting quantum information processor [15], it still remains unclear how this demonstration can be transformed into a useful computation. At the same time, there are solid results on the advantages in scalability offered by memcomputing in the solution of combinatorial optimization problems (see, e.g., Ref. [4], [16]).

This paper is organized as follows. In Sec. II, we briefly present the 3-SAT problem and memcomputing ODEs used in this work. Some related work and approaches are summarily given in Sec. III. Next, we provide details of the FPGA implementation, which we compare with the performance of a code written in python to solve those ODEs (Sec. IV). Our

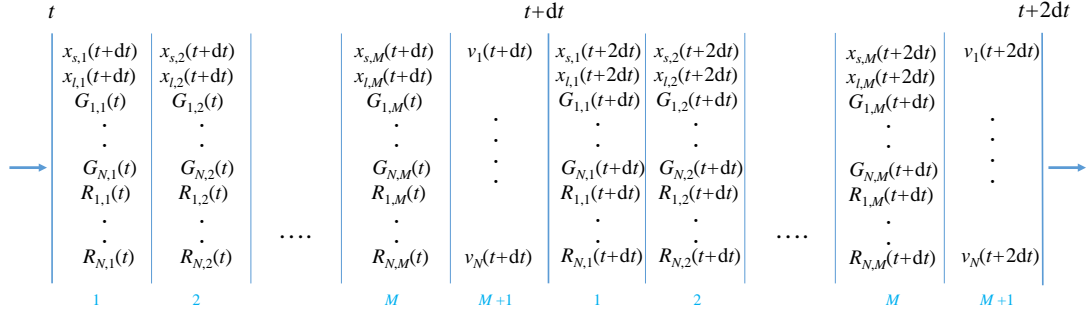


Fig. 1. Schematics of the parallelization of the memcomputing model. See the text for details.

results are presented in Sec. V and discussed in Sec. VI. Finally, we offer our conclusions in Sec. VII.

## II. MEMCOMPUTING EQUATIONS FOR 3-SAT

3-SAT is a particular case of satisfiability (SAT) problems, wherein each clause is the disjunction of 3 literals. A literal is a Boolean variable or its negation. The problem consists in finding the assignment of variables such that all clauses evaluate to true.

To tackle the 3-SAT, we have selected the DMM equations introduced in Ref. [14]. These equations are:

$$\dot{v}_n = \sum_m x_{l,m} x_{s,m} G_{n,m}(v_n, v_j, v_k) + (1 + \zeta x_{l,m}) \cdot (1 - x_{s,m}) R_{n,m}(v_n, v_m, v_k), \quad (1)$$

$$\dot{x}_{s,m} = \beta (x_{s,m} + \epsilon) (C_m(v_i, v_j, v_k) - \gamma), \quad (2)$$

$$\dot{x}_{l,m} = \alpha (C_m(v_i, v_j, v_k) - \delta), \quad (3)$$

$$G_{n,m} = \frac{1}{2} q_{n,m} \min[(1 - q_{j,m} v_j), (1 - q_{k,m} v_k)], \quad (4)$$

$$R_{n,m} = \begin{cases} \frac{1}{2} (q_{n,m} - v_n), & \text{if } C_m(v_n, v_j, v_k) = \frac{1}{2} (1 - q_{n,m} v_n), \\ 0, & \text{otherwise.} \end{cases} \quad (5)$$

Here,  $v_n$  are continuous variables ( $n = 1, \dots, N$ ),  $x_{s,m}$  and  $x_{l,m}$  are the memory variables ( $m = 1, \dots, M$ ), where  $N$  is the number of variables,  $M$  is the number of clauses,  $q_{j,m} = 1$  if the  $j$ -th variable enters  $m$ -th clause,  $q_{j,m} = -1$  if the negation of the  $j$ -th variable enters  $m$ -th clause. Moreover,  $\alpha, \beta, \gamma, \delta, \epsilon$  and  $\zeta$  are constants [14]. We emphasize that in the above equations, each variable of the 3-SAT is represented by a continuous quantity  $v_n$ , and two memory variables, the short (s) and long (l), are associated with each clause. Additionally,  $v_n$ -s are constrained to the interval  $[-1, 1]$ ,  $x_{s,m}$ -s are constrained to the interval  $[\epsilon, 1 - \epsilon]$ , and  $x_{l,m}$  to the interval  $[1, 10^4 M]$ . The sign of  $v_n$  defines its Boolean value: 0 if the sign is negative, and 1 otherwise.

Moreover, the clause function  $C_m(v_i, v_j, v_k)$  is defined as

$$C_m(v_i, v_j, v_k) = \frac{1}{2} \min[(1 - q_{i,m} v_i), (1 - q_{j,m} v_j), (1 - q_{k,m} v_k)]. \quad (6)$$

This function characterizes the state of the variable that most closely satisfies the clause  $m$ . For more information on the model, and how it has been obtained, see Refs. [4], [14].

## III. RELATED WORK

The integration of ODEs on FPGAs and hardware acceleration of SAT were explored in the past. For instance, Stamoulias *et al.* [17] reported a high-performance FPGA accelerator for the hardware integration of ODEs that achieves up to 14x speedup compared to single-core CPU solution [17]. Recently, Hollabough and Chakraborty [18] programmed an FPGA coprocessor to solve Lotka-Volterra equations. They reported 4.8x speedup.

Molnár *et al.* [19] used GPUs to accelerate a continuous-time analog SAT solver. They reported up to two orders of magnitude improvement compared to the CPU implementation. Sohaghpurwala *et al.* [20] published a survey of hardware-accelerated SAT solvers. For a comprehensive review of various hardware accelerators in general see Ref. [21]. In view of these previous results, one can then expect a similar speed-up of memcomputing on FPGAs.

## IV. METHODS

### A. Generation of SAT instances

To generate random “hard” 3-SAT instances, we use the algorithm proposed in [22]. First, a planted solution is set to  $y_i = 1$  for all  $i \in \{1, \dots, N\}$ , where  $y_i$  is the  $i$ -th Boolean variable. Then, we generate  $M$  clauses randomly and independently. Each clause has three literals randomly selected from the  $N$  variables and can have either 0, 1, or 2 negated literals, with probabilities  $p_0, 3p_1$ , and  $3p_2$ , respectively. The factor of 3 accounts for the fact that there are 3 possible ways to negate either 1 or 2 literals. Clauses with 3 negated literals are excluded since  $\bar{y}_i \vee \bar{y}_j \vee \bar{y}_k$  is not satisfied under the planted solution.

To ensure that the generated 3-SAT instances are hard, the probabilities should satisfy the following constraints:

$$0.077 < p_0 < 0.25, \quad p_1 = \frac{1 - 4p_0}{6}, \quad p_2 = \frac{1 + 2p_0}{6}. \quad (7)$$

The proof of these constraints can be found in [22]. In this work, we choose  $p_0 = 0.08$ .

Finally, we generate a random planted solution by randomly negating each variable  $y_i$  with probability 0.5 and negating all occurrences of  $y_i$  in all clauses.

### B. FPGA implementation

In this work, we used a commercially available Nexys A7-100T Artix-7 FPGA board from Digilent (FPGA part XC7A100T-1CSG324C). This FPGA contains 63,400 lookup tables (LUTs), 15,850 logic slices, and 126,800 CLB flip-flops. The clock speed is 100 MHz. To program the FPGA we used Verilog, which is a hardware design language (HDL). Its syntax is based on C programming language, making it fast and easy to program.

There are multiple ways to implement Eqs. (1)-(6) in FPGAs. Although the entire parallelization of integration steps in Eqs. (1)-(6) is possible<sup>1</sup>, such an approach is highly resource-demanding and, therefore, not useful in practice. In fact, the largest problem that we were able to implement fully in parallel with these small-size FPGAs contained 3 variables and 6 clauses.

Therefore, we have adopted a hybrid approach, see Fig. 1 for the general scheme. Within this approach, the time period between  $t$  and  $t+dt$  is divided into  $M+1$  intervals. The first  $M$  intervals are used to evaluate variables and functions related to the  $m$ -th clause and compute the sums in the right-hand side of Eq. (1) (not shown in Fig. 1). The last step in the sequence is used to update the voltages based on the sums evaluated in the previous steps. Essentially, this procedure corresponds to the forward Euler integration at a constant time step.

We note that this implementation relies on trading a clock cycle on computing  $C_m$ ,  $G_{n,m}$ ,  $R_{n,m}$  for each clause by using block RAM of Nexys A7-100T. The last  $(M+1)$ -th step is also needed to implement a delay between reading and writing variables into the block RAM of FPGA.

### C. Python code

To compare with the FPGA implementation, we also implemented the same equations using PyTorch [23]. The code is publicly available online at [24].

## V. RESULTS

The memcomputing approach was implemented in hardware for  $M/N = 4.3$  and 7,  $p_0 = 0.08$ , and  $N = 10, 30, 50, 70$ , and 90. Instances are typically more difficult on approaching  $M/N \sim 4.3$  [25]. For each value of  $N$ , we generated 10 instances of 3-SAT that were used (without pre-selection) to compile the FPGA code. The initial conditions utilized in FPGA and python calculations were the same. Specifically, we used randomly generated initial values of variables (in the interval from -1 to 1),  $x_{l,m}(0) = 1$ ,  $x_{s,m}(0) = C_m(0)$  that are the initial values of corresponding clause functions  $C_m$ .

The results presented herein were obtained using the following set of parameter values:  $\alpha = 5$ ,  $\beta = 20$ ,  $\gamma = 1/4$ ,  $\delta = 1/20$ ,  $\epsilon = 10^{-3}$ ,  $\zeta = 0.1$  for  $M/N = 7$ , and  $\zeta = 0.001$  for  $M/N = 4.3$  [14]. In all cases considered in this work,

<sup>1</sup>In this case, all  $M+1$  steps in Fig. 1 are merged into a single step.

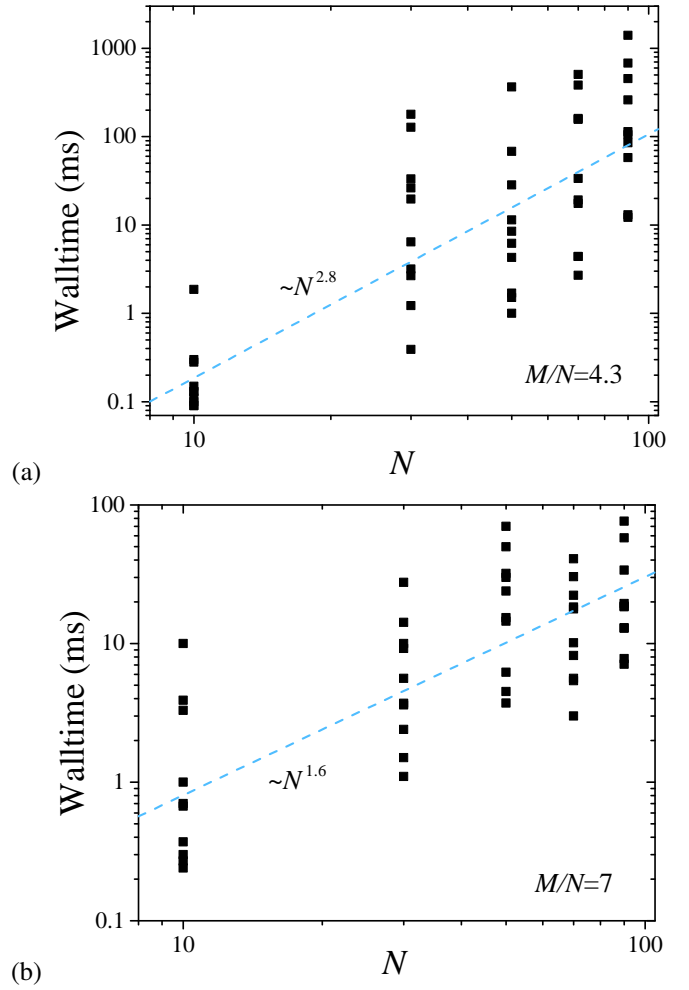


Fig. 2. Time to reach the solution,  $T_{\text{FPGA}}$ , as the function of the number of variables for (a)  $M/N = 4.3$  and (b)  $M/N = 7$  using FPGA board. Median times were used to obtain the fits (see the text).

the problem solutions were found. Fig. 2 shows the resulting calculation times for  $M/N = 4.3$  and 7 using FPGA. The data points were fitted using the allometric equation. To make the fit, we first found the median time for each problem size in Fig. 2(a) and (b). A log-log plot for the median times was fitted by a linear curve that was converted into  $\sim N^\alpha$  dependence for the original variables. We have obtained  $\alpha_{4.3}^{\text{FPGA}} \approx 2.8 \pm 0.5$  and  $\alpha_7^{\text{FPGA}} \approx 1.6 \pm 0.3$ . Although the number of data points in our study was limited, the fitting curves show a very reasonable description of the overall tendencies in Fig. 2.

The FPGA calculations were compared to calculations with the python code on an Intel Core i7-10750H CPU @ 2.60 GHz on the same problem instances. We have observed that the solutions obtained by different methods may differ, and even to reach the same solution the number of integration steps may not be the same. Although in both cases we utilized the same equations, parameters, and initial conditions, there are certain differences in the implementation, such as the precision of floating point numbers.

To better understand the relationship between the times to reach the solution in the two approaches, in Fig. 3 we plot the ratio of the python to FPGA times that demonstrates that in all cases the result was found significantly (1-2 orders of magnitude) faster by the FPGA. This plot shows that on average, the ratio  $T_{\text{python}}/T_{\text{FPGA}}$  slightly decreases with  $N$  and it would be interesting to see how it varies with larger  $N$ . We noticed that in the case of python, the duration of the integration step (in real-time) depends weakly on  $N$  and  $M/N$ . However, no attempts were made to understand this dependence better as well as the efficiency of the python implementation as these topics were not the focus of this study.

## VI. DISCUSSION

Our initial results presented here can be considered from several perspectives: the scaling of time to solution, utilization of hardware resources, and comparative performance.

First of all, we note that the scaling of time to solution (Fig. 3) has been estimated using a small set of data points that may not be sufficient to estimate the power-law exponents very accurately. Nonetheless, the power-law exponents we have found with the FPGA are not so different from the ones obtained using a software implementation [14].

To estimate the scaling of the hardware resources, in Fig. 4 we plot the number of lookup tables (LUTs) in our design versus the number of variables. This plot clearly shows the linear dependence with 582 LUTs per single variable, almost independent of  $M/N$ . To project this observation to larger boards, we estimated the number of LUTs for a VCU118 evaluation board employing VIVADO synthesis (see the inset in Fig. 4). For smaller values of  $N$ , we have obtained exactly the same linear dependence as in the case of the small-size board. Interestingly, this initial linear dependence,  $f_1(N)$ , changes to a slower linear dependence,  $f_2(N)$ , with

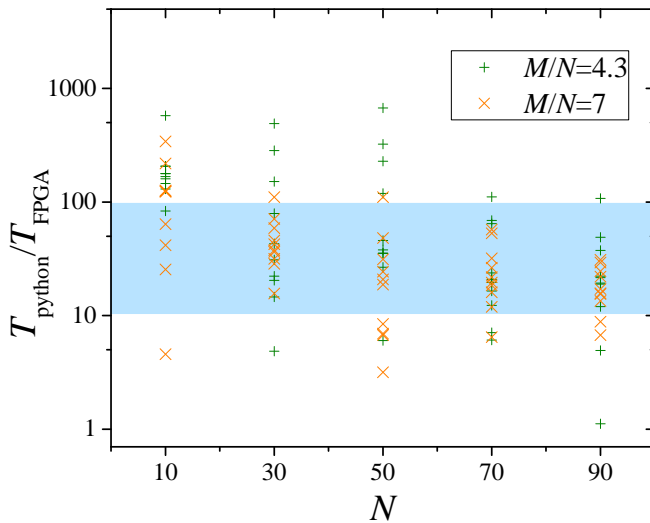


Fig. 3. The ratio of the python code calculation time to FPGA calculation time,  $T_{\text{python}}/T_{\text{FPGA}}$ . Each point was obtained for the same problem instance and initial conditions.

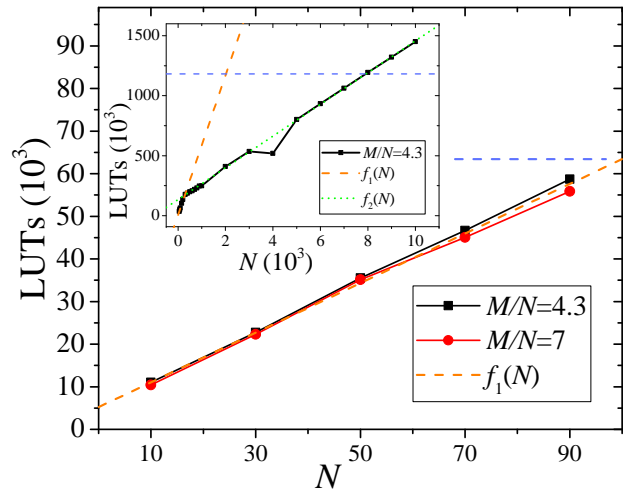


Fig. 4. Utilization of LUTs depending on the problem size. The dashed horizontal lines denote the maximum number of LUTs in our small-size FPGA board and VCU118 evaluation board. Inset: LUTs requirement for a larger board obtained using VIVADO synthesis. The fitting curves are  $f_1(N) = 5226 + 582 \cdot N$  and  $f_2(N) = 134147 + 132 \cdot N$ .

an unexpected dip at  $N = 4000$ . Based on this dependence, we expect to be able to fit problems with up to 7.5k variables into VCU118 based on VU9P device (1,182k LUTs). Note that some currently largest FPGAs, Xilinx VU19P and Intel Stratix 10 GX 10M, contain 4,086k and 10,000k LUTs, respectively, thus potentially increasing the size of the maximum problem that can be solved by an additional order of magnitude.

Finally, it is worth noting from Fig. 3 that we have obtained a hardware acceleration of the memcomputing solver by one to two orders of magnitude compared to the software. This is consistent with previous hardware accelerations of other types of ODEs [21] and it will be interesting to see if this speed-up holds, or even improves, with larger boards.

## VII. CONCLUSION

In this work, we have implemented the digital memcomputing algorithm for 3-SAT [14] on a low-cost FPGA for the first time and performed an initial evaluation of the scalability and resource requirements of such implementation. Compared to the python simulations, we have observed a significant (1-2 orders of magnitude) reduction in calculation time, although further research is necessary to better understand this trend in larger problem sizes. Our specific method can implement 3-SAT problems with up to tens (and possibly hundreds) of thousands of variables on state-of-the-art FPGA devices. To improve the statistics, a change to the problem-specific design is desirable<sup>2</sup>. There are several avenues for further optimization of the present implementation, including the processing of several clauses at a single sub-step that would be interesting to implement on a larger board.

<sup>2</sup>The present design is instance-specific.

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