HHS Public Access

Author manuscript

Symp VLSI Circuits. Author manuscript; available in PMC 2016 February 03.

Published in final edited form as:

Symp VLSI Circuits. 2015 June ; 2015: C238–C239. doi:10.1109/VLSIC.2015.7231271.

A 99nW 70.4kHz Resistive Frequency Locking On-Chip Oscillator with 27.4ppm/°C Temperature Stability

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Abstract

We present a low power on-chip oscillator for system-on-chip designs. The oscillator introduces a resistive frequency locking loop topology where the equivalent resistance of a switched-capacitor is matched to a temperature-compensated resistor. The approach eliminates the traditional comparator from the oscillation loop, which consumes significant power and limits temperature stability in conventional relaxation oscillators. The oscillator is fabricated in 0.18μm CMOS and exhibits 27.4ppm/°C and <7ppm long-term stability while consuming 99.4nW at 70.4 kHz.

Introduction

On-chip generation of a clock source has become more important as system-on-chip designs proliferate. More specifically, in sensor nodes with minimal board space (or even no board mounting [1]) for IoT applications, crystal oscillators are difficult to integrate. In these highly duty-cycled applications, power consumption in sleep mode can be dominated by the always-on oscillator. Key design goals for such an oscillator therefore include very low power while maintaining good frequency stability to ensure the synchronization of nodes for radio transmission and to maintain a constant system wakeup period.

A conventional relaxation oscillator (Fig. 1) charges a capacitor with a current source and resets the capacitor when V_{IN+} exceeds a threshold voltage ($V_{IN-} = I_{REF} \times R_{REF}$). In this structure, clock period is the sum of RC delay, comparator delay ($t_{d,comp}$), and buffer delays. While RC delay can be made insensitive to temperature fairly easily, $t_{d,comp}$ and buffer delay variation is known to impact temperature stability. To address this, a feed-forward period control was introduced in [2] to cancel $t_{d,comp}$ variation by measuring $t_{d,comp}$ and removing the effect with boost charging. However, the replica circuits to measure $t_{d,comp}$ nearly double the area and power. A comparator offset cancellation technique was proposed by switching comparator input polarity every half period [3]. However, $t_{d,comp}$ itself remains in the output period and, thus, a significant amount of power is consumed to keep the delay of comparator and buffers under 0.4% of oscillator period. Another design achieves 38.2ppm/°C with a circuit technique called local supply tracking threshold voltage, but it uses a dedicated implant process for a zero temperature coefficient (TC) poly resistor [4]. Most recently, a constant charge subtraction method was suggested to address $t_{d,comp}$ variation, but the output frequency is limited by a low power amplifier, producing an 11Hz clock [5].

Resistive Frequency Locking Oscillator

This paper proposes a Resistive Frequency Locking on-chip Oscillator (RFLO) that breaks away from the traditional topology by completely removing the comparator from the oscillation loop. As shown in Fig. 2, a stable output frequency is generated in a PLL-like manner by matching the equivalent resistance of a switched-capacitor (C_{SW}) to a temperature-compensated resistor (R_{REF}). First, a current I_{REF} is injected into R_{REF} to develop a reference voltage $V_{IN-} = I_{REF} \times R_{REF}$. An amplifier forces this voltage to match the voltage $V_{IN+} = I_{REF}/(C_{SW}F_{OUT})$ that develops when the same I_{REF} flows through C_{SW}, which is clocked by a VCO controlled by the amplifier output. As a result, the VCO frequency is regulated to $F_{OUT} = 1/(R_{REF}C_{SW})$, canceling sensitivity to I_{REF} (and hence supply fluctuation). Since R_{REF} is temperature compensated and C_{SW} is a MIM capacitor that is inherently temperature insensitive, a highly temperature-stable frequency is generated. The proposed topology has the following key advantages over a traditional relaxation oscillator topology: 1) It removes the traditional comparator from the oscillation loop; this comparator is power-hungry and introduces temperature dependency. 2) The amplifier that provides frequency locking must only track the impact of temperature changes on the VCO; these changes are slow and hence the amplifier can be low-bandwidth and ultra-low power. 3) Any slight deviation in frequency in any particular cycle *i* will result in a slight difference in the charge flowing into and out of node V_{IN+} (ΔQ_i). Unlike a traditional relaxation oscillator where the circuit is reset every cycle, this ΔQ_i is carried over from one cycle to the next and accumulates on the capacitor C_{IN+}, as $V_\Delta = \Sigma \Delta Q_i / C_{IN+}$. This enables the amplifier to compensate by adjusting frequency in subsequent cycles, providing excellent long-term frequency stability.

Fig. 2 shows the RFLO locking process when VCO frequency is lower than a target frequency and hence the charge pumped out of V_{IN+} by C_{SW} is less than the charge flowing in from I_{REF}, causing V_{IN+} to rise. When V_{IN+} matches V_{IN-}, the VCO frequency is locked. Ripples exist on the V_{IN+} node, but their amplitude is negligible due to a small C_{SW}/C_{IN+} ratio. The low bandwidth of the ultra-low power amplifier works like a loop filter in a PLL and helps to further reduce ripples and stabilize F_{OUT}. C_{OUT} also filters out high frequency noise.

Sources of Temperature Instability and Solutions

Ideally, F_{OUT} is only defined by $1/R_{REF}C_{SW}$. While MIM capacitors have almost zero temperature coefficient (TC), on-chip resistors show non-zero TC. In this work, a poly resistor without silicide ((−) TC) is serially combined with a diffusion resistor without silicide ((+) TC) to cancel their TCs. For the diffusion resistor, a segmented n-well technique is adopted to address well leakage current, increasing the maximum operating temperature by 30°C in simulation [5].

Amplifier offset voltage (V_{OS}) does not affect temperature stability by itself, however V_{OS} temperature dependency does. To cancel this, two identical auto-zeroed amplifiers can be used every other cycle with a Ping-Pong control scheme (Fig. 3). As described in Fig. 4, each amplifier is a 1-stage folded cascode structure operating in subthreshold region

providing 85dB gain and wide output range of 0.4V–0.8V while consuming only 3.6nW at room temperature (simulation). Likewise, mismatch between I_{REF1} and I_{REF2} over temperature impacts temperature stability. As illustrated in Fig. 3, I_{REF1} and I_{REF2} alternate their connections to the amplifiers, thus effective current at each input is the average of I_{REF1} and I_{REF2}, canceling each other. Switches ($SW_{1,2}$) also have minor impact on temperature stability. If the V_{IN+} (=V_{IN-}) level changes, switch parasitic capacitance (C_{PAR}) varies and alters total capacitance at V_{IN+}. To render this effect negligible, C_{SW} is sized so that C_{PAR} < 0.02% of C_{SW}. $SW_{1,2}$ leakages increase from sub-pA at −20°C to ~2pA at 80°C (simulation). To nullify this effect, identical dummy switches are added at the V_{IN-} node, as shown in the gray area of Fig. 3.

Fig. 5 shows the rail-to-rail VCO. The delay of the first four stages is exponential with V_{OUT}, relaxing amplifier output voltage range. The next four stages are buffers to restore slew rate, the first of which is a stacked inverter with high V_T devices. This stage reduces VCO power (10.3nW, simulation) by 67× by minimizing short circuit current. RFLO does not require the VCO to have a linear voltage-frequency relation, which relaxes the VCO specification.

Measurement Results

The proposed design is fabricated in 0.18μm CMOS (die photo in Fig. 8) with total area of 0.26mm^2. F_{OUT} has temperature stability of 27.4ppm/°C in −40°C to 80°C range, which is the lowest among reported ultra-low power on-chip oscillators (Table 1). It also exhibits supply voltage sensitivity of 0.5%/V (Fig. 6), and long-term stability of < 7ppm (Fig. 7). The design consumes 99.4nW at room temperature, yielding the lowest energy per cycle of 1.41pJ/cycle. All reference voltages and currents are generated on chip with techniques proposed in [6]. Auto-zeroing is not used for measurement results in Figs. 6 and 7, since excellent TC was obtained at reduced power.

References

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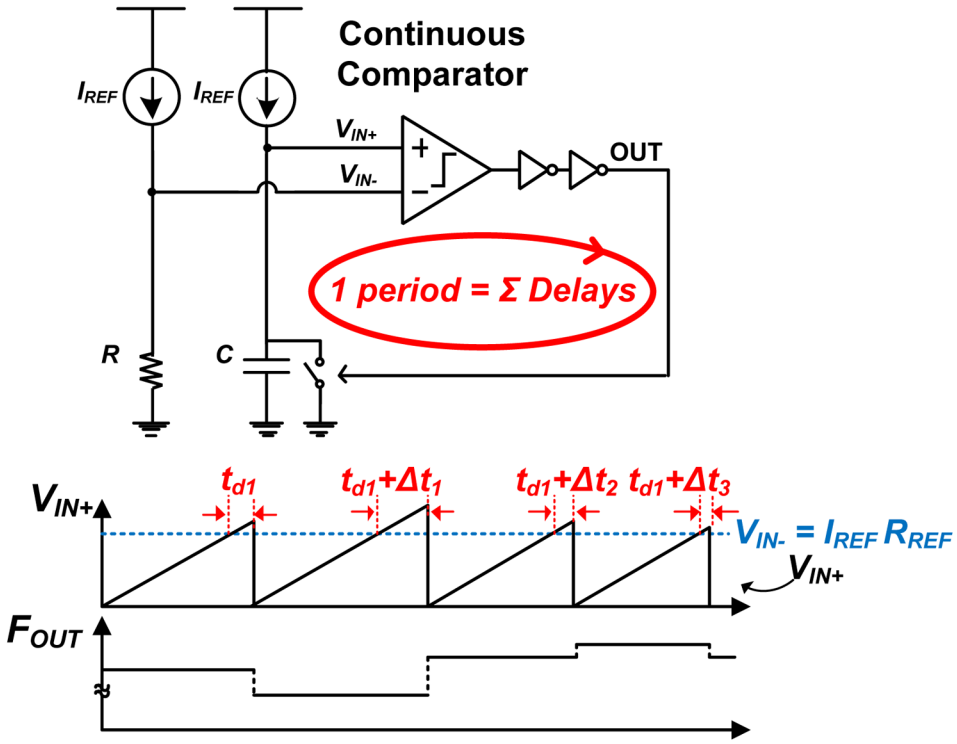

Fig. 1.

Conventional relaxation oscillator circuit and its unstable frequency caused by comparator delay variation.

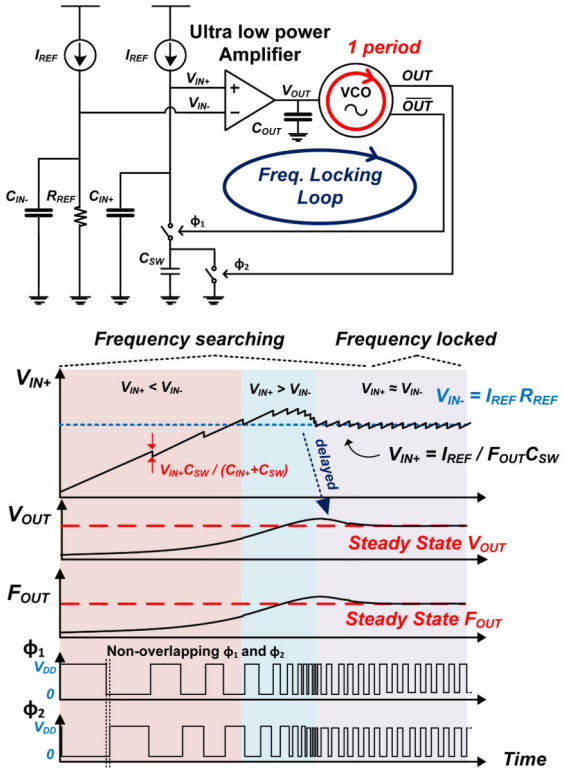

Fig. 2.

Circuit diagram of proposed Resistive Frequency Locking on-chip Oscillator and its waveforms.

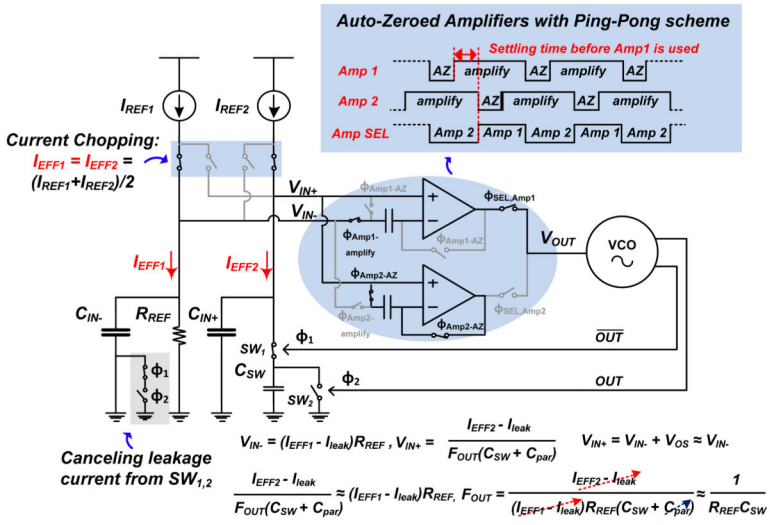

Fig. 3.

Detailed circuit diagram of RFLO with Pin g-pong autozeroing amplifier, current chopping technique, and dummy switches to cancel leakage of $SW_{1,2}$.

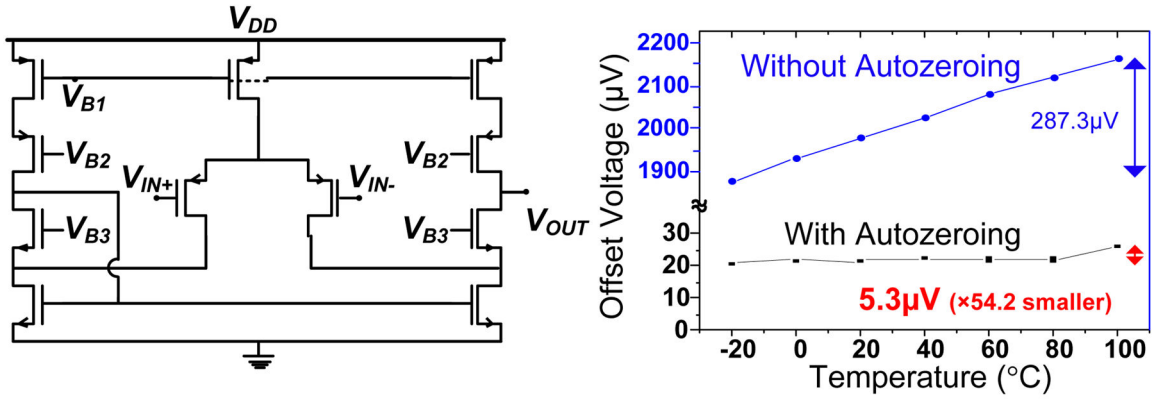

Fig. 4.

Schematic of subthreshold mode ultra low power amplifier, and simulation results of its offset voltage with and without autozeroing.

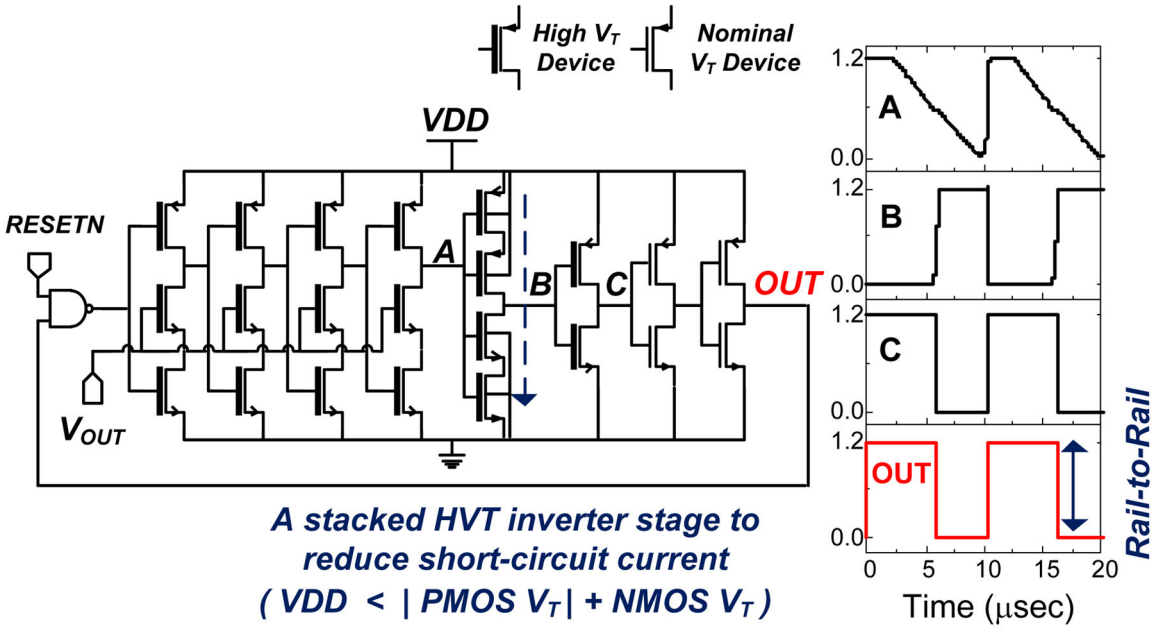

Fig. 5.
Schematic of rail-to-rail voltage controlled oscillator and its simulated waveforms.

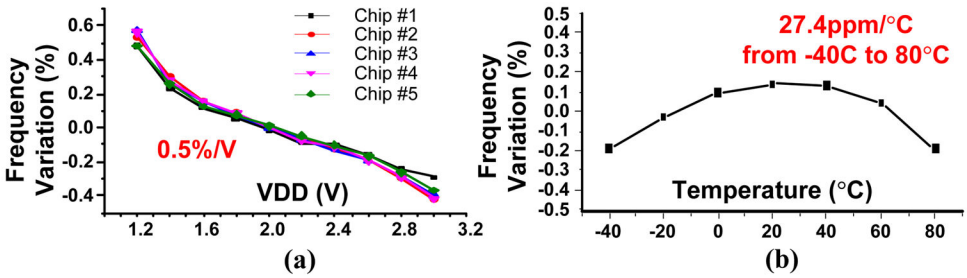

Fig. 6.

Measured frequency variation with respect to (a) supply voltage (b) temperature.

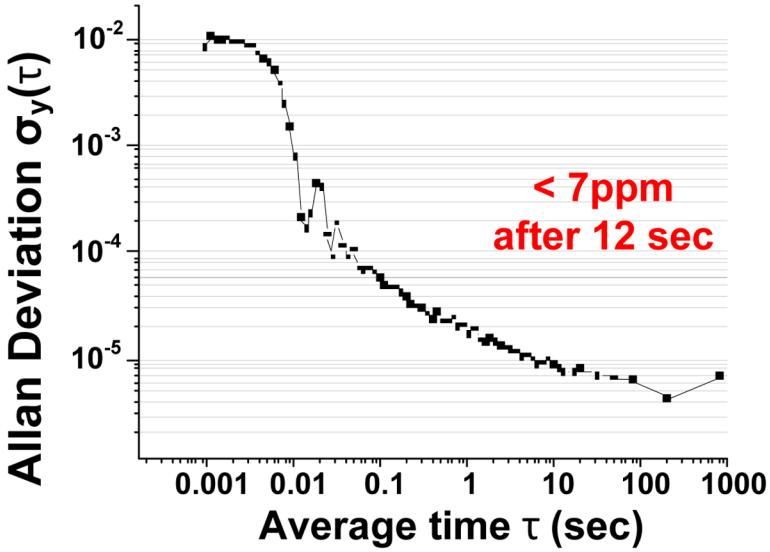

Fig. 7.
Measured Allan Deviation.

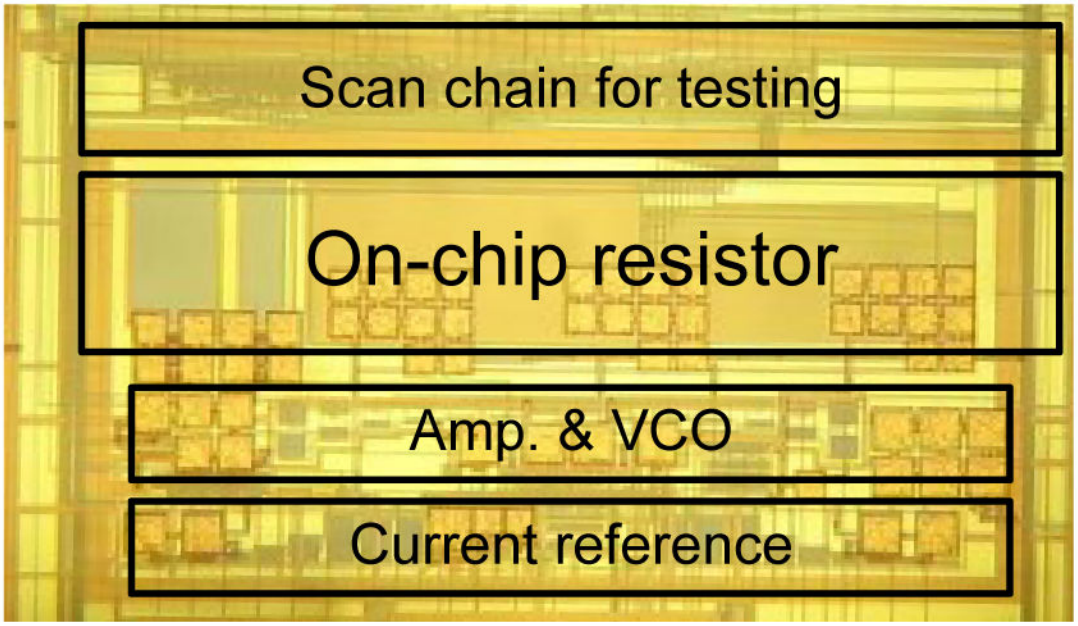

Fig. 8.
Die photo.

Table 1

Performance summary & comparison.

	This work	ISSCC 2013 [3]	ISS CC 2014 [4]	VLSI 2012 [2]	VLSI 2012	CICC 2014 [5]	ISSCC 2011
Process (nm)	**180**	65	65	90	60	180	130
Frequency (Hz)	**70,400**	18,500	33, 000	100,000	32,768	11	0.37
TC (ppm/°C)	**27.4**	38.5	38.2	104.6	16.7	45	375(31[1])
Temp. Range (°C)	**−40–80**	−40–90	−20–90	−40–90	−20–100	−10–90	−20–60
Line sensitivity (%/V)	**0.5**	1	0. 09	9.4	0.06	1	490
Power (nW)	**99.4**	120	190	280	4,480	5.8	0.66[2]
Energy/Cycle (pJ/Cycle)	**1.41**	6.49	5.76	2.80	136.72	527.27	1,738.8
Long term stability (ppm)	**< 7**	< 20	< 4	N/A	N/A	< 15	N/A
Area (mm^2)	**0.26**	0.032	0.015	0.12	0.048	0.24	0.015

[1] With 10 point calibration using temperature sensor.

[2] Power consumption of temperature sensor is not included.

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