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A Second-Order All-Digital TDC with Low-Jitter Frequency Shift Oscillators and Dynamic Flipflops*

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SUMMARY We present a small-area second-order all-digital time-to-digital converter (TDC) with two frequency shift oscillators (FSOs) comprising inverter chains and dynamic flipflops featuring low jitter. The proposed FSOs can maintain their phase states through continuous oscillation, unlike conventional gated ring oscillators (GROs) that are affected by transistor leakage. Our proposed FSOTDC is more robust and is eligible for all-digital TDC architectures in recent leaky processes. Low-jitter dynamic flipflops are adopted as a quantization noise propagator (QNP). A frequency mismatch occurring between the two FSOs can be canceled out using a least mean squares (LMS) filter so that second-order noise shaping is possible. In a standard 65-nm CMOS process, an SNDR of 61 dB is achievable at an input bandwidth of 500 kHz and a sampling rate of 16 MHz, where the respective area and power are 700 μm^2 and 281 μW.

key words: *ADC, TDC, oscillator, digital circuit, adaptive LMS filtering*

1. Introduction

To produce competitive information and communication equipment, designing high-performance and low-cost chips at low power is needed. Scaling in process technology has enabled miniaturization of transistors. Consequently, the number of transistors can be increased. Functionality in a digital system has developed rapidly at low cost. The low-power feature is also achieved by reducing the supply voltage.

For analog circuits, however, it is difficult to benefit from scaling. Operating at low supply voltage yields a small dynamic range. Linearity becomes degraded, and a gain in an opamp is lowered. To compensate for these disadvantages, transistor sizing and the area of passive components are ever-increasing. Consequently, a mixed-signal chip comprising digital and analog circuitry can achieve neither low cost nor low power in the recent advanced process. An analog-to-digital converter (ADC) is a critical component in mixed-signal circuits, in which opamps and capacitors — particularly in a $\Delta\Sigma$ ADC — prevent merits derived from scaling.

Several ADCs operating in a time domain have been proposed recently. In the advanced CMOS process, the speed of the transistor will be increasing. It enables TDC to get the more accurate time resolution. A GRO that uses a ring oscillator comprising gated inverters has been studied for use as a TDC [1]. It is noteworthy that this GROTDC has a first-order noise-shaping nature, but only its function as a first-order modulator is described in the literature. Higher-order noise shaping GROTDCs have been reported as presenting the possibility of realizing higher performance [2]. Mandai used GROs and a time difference amplifier as a time residue transmitter [3]. Instead of the GRO, Cao adopted a relaxation oscillator [4]. Gating in the GRO or the relaxation oscillator, however, causes switching noise and transistor leakage at internal nodes storing phase states. The gating transistor must be small to avoid the switching noise, which limits the oscillating frequency and performance. Moreover, the stored phase states are degraded or even lost by the transistor leakage. They are therefore unsuitable for recent leaky processes [5].

In this paper, we propose an opampless second-order MASH TDC topology in the next section. Then, simulation results and measured results with a test chip are described in Sects. 3 and 4, respectively. The final section summarizes this paper.

2. Proposed Frequency Shift Oscillator TDC (FSOTDC)

Our proposed FSOTDC architecture is depicted in Fig. 1. No area-consuming capacitor or analog component is used. For that reason, it has process scalability. The FSO on the

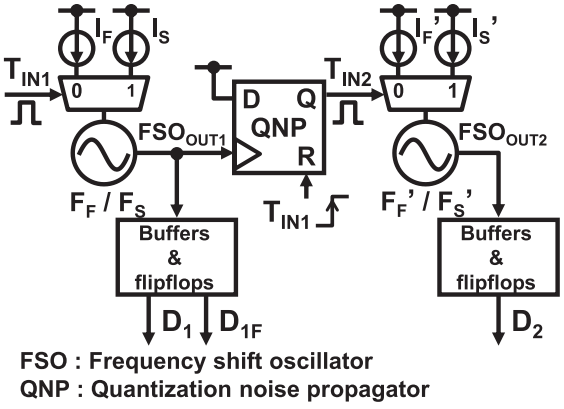

Fig. 1 Proposed second-order frequency-shift-oscillator-based time-to-digital converter (FSOTDC) architecture.

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first stage outputs a frequency of F_S ($\approx$ 217 MHz: low frequency) or F_F ($\approx$ 557 MHz: high frequency). The FSO layouts of the first and second stages are identical, but their output frequencies differ ($F_S \neq F_S$', $F_F \neq F_F$') due to transistor variation. In an extreme case, if all transistors in the first-stage oscillator have a $+3\sigma$ threshold voltage and those in the second-stage oscillator have a -3σ threshold voltage as local variation (random variation), their output frequencies will change by $-15.0\%/+15.4\%$, respectively, even at the typical process corner. This means that the frequency mismatch possibly results in 35.7%. In our proposed architecture, this frequency mismatch can be, however, compensated by a first-order LMS filter.

The FSO presents advantages over a GRO by alleviating problems related to switching noise and transistor leakage [6]. In GRO's gating, the stored phase states are degraded or even lost. The switching noise or transistor leakage will prevent maintenance of its internal state. Unlike the GRO, the FSO does not stop its oscillation or does not maintain its output phase state; use of the FSO eliminates these problems because it continues oscillating. Furthermore, the power supply noise in the FSO is less than that in the GRO because the FSO does not cease oscillating; the fluctuation in switching current is smaller (current fluctuation: FSO = $I_F - I_S$, GRO = I_F).

Figure 2 depicts a timing diagram of the proposed FSOTDC. Therein, T is a sampling period, T_{IN1} (T_{IN2}) signifies an input pulse width into the first-stage (second-stage) FSO, FSO_{OUT1} (FSO_{OUT2}) stands for its output, D_1 (D_2) denotes the number of FSO_{OUT1} (FSO_{OUT2}) oscillations in a sampling period, D_{1F} denotes the number of oscillations while T_{IN1} is off, and QN_1 (QN_2) represents a quantization noise of FSO_{OUT1} (FSO_{OUT2}). Herein, we define ξ as a time residue in T_{IN1}. T_{IN1} and $T - T_{IN1}$ are given respectively as (1) and (2).

$$T_{IN1} = \frac{1}{F_S} - \frac{QN_1[n-1] \cdot F_F}{F_S} + \frac{(D_1 - D_{1F})}{F_S} + \xi \quad (1)$$

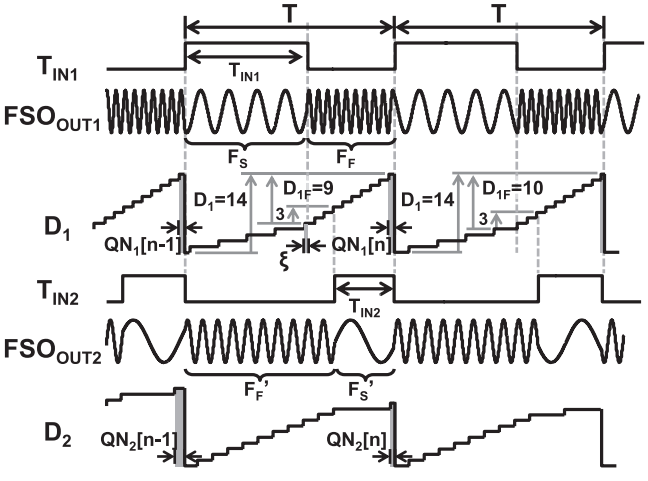

Fig. 2 FSOTDC timing diagram.

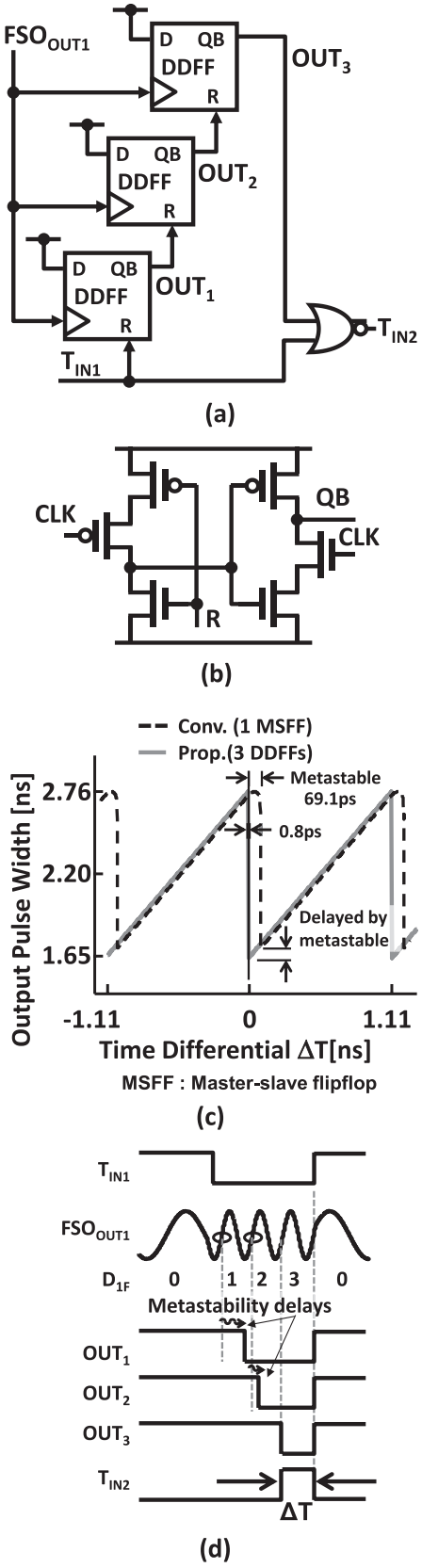

Fig. 3 (a) Quantization noise propagator (QNP), (b) dynamic D-flipflop, (c) transfer characteristics, and (d) QNP timing diagrams.

$$T - T_{IN1} = \frac{1}{F_F} - \frac{\xi \cdot F_S}{F_F} + \frac{D_{1F}}{F_F} + QN_1[n] \quad (2)$$

Next, D_1 and D_{1F}, which are digital values corresponding to T_{IN1} and $T - T_{\mathrm{IN1}}$, are given respectively as (3) and (4) (where $F_{\mathrm{F}} \cdot T$ is a constant offset).

$$D_1 = (F_S - F_F) \cdot T_{IN1} + F_F\,(QN_1[n-1] - QN_1[n]) + F_F \cdot T \quad (3)$$

$$D_{1F} = -F_F \cdot T_{IN1} + F_F \cdot QN_1[n] + F_F \cdot T \quad (4)$$

In the equations, respective $QN_1[n-1]$ and $QN_1[n]$ are quantization noises in the previous and present sampling periods. The QNP detects the third rising-edge of FSO_{OUT1} (see Fig. 3; because it has three flipflops) when T_{IN1} is off, and then it outputs T_{IN2}. In this case, T_{IN2} is represented as (5).

$$T_{IN2} = QN_1[n] + \frac{D_{1F} - 2}{F_F} \quad (5)$$

By putting (4) in (5), we can obtain (6), from which D2 is given as (7) (C_1 and C_2 are constants).

$$T_{IN2} = -T_{IN1} + 2 \cdot QN_1[n] + C_1 \quad (6)$$

$$D_2 = (F'_F - F'_S) \cdot (-T_{IN1} + 2 \cdot QN_1[n]) + F'_S \cdot (QN_2[n-1] - QN_2[n]) + C_2 \quad (7)$$

As depicted in Fig. 3(a), the proposed QNP has three dynamic D-flipflops (DDFFs) to avoid metastability. In the FSOTDC architecture, ΔT in Fig. 3(c) might be very small because of continuous oscillation, which might cause metastability in the QNP. The DDFF depicted in Fig. 3(b) is simple and is five times faster than the conventional master-slave flipflop. By connecting the three DDFFs, the metastable period, which worsens stability and linearity, can be minimized to 0.8 ps (Fig. 3(c)). Figure 3(d) illustrates the timing diagrams of the QNP; even if the falling edges of "OUT_1" and "OUT_2" at the first and second flipflops get slower by the successive metastabilities, the proposed QNP properly mask the unnecessary delays.

3. Simulated Results with Considering Effects of Jitters

Because the simulation of TDC needs high accurate time step, the lower the clock frequency is, the longer the simulation time and the bigger data is needed. Then it is difficult to simulate under the condition of low sampling frequency. In this section, we will discuss the numerical calculation by using MATLAB with considering SPICE simulated results.

Table 1 shows SPICE simulated results of the oscillator, which is used in our proposed TDC. We added the noise sources on power supply lines and set the amplitude of noise to the 10 mVp-p.

3.1 Consideration to Timing Jitters

We considered the effect of timing jitter. Actually, when the oscillator is running, there are some jitters as shown in Fig. 4. If the jitter exists, the period of FSO_{out} may shift.

Table 1 Simulated data of the oscillator.

Item	F_{S}	F_{F}
Frequency [GHz]	0.217	0.557
Period [ns]	4.59	1.79
Jitter (stddev) [ps]	3.70	1.95
Jitter / Period [%]	0.0805	0.1085

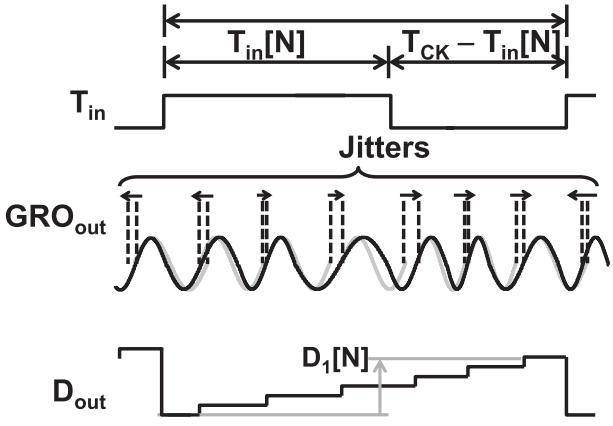

Fig. 4 Timing diagram with considering the effects of the jitters.

We define the time difference occurred from the jitters as $Jitter1_i$ ($i = 1, 2, 3 \ldots Nj_1$) in the slow frequency mode. Nj_1 is the total counts of the rising edge during one sample period in the slow frequency mode. And also, $Jitter2_i$ ($i = 1, 2, 3 \ldots Nj_2$) are the jitters in the high frequency mode. Nj_2 is the total counts of the rising edge during one sample period in the high frequency mode. Then, T_{in} is expressed as follows:

$$T_{IN1} = \frac{1}{F_S} - \frac{QN_1[n-1] \cdot F_F}{F_S} + \frac{D_1 - D_{1F}}{F_S} + \sum Jitter1_i + \xi \quad (8)$$

$$T - T_{IN1} = \frac{1}{F_F} - \frac{\xi \cdot F_S}{F_F} + \frac{D_{1F}}{F_F} + \sum Jitter2_i + QN_1[n] \quad (9)$$

D_1 is given as

$$D_1 = (F_S - F_F) \cdot T_{IN1} + F_F\,(QN_1[n-1] - QN_1[n]) + F_S \cdot \sum Jitter1_i + F_F \cdot \sum Jitter2_i + F_F \cdot T \quad (10)$$

$Jitter1_i$ and $Jitter2_i$ are series of random numbers defined as Gaussian distribution. The average is set to 0. And 3σ is set to 0.08–0.11% of the oscillation period. This parameter is based on the SPICE simulation in which 10 mVp-p of white noise is added on the power lines.

3.2 Modeling in MATLAB

MATLAB function 1 is the model of the ring oscillator. This function outputs the total counts of the rising edge of the

MATLAB function 1 Numerical calculation of the oscillation

```
function [Do,Po] = OSC(Tin,Pi,Fo,Aj)
Do=0;
Po=Tin*Fo;
Nj=fix(Po+1);
rng('shuffle');
pjitter=Aj.*randn(1,Nj);
Po=Po+Pi;
if Po < 1
   Do=0;
else
   for j=1:1:Nj
      if Po < 1
         break
      end
      Po=Po-(1+pjitter(j));
      Do=Do+1;
   end
end
```

MATLAB function 2 Numerical calculation of the TDC

```
function [D1,D2,D2d,TDout] = TDC(Tin,T,Nsample)
F1S=217e6;% oscillation frequency during Tin = 'on'
F1F=557e6;% oscillation frequency during Tin = 'off'
F2S=217e6;% oscillation frequency during Tin = 'on'
F2F=557e6;% oscillation frequency during Tin = 'off'
ph1i=0;% initial phase condition of FSO1
ph2i=0;% initial phase condition of FSO2
Aj1=0.08/100;% jitter amplitude of the F_S mode
Aj2=0.11/100;% jitter amplitude of the F_F mode

B1=F1F;
A2=F2S−F2F;
w0=−A2/B1;

%% Time to digital conversion%%
for i=1:1:Nsample
   [D1S(i),Po] = OSC(Tin(i),ph1(i),F1S,Aj1);
   [D1F(i),ph1(i+1)] = OSC(T−Tin(i),Po,F1F,Aj2);

   rng('shuffle');
   Tin2(i)=Tin(i)+(3−Po)/F1F+(0.1e−12).*randn(1);

   [D2S(i),Po2] = OSC (Tin2(i),ph2(i),F2S,Aj1);
   [D2F(i),ph2(i+1)] = OSC (T−Tin2(i),Po2,F2F,Aj2);
End

%% Noise cancellation%%
D1=D1S+D1F;
D2=D2S+D2F;
D2d=D2−w0*D1F;

for i=1:1:Nsample−1
   TDout(i)=−w0*D1(i+1)−(D2d(i+1)−D2d(i));
end
```

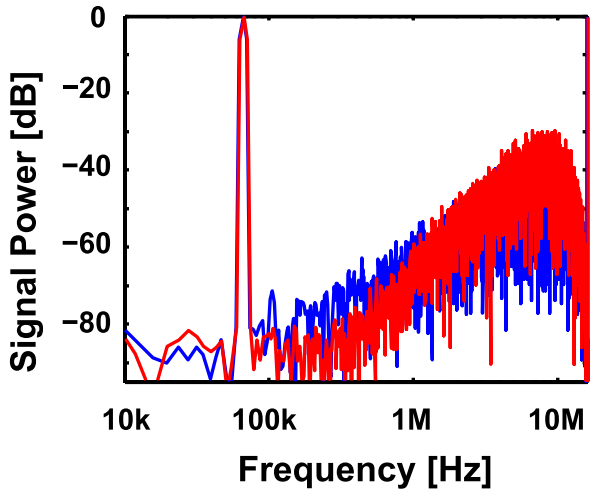

Fig. 5 Output results of the numerical calculation. CK=16 MHz. Blue and red lines are outputs of the first-order FSOTDC and the second-order FSOTDC respectively.

Table 2 Specifications of the calculated results.

Item	Data
Technology (nm)	65
Bandwidth (kHz)	500
Sampling rate (MS/s)	16
First-order SNDR (dB)	54
Second-order SNDR (dB)	63

FSO. "Tin" is the width of time-domain input. "Po" is the final phase state of the FSO during the period of "Tin". "Pi" is initial phase state. "Fo" is the frequency of the FSO. "Aj" is the maximum amplitude of the jitters.

MATLAB function 2 is the model of the second-order FSOTDC. And this function outputs the second-order noise shaped output "TDCout" and the first-order noise shaped output "D1". "Tin" is the time series of time-domain input signals. "T" is the frequency of the clock. "Nsample" is the total number of samples. "F1S" means F_S, "F1F" means F_F, "F2S" means F_S', and "F2F" means F_F' respectively.

3.3 Simulated Results

Figure 5 shows the results of numerical calculations based on the MATLAB models described in the next section (subsection B). The jitters affect the performance of TDC and raise up the noise floors in the low frequency region. Table 2 shows specifications of the calculated results. The input signal frequency is 66.4 kHz, the input signal width is 31.25 ns (signal amplitude is 15.62 ns), and the sampling rate is 16 MHz. The output SNDR of the first-order noise shaping is 54 dB in this case. The output SNDR of the second-order noise shaping is 63 dB, which achieves about a 9-dB improvement in the SNDR.

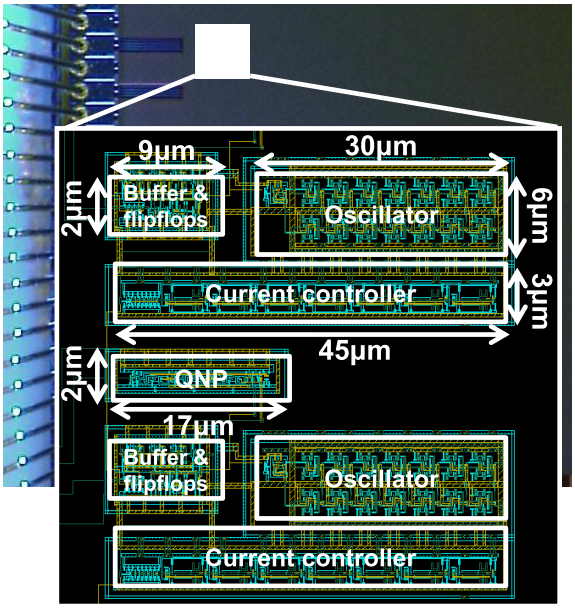

Fig. 6 Chip micrograph.

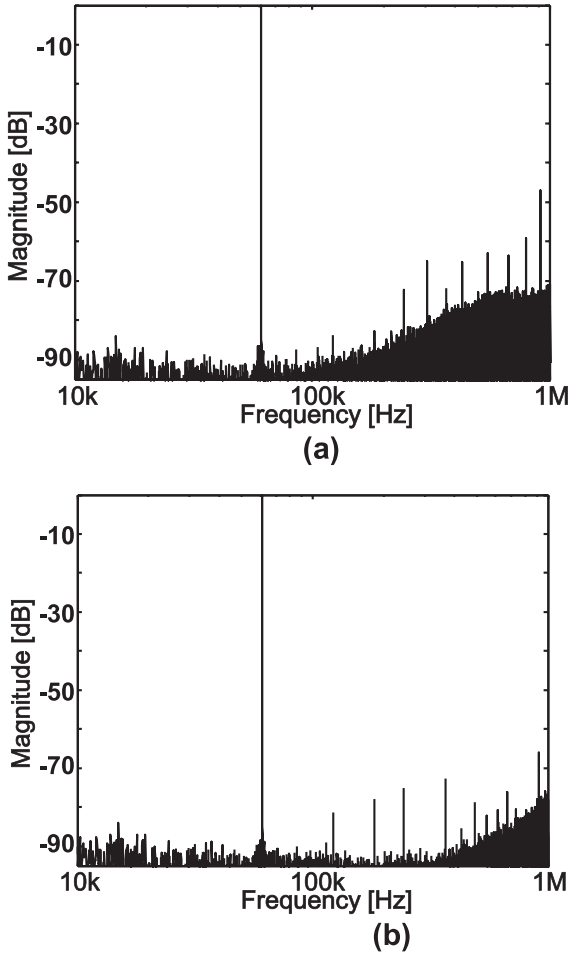

Fig. 7 Output spectra of (a) without LMS and (b) with LMS.

4. Measurement Results

A test chip was fabricated using a 65 nm CMOS process (Fig. 6). The TDC core occupies 700 μm^2 as an active area. The power supply voltage is 1.2 V.

Figures 7(a) and 7(b) show the measured output spectrum of the proposed TDC with and without the LMS filter.

Figure 8(a) presents a conceptual diagram of the first-order LMS filter, which estimates the ratio of the oscillation frequencies (desired coefficient: w_0) between the two FSOs adaptively in the manner described above. Figure 8(b) presents results of the estimated coefficients when the sampling rate is 16 MHz, the filter order is one, the internal coefficients are 16bits, and the step size is 0.001. The desired coefficient w_0 can be estimated until 4 milli-seconds. It is apparent that second-order noise shaping is achieved by the LMS filter (see Fig. 7(b)). In the spectra, the input signal frequency is 61 kHz, and the input width is 31.25 ns (the

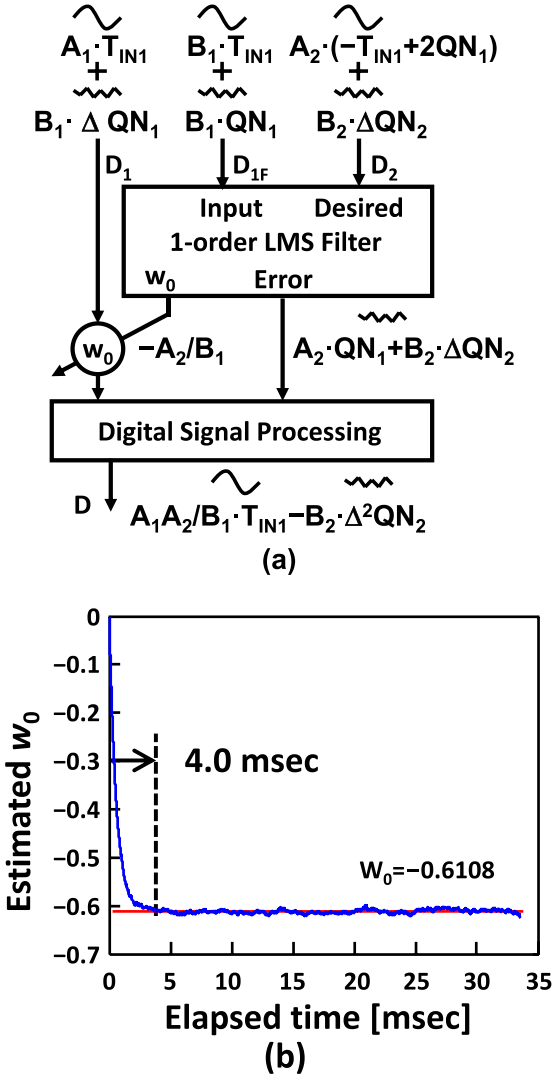

Fig. 8 (a) Block diagram of LMS for mismatch correction and (b) the elapsed time of the coefficient estimation.

Table 3 Chip characteristics.

Item	Data
Technology (nm)	65
Supply voltage (V)	1.2
Bandwidth (kHz)	500
Sampling rate (MS/s)	16
Power (mW)	0.281
SFDR (dB)	72
SNDR (dB)	61
ENOB (bits)	9.8
FoM (fJ/conv.step)	308
Active area (mm^2)	0.0007

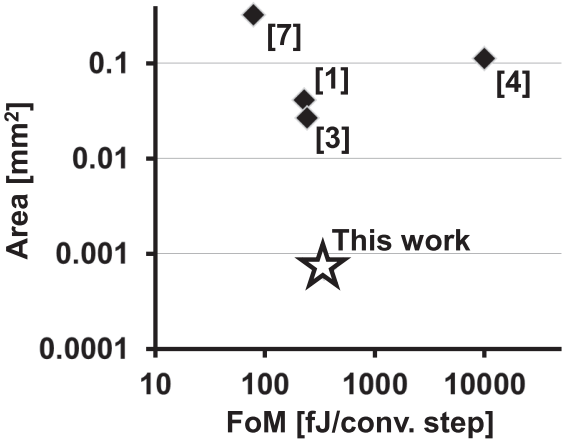

Fig. 9 Comparison with other state-of-the-art TDCs (a pipeline TDC [7] is added for area comparison).

sampling rate is 16 MHz). The SNDR is 61 dB.

In the test chip, there are some harmonic noises in the outputs of the TDC, which were not found in the SPICE and MATLAB simulations. We suppose that the harmonic noises come from power lines of the oscillators. Except for such harmonic noises, Figs. 5 and 7 exhibit the same noise floor; owing to the second-order noise shaping effect, the both noise floors of the simulation and measurement are decreased by −20 dB (roughly from −70 dB to −90 dB) in a bandwidth of 100 kHz and 1 MHz. At this point, this measured result matches with the simulated results described in Sect. 3.

The FSOs and QNP consume 211 μW. The peripheral buffers and flipflops consume 70 μW. The test chip performance is summarized in Table 3. Our TDC is smaller than any other TDCs (see Fig. 9).

5. Conclusion

We proposed a 700-μm^2, 61-dB, and 281-μW second-order MASH ΔΣ TDC. In the proposed architecture, analog circuits such as opamps and switched capacitors can be eliminated. The control and calibration of the TDC are implemented with digital circuits, which achieve the low-cost and low-power TDC. The proposed TDC thereby maintains scalability with future advanced processes. Because the proposed architecture is configured by using digital circuits in the standard cell library, the design cost and turn around time (TAT) are reduced as well.

The proposed TDC exploits an oversampling technique. Therefore, by increasing the sampling rate, we can further enhance the quantization accuracy (time resolution) and signal bandwidth. Furthermore, the ENOB can be improved with the third-order or higher MASH topology by connecting multiple stages. As process technology advances, the ring oscillator frequency becomes faster, which is good news for the proposed TDC. Process scaling will back up our proposed TDC architecture in the future.

If we adopt a voltage-to-time converter for our architecture, this TDC can be adopted for a range of applications such as a ubiquitous sensor, in which many ADCs must be implemented on a chip. Therein, one node collects various information through the ADCs; it then forwards it to a base station. Small-area and low-power ADC without opamps or capacitors is useful for the future ubiquitous applications.

Acknowledgments

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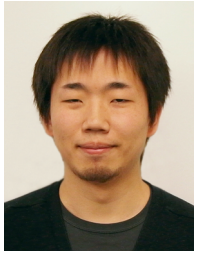

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