PERFECT WIRELESS EXPERIENCE

FM101-CG

Hardware Guide

V1.0

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Contents

Change History

V1.0 (2021-11-17)	Initial version.

1. Foreword

1.1. Document Description

This document describes the electrical characteristics, RF performance, dimensions and application environment, etc. of the FM101-CG wireless module. With the assistance of this document and other related documents, application developers can quickly understand the hardware functions of the FM101-CG module and develop product hardware.

1.2. Safety Instructions

By following the safety guidelines below, you can ensure your personal safety and help protect the product and work environment from potential damage. Product manufacturers need to communicate the following safety instructions to end users. Fibocom Wireless does not assume any responsibility for the consequences caused by users' misuse because they do not comply with these safety rules.

Road safety first! When you are driving, do not use any handheld mobile device even if it has a hand-free feature. Stop the car before making a call.

Please turn off the mobile device before boarding. The wireless feature of the mobile device is not allowed on the aircraft to prevent interference with the aircraft communication system. Ignoring this note may result in flight safety issue or even violate the law.

When in a hospital or health care facility, please be aware of restrictions on the use of mobile devices. Radio frequency interference may cause medical equipment to malfunction, so it may be necessary to turn off the mobile device.

The mobile device does not guarantee that an effective connection can be made under any circumstances, for example, when there is no prepayment for the mobile device or (U)SIM is invalid. When you encounter the above situation in an emergency, please remember to use emergency calls, and ensure that your device is turned on and in an area with strong signal.

Your mobile device receives and transmits RF signals when it is powered on. Your mobile device will receive and transmit RF signals when it is turned on. RF interference occurs when it is near a TV, radio, computer, or other electronic device.

Keep mobile device away from flammable gases. Turn off the mobile device when you are near to gas stations, oil depots, chemical plants or explosive workplaces. There are potential safety hazards when operating electronic equipment in any potentially explosive area.

2. Product Overview

2.1. Product Introduction

Fibocom FM101-CG module is designed based on Qualcomm SDX12 platform, supporting Cat 6 network level, and supporting CA network architecture. FM101-CG integrates Baseband, Memory, PMIC, Transceiver, PA and other core devices, supporting TDD-LTE. The maximum downlink rate supported in CA mode is 261 Mbps, and the maximum uplink rate is 30 Mbps. FM101-CG is designed with M.2 package and is applicable to various scenarios such as CPE, VR/AR, gateway, Internet TV set-top box, and intelligent monitoring.

2.2. Product Specifications

2.2.1. Radio Frequency Features

Table 1. Operating band

System	FM101-CG
TDD-LTE	Band 42/43/48

Table 2. Transmission capacity

System	FM101-CG
LTE	DL peak rate 261 Mbps UL peak rate 30 Mbps DL 4 × 2 MIMO

Table 3. Modulation features

System	FM101-CG
LTE	Support 3GPP R12 Support DL 64QAM, 16QAM and QPSK modulations Support UL 16QAM and QPSK modulation Support RF bandwidth 5 MHz to 20 MHz

2.2.2. Other Key Features

Table 4. Other key features

Item	Description
Power supply	DC: 3.135 V–4.4 V Typical voltage: 3.8 V
Processor	Qualcomm SDX12, 14nm process, single-core ARM Cortex-A7, up to 1.28 GHz
Storage	2Gb LPDDR2 + 2Gb NAND Flash
Supported systems	Linux/Android/Windows
Power class	Class 3 (23dBm ± 2dB) for LTE bands
Satellite positioning	GPS/GLONASS/Galileo/BDS
SMS	Support
Audio interface	Support PCM/I^2S digital audio interface
USB interface	A group of USB 3.0 superspeed (SS) interfaces with data transmission rate up to 5 Gbps Compatible with USB 2.0 highspeed (HS) interfaces, with data transmission rate up to 480 Mbps Used for AT command transmission, data transmission, software debugging, software upgrading, etc.

Item	Description
PCIe interface	PCIe Gen2 x 1Lane, the maximum transmission rate is 5GT/s, and RC mode is supported
SIM interface	2 groups of SIM card interfaces, supporting dual SIM single standby Support USIM: 1.8 V and 3 V
I^2C interface	1 group I^2C with a maximum speed of 3.4 Mbps
Physical characteristic	Dimensions: 30 mm × 42 mm × 2.3 mm Packaging: M.2 Weight: TBD
Temperature range	**Operating temperature: –30°C to 75°C** The module works normally within this temperature range, and the related performance meets the requirements of 3GPP standards. **Extended temperature: –40°C to 85°C** The module works normally within this temperature range, and the baseband and RF functions are normal. However, some indicators may exceed the range of 3GPP standards. When the temperature returns to the normal working range of the module, all the indicators of the module meet the requirements of 3GPP standards. **Storage temperature: –40°C to 90°C** The storage temperature range of the module when the module is powered off.
Software upgrade	Through USB interface/FOTA
Environmental standards	RoHS and halogen-free

2.3. Supported CA Combinations

Table 5. CA combinations supported by FM101-CG

Combination	FM101-CG
2DLCA	B42C B48C

2.4. Functional Block Diagram

Functional block diagram shows the main hardware functions of the FM101-CG module, including the baseband and RF functions.

Baseband section

- CPU
- PMIC
- LPDDR2
- NAND
- USB, PCIe, (U)SIM, PCM/I^2S, I^2C
- LTE TDD controller

RF section

- RF Transceiver
- RF PA
- RF Switch
- RF filter
- Antenna

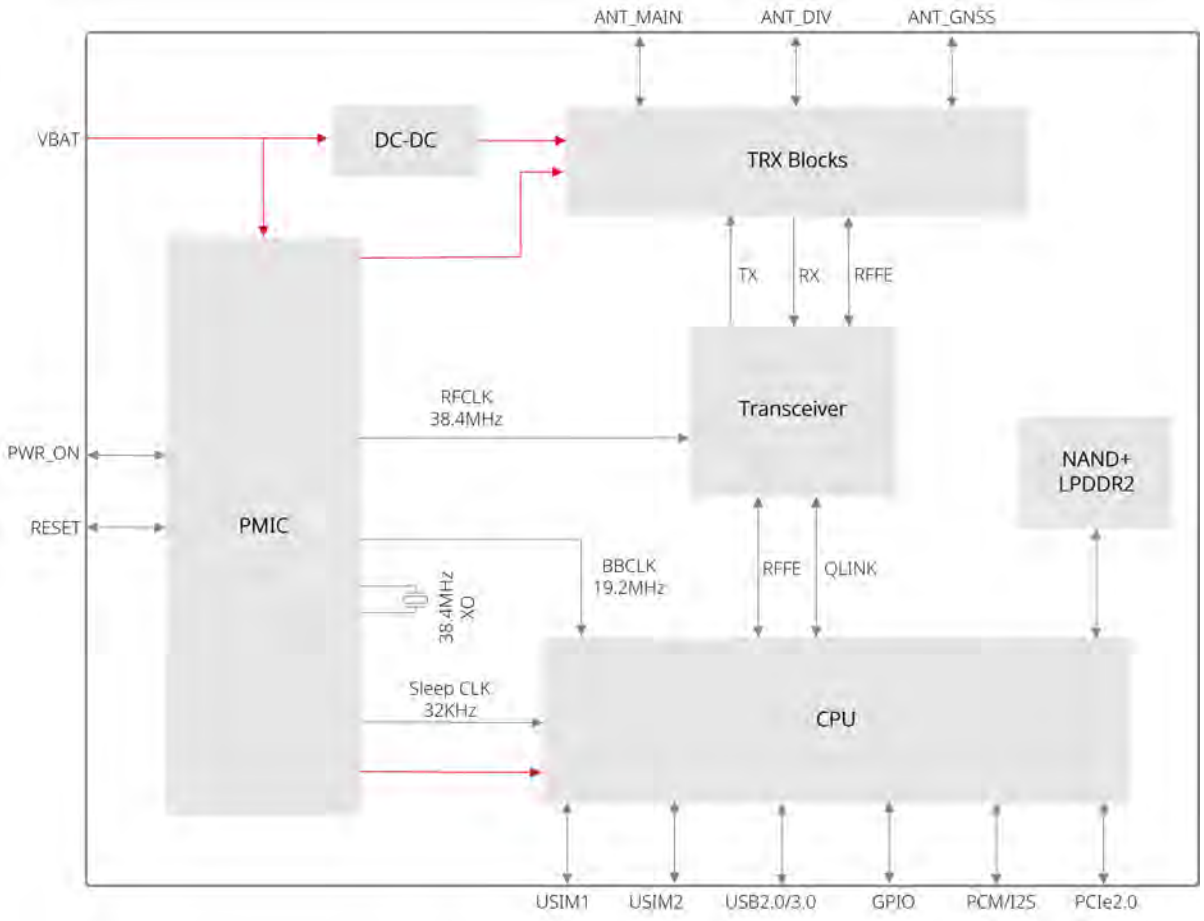


Figure 1. Functional block diagram

2.5. Evaluation Board

Fibocom provides EVB-M.2 evaluation board to facilitate module debug and testing. For how to use it, see *FIBOCOM EVB-M2 User Guide*.

3. Pin Definition

3.1. Pin Distribution

The FM101-CG module uses M.2 packaging and have 75 pins in total. The following figure shows the pin mapping.

74	VCC	CONFIG_2	75
72	VCC	GND	73
70	VCC	GND	71
68	I2S_MCLK	CONFIG_1	69
66	UIM1_DETECT	RESET_N	67
64	COEX_UART_TXD	GRFC4	65
62	COEX_UART_RXD	GRFC5	63
60	COEX3/GPIO86	GRFC6	61
58	RFFE_SDATA	GRFC7	59
56	RFFE_SCLK	GND	57
54	PEWAKE#	REFCLKP	55
52	CLKREQ#	REFCLKN	53
50	PERST#	GND	51
48	UIM2_PWR	PERp0	49
46	UIM2_RESET	PERn0	47
44	UIM2_CLK	GND	45
42	UIM2_DATA	PETp0	43
40	SIM2_DETECT	PETn0	41
38	WAKEUP_IN	GND	39
36	UIM1_PWR	USB_SS_RX_P	37
34	UIM1_DATA	USB_SS_RX_M	35
32	UIM1_CLK	GND	33
30	UIM1_RESET	USB_SS_TX_P	31
28	I2S_WA	USB_SS_TX_M	29
26	W_DISABLE2#	GND	27
24	I2S_TX	DPR	25
22	I2S_RX	WOWWAN#	23
20	I2S_SCK	CONFIG_0	21
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
10	LED1#	GND	11
8	W_DISABLE1#	USB_DM	9
6	FULL_CARD_POWER_OFF#	USB_DP	7
4	VCC	GND	5
2	VCC	GND	3
		CONFIG_3	1

Figure 2. Pin mapping

3.2. Pin Function

The FM101-CG module pin function is described in the following table.

Table 6. M.2 pin function description

Pin Number	Pin Name	I/O	Reset Status	Pin Description	Type
1	CONFIG_3	DO	NC	NC, WWAN-PCIe is configured for FM101-CG module, USB_SS interface type M.2 module	- -
2	VCC	PI	*	Power input	Power supply
3	GND	- -	- -	Ground	Power supply
4	VCC	PI	*	Power input	Power supply
5	GND	- -	- -	Ground	Power supply
6	FULL_CARD_POWER_OFF#	DI	PU	Module on/off control, high-level on, low-level off; internal pull-up	CMOS 3.3V/1.8V
7	USB_DP	DIO	*	USB 2.0 data +	0.3V–3V
8	W_DISABLE1#	DI	PU	Turn off WWAN of the module, i.e. flight mode, active low	CMOS 3.3V/1.8V
9	USB_DM	DIO	*	USB 2.0 data –	0.3V–3V
10	LED1#	OD	T	System status indication, open drain output	*

Pin Number	Pin Name	I/O	Reset Status	Pin Description	Type
11	GND	- -	- -	Ground	Power supply
12	Notch	*	*	Notch groove	*
13	Notch	*	*	Notch groove	*
14	Notch	*	*	Notch groove	*
15	Notch	*	*	Notch groove	*
16	Notch	*	*	Notch groove	*
17	Notch	*	*	Notch groove	*
18	Notch	*	*	Notch groove	*
19	Notch	*	*	Notch groove	*
20	I2S_SCK	DO	PD	I^2S serial clock, reserved	CMOS 1.8V
21	CONFIG_0	- -	NC	NC, WWAN-PCIe is configured for FM101-CG module, USB_SS interface type M.2 module	- -
22	I2S_RX	DI	PD	I^2S serial data receiving, reserved	CMOS 1.8V
23	WOWWAN#	DO	PD	Wakeup host	CMOS 1.8V
24	I2S_TX	DO	PD	I^2S serial data transmission, reserved	CMOS 1.8V
25	DPR	DI	PU	Dynamic power control for SAR interrupt detection, active low, reserved	CMOS 3.3V/1.8V

Pin Number	Pin Name	I/O	Reset Status	Pin Description	Type
26	W_DISABLE2#	DI	PU	GNSS positioning is disabled, active low, reserved	CMOS 3.3V/1.8V
27	GND	- -	- -	Ground	Power supply
28	I2S_WA	DO	PD	I^2S byte selection, left and right channels, reserved	CMOS 1.8V
29	USB_SS_TX_M	DO	*	Ultra high speed USB data transmitting negative	*
30	UIM1_RESET	DO	L	SIM card 1 reset	CMOS 3V/1.8V
31	USB_SS_TX_P	AO	*	Ultra high speed USB data transmitting positive	*
32	UIM1_CLK	DO	L	SIM card 1 clock	CMOS 3V/1.8V
33	GND	- -	- -	Ground	Power supply
34	UIM1_DATA	DIO	L	SIM card 1 data	CMOS 3V/1.8V
35	USB_SS_RX_M	AI	*	Ultra high speed USB data receiving negative	*
36	UIM1_PWR	PO	*	SIM card 1 power supply, 3V/1.8V	CMOS 3V/1.8V
37	USB_SS_RX_P	AI	*	Ultra high speed USB data receiving positive	*
38	WAKEUP_IN	DI	*	Peripheral wake-up module control signal	CMOS 1.8V

Pin Number	Pin Name	I/O	Reset Status	Pin Description	Type
39	GND	- -	- -	Ground	Power supply
40	SIM2_DETECT	DI	*	SIM card 2 detection, and external pull-up and pull-down are required. A card is available at high level by default, SPI_MISO (Reserved)	CMOS 1.8V
41	PETn0	DO	*	PCIe data transmitting negative	*
42	UIM2_DATA	DIO	L	SIM card 2 data, SPI_MOSI (Reserved)	CMOS 3V/1.8V
43	PETp0	DO	*	PCIe data transmitting positive	*
44	UIM2_CLK	DO	L	SIM card 2 clock, SPI_CLK (Reserved)	CMOS 3V/1.8V
45	GND	- -	- -	Ground	Power supply
46	UIM2_RESET	DO	L	SIM card 2 reset, SPI_CS(Reserved)	CMOS 3V/1.8V
47	PERn0	DI	*	PCIe data receiving negative	*
48	UIM2_PWR	PO	*	SIM card 2 power supply	CMOS 3V/1.8V
49	PERp0	DI	*	PCIe data receiving positive	*
50	PERST#	DI	PD	Module PCIe interface reset. Active low, and an external pull-up resistor is required	CMOS 3.3V/1.8V
51	GND	- -	- -	Ground	Power supply

Pin Number	Pin Name	I/O	Reset Status	Pin Description	Type
52	CLKREQ#	DIO	T	PCIe clock request signal, active low, open drain output, an external pull-up resistor needs to be reserved	CMOS 3.3V/1.8V
53	REFCLKN	DIO	*	PCIe reference clock differential negative signal	*
54	PEWAKE#	DO	T	PCIe wake-up signal, active low, open drain output, an external pull-up resistor is required	CMOS 3.3V/1.8V
55	REFCLKP	DIO	*	PCIe reference clock differential positive signal	*
56	RFFE_SCLK	DO	PD	RFFE-MIPI serial clock signal, I2C_SCL (Reserved)	CMOS 1.8V
57	GND	- -	- -	Ground	Power supply
58	RFFE_SDATA	DIO	PD	RFFE-MIPI serial data signal, I2C_SDA (Reserved)	CMOS 1.8V
59	GRFC7*	DO	PD	Tuning antenna control bit, reserved	CMOS 1.8V
60	COEX3/GPIO 86	DI	*	LTE/WLAN common control signal	CMOS 1.8V
61	GRFC6*	DO	PD	Tuned antenna control bit 1, reserved	CMOS 1.8V
62	COEX_UART_ RXD*	DI	- -	LTE and WLAN share a serial port receiving signal line, reserved	CMOS 1.8V

Pin Number	Pin Name	I/O	Reset Status	Pin Description	Type
63	GRFC5*	DO	PD	Tuned antenna control bit 2, reserved	CMOS 1.8V
64	COEX_UART_TXD*	DO	- -	LTE and WLAN share a serial port transmission signal line, reserved	CMOS 1.8V
65	GRFC4*	DO	PD	Tuned antenna control bit, reserved	*
66	UIM1_DETECT	DI	PU	SIM card 1 detection, external pull-up and pull-down are required. A card is available at high level by default	CMOS 1.8V
67	RESET_N	DI	PU	Module reset. Active low	CMOS 1.8V
68	I2S_MCLK	DO	*	I2S MCLK clock output	*
69	CONFIG_1	DO	GND	GND, WWAN–PCIe is configured for the FM101-CG module, USB_SS interface type M.2 module	- -
70	VCC	PI	*	Power input	Power supply
71	GND	- -	- -	Ground	Power supply
72	VCC	PI	*	Power input	Power supply
73	GND	- -	- -	Ground	Power supply

Pin Number	Pin Name	I/O	Reset Status	Pin Description	Type
74	VCC	PI	*	Power input	Power supply
75	CONFIG_2	DO	NC	NC, WWAN-PCIe is configured for FM101-CG module, USB_SS interface type M.2 module	- -

Pins marked with * are reserved functions or under development. Unused pins remain floating.

Table 7. I/O parameter description

Type	Description
PI	Power input
PO	Power output
DI	Digital input
DO	Digital output
DIO	Digital input/output
AI	Analog input
AO	Analog output
AIO	Analog input/output
OD	Open drain

4. Electrical Characteristics

4.1. Limit Voltage Range

The limit voltage includes the absolute limit voltage and the operating limit voltage. The absolute limit voltage is the maximum voltage that the module can bear, beyond which the module may be damaged. The operating limit voltage is the normal operating voltage range of the module, beyond which the module will have an abnormal performance.

4.1.1. Absolute Limit Voltage

The following table describes the absolute limit voltage ranges of FM101-CG module.

Table 8. Absolute limit voltage range

Parameter	Description	Minimum Value (V)	Typical Value	Maximum Value (V)
VBAT	Power supply	–0.3	3.8	4.75
GPIO	Digital IO level supply voltage	–0.3	1.8	2.1

4.1.2. Recommended Operating Voltage

Table 9. Recommended operating voltage (signal)

Signal	Logical low level		Logical high level	
	Minimum Value (V)	Maximum Value (V)	Minimum Value (V)	Maximum Value (V)
Digital input	–0.3	0.36	0.7 × VDD	VDD + 0.3
Digital output	0	0.45	VDD – 0.45	VDD
RESET_N	–0.3	0.5	1.25	1.89
FCPO#	–0.3	0.5	1.25	1.89

Table 10. Recommended operating voltage (power supply)

Parameter	I/O	Minimum Value (V)	Typical Value	Maximum Value (V)
VBAT	PI	3.135	3.8	4.4
USIM1_VDD	PO	1.75/2.8	1.8/2.85	1.85/2.928
USIM2_VDD	PO	1.75/2.8	1.8/2.85	1.85/2.928

4.2. Power Consumption

The power consumption of FM101-CG module measured under 3.8 V power supply is described in the following table. For AT commands used for USB sleep and wakeup, see *Fibocom_FM101_AT Commands User Manual*.

Table 11. Power consumption

Parameter	Mode	Status	Average Current Typical Value (mA)
I_{off}	Power off	Module power-off	0.06
I_{sleep}	TDD-LTE	Paging Cycle #64 (USB sleep)	3.3
	TDD-LTE	Paging Cycle #256 (USB sleep)	2.2
	Radio Off	AT+CFUN=0 (USB sleep)	1.8
I_{idle}	TDD-LTE	Paging Cycle #32 (USB wakeup)	33
		Paging Cycle #64 (USB wakeup)	32
		Paging Cycle #128 (USB wakeup)	31
		Paging Cycle #256 (USB wakeup)	31
$I_{LTE\text{-}RMS(10MHz\ 1RB)}$	TDD-LTE	Band42 @+23dBm	450
		Band43 @+23dBm	450
		Band48 @+23dBm	450

Table 12. 2CA power consumption

2CA Typical Combination	Transmitting Band@FRB@Data Transmission Status	Typical Current (mA)
42C	B42+B42 @+21dBm	TBD
48C	B48+B48 @+21dBm	TBD

5. Functional Interface

5.1. Power Supply

The following table describes the power interface of FM101-CG module.

Table 13. Power interface

Pin Name	I/O	Pin Number	Description
VBAT	PI	2,4, 70, 72, 74	Module power supply, 3.135V–4.4V, 3.8V is recommended
GND	G	3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73	GND, all GND pins must be grounded

Power Input

The FM101-CG module is powered on through the VBAT pin. The following figure shows the recommended power supply design.

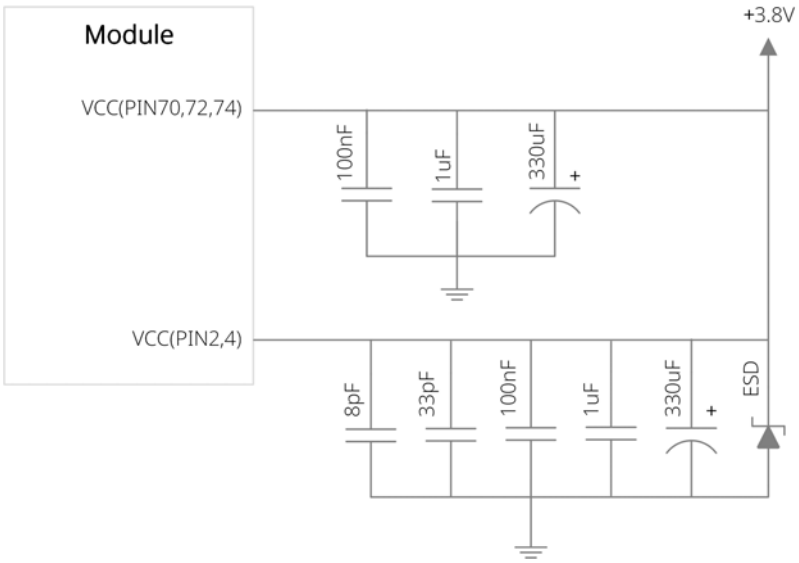


Figure 3. Recommended power supply design

The filter capacitor design of power supply is shown in the following table.

Table 14. Power supply filter capacitor design

Recommended Capacitor	Application	Description
330uF x 2	Voltage stabilizing capacitor	To reduce the power supply fluctuation when the module works, it is required to adopt low ESR capacitor, which is not less than 440uF, and the driving capacity of VBAT power supply current is not less than 2.0 A.
1uF, 100nF	Digital signal noise	Filter out interference caused by clock and digital signals.
33pF	850 MHz/900 MHz band	Filter out low band RF interference
8.2pF	1800/1900/2100/2300/ 2500/2600 MHz band	Filter out middle/high band RF interference.

Stable power supply ensures proper operating of the FM101-CG module. During design, ensure that the power supply ripple is less than 300 mV (circuit ESR < 100 mΩ). When the module is working in maximum load, ensure that the power supply voltage is not lower than 3.135V. Otherwise, the module may power off or restart. When the module is working in Burst transmit state, the power limit is shown in the following figure.

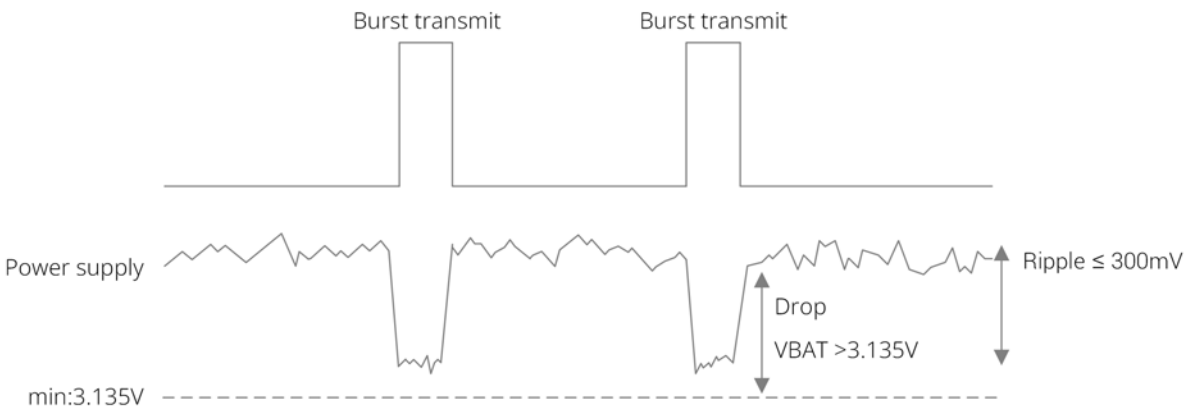


Figure 4. Power supply limit

5.2. Control Interface

The module has three control signals for power on/off and reset of the module. The pins are defined in the following table.

Table 15. Control signal

Pin Name	I/O	Pin Number	Description
RESET_N	DI	67	In the power-on state, pull down RESET_N for 0.5s to 3s, and then release it. The module is reset. The chip is internally pulled up.
FULL_CARD_POWER_OFF#(3.3V/1.8V)	DI	6	Module on/off signal, pull up to power on, and pull down to power off. In the power-off state, pull up the FCP# for more than 1.2s. The module is powered on.

5.2.1. Power on/off

5.2.1.1. Power on

When the module power-on pin FCPO# (FULL_CARD_POWER_OFF#) is connected to an external voltage of 3.3 V or 1.8 V, the module is powered on. When the AP (Application Processor) controls the power-on of the module, it is recommended to use GPIO with the reset status of low or internal pull-down.

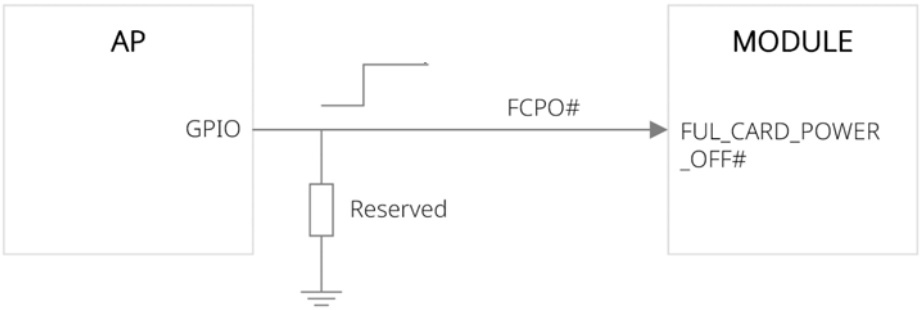


Figure 5. AP controls the power-on circuit of the module

5.2.1.2. Power-on Sequence

The following figure shows the power-on sequence.

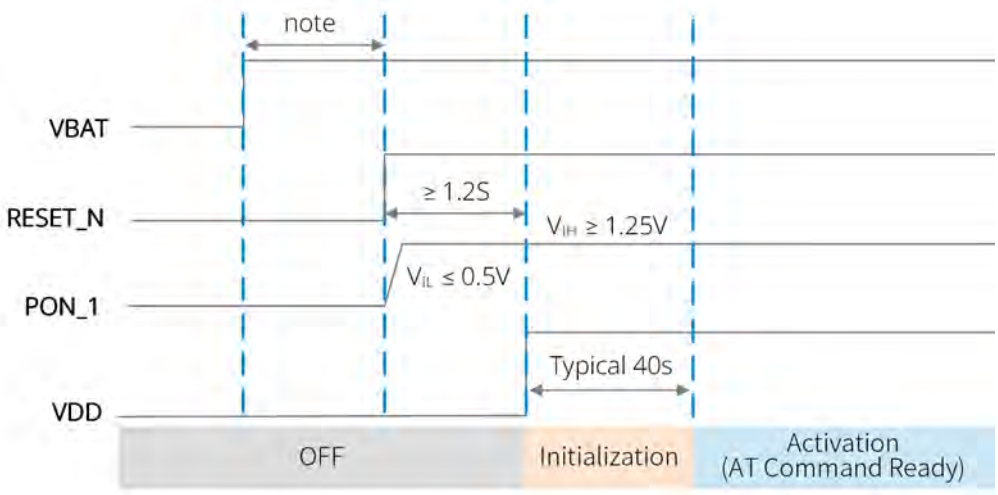


Figure 6. Power-on sequence (FCPO#)

Before pulling the FCPO# pin high, ensure that the VBAT voltage is stable. It is recommended that the time interval between powering on VBAT and pulling low or high the power-on control pin is not less than 40ms. The power-on control is automatically pulled up inside the module.

5.2.1.3. Power Off

When the module is powered on, pull down FCPO#, and the module is powered off. The

recommended power-off sequence is shown in the following figure.

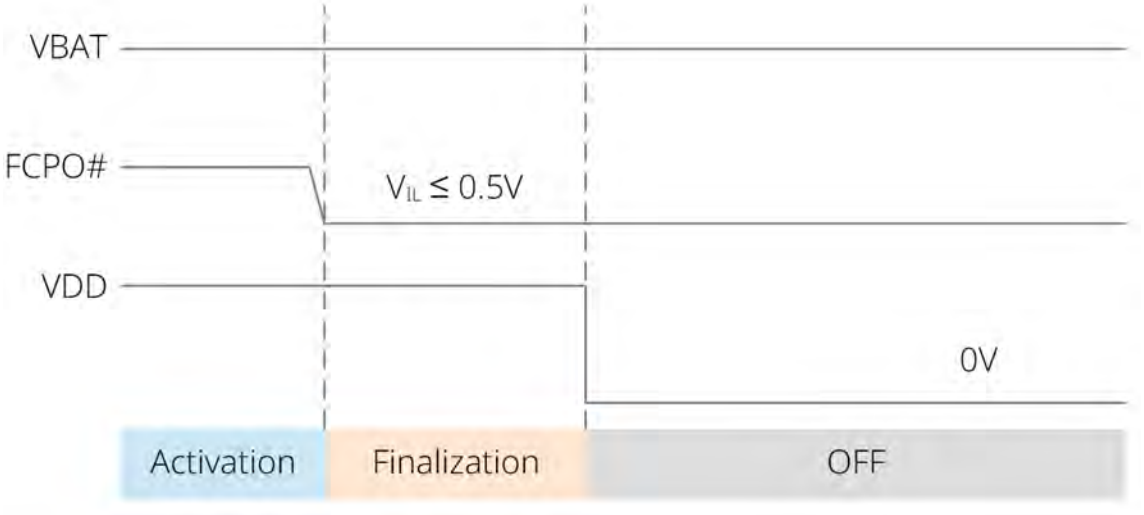


Figure 7. Recommended power-off sequence

5.2.2. Reset

FM101-CG module can be reset by hardware and software.

Table 16. Reset methods

Reset Method	Action
Hardware reset	Pull down the RESET_N pin for 0.5s or more, and then release
Software reset	Send the **AT+CFUN=15** command

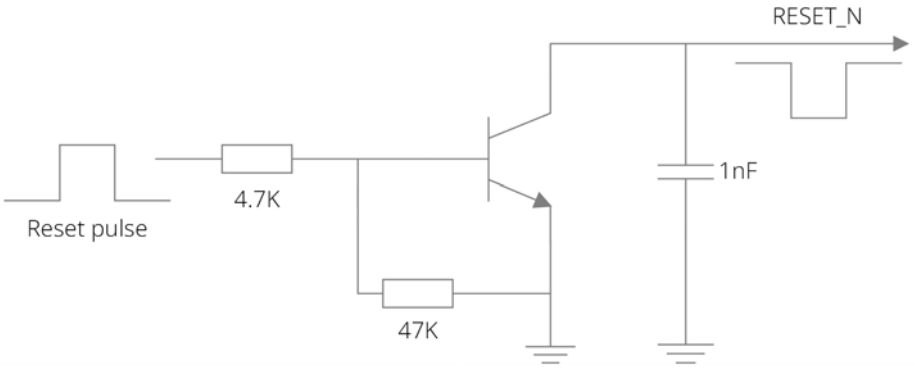


Figure 8. OC drive reset reference circuit

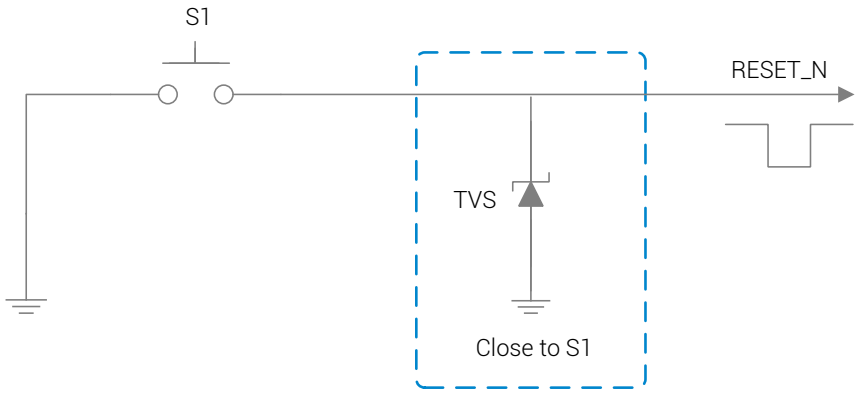


Figure 9. Button reset reference circuit

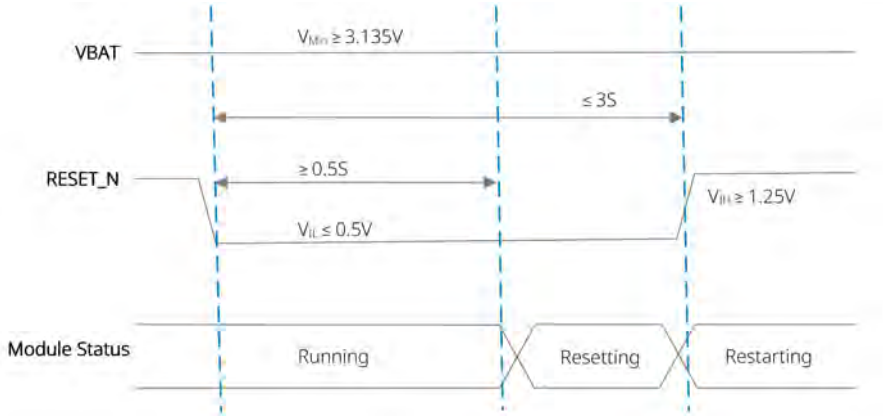


Figure 10. Reset sequence

It is recommended to wait at least 20 seconds between two reset operations. The RESET pin can be internally pulled up, without external pull-up. Keep the pin floating when it is not used.

5.3. LED1#

The LED1# signal is used to indicate the operating status of the module, as described in the table below.

Table 17. Network status indication

Module Operating Mode	LED1# Signal
RF function is enabled	Low level (LED on)
RF function is disabled	High level (LED off)

The LED driver circuit is shown in the following figure.

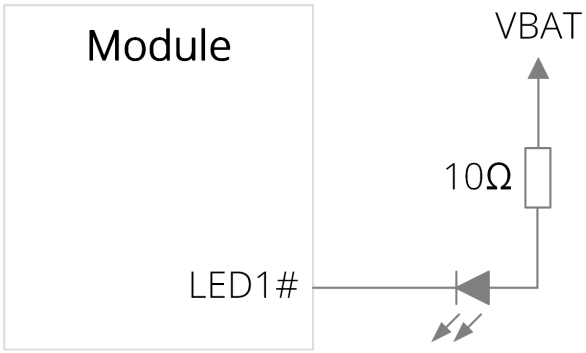


Figure 11. Reference circuit of network status indicators

5.4. (U)SIM Card Interface

FM101-CG module has built-in (U)SIM card interface, and supports 1.8 V and 3.0 V (U)SIM cards.

5.4.1. (U)SIM Pin Definition

(U)SIM pin definition is described in the following table.

Table 18. (U)SIM pin definition

Pin Number	Pin Name	I/O	Reset Status	Description	Type
30	UIM1_RESET	DO	L	USIM1 reset	1.8V/3V
32	UIM1_CLK	DO	L	USIM1 clock	1.8V/3V
34	UIM1_DATA	DIO	L	USIM1 data	1.8V/3V
36	UIM1_PWR	PO	- -	USIM1 power supply	1.8V/3V

Pin Number	Pin Name	I/O	Reset Status	Description	Type
40	SIM2_DETECT	DI	- -	USIM2 detection Active high by default. And high level indicates a SIM card is inserted; and low level indicates a SIM card is removed.	1.8V
42	UIM2_DATA	DIO	L	USIM1 data	1.8V/3V
44	UIM2_CLK	DO	L	USIM1 clock	1.8V/3V
46	UIM2_RESET	DO	L	USIM1 reset	1.8V/3V
48	UIM2_PWR	PO	- -	USIM1 power supply	1.8V/3V
66	SIM1_DETECT	DI	- -	USIM1 detection Active high by default. And high level indicates a SIM card is inserted; and low level indicates a SIM card is removed.	1.8V

5.4.2. (U)SIM Interface Circuit

(U)SIM Card Slot with Card Detection Signal

(U)SIM card slot should be selected for (U)SIM design. It is recommended to use (U)SIM card slot with hot plug detection function.

The following figure shows the reference design circuit. When (U)SIM card is inserted, USIM_DET pin is at high level, when (U)SIM card is removed, USIM_DET pin is at low level.

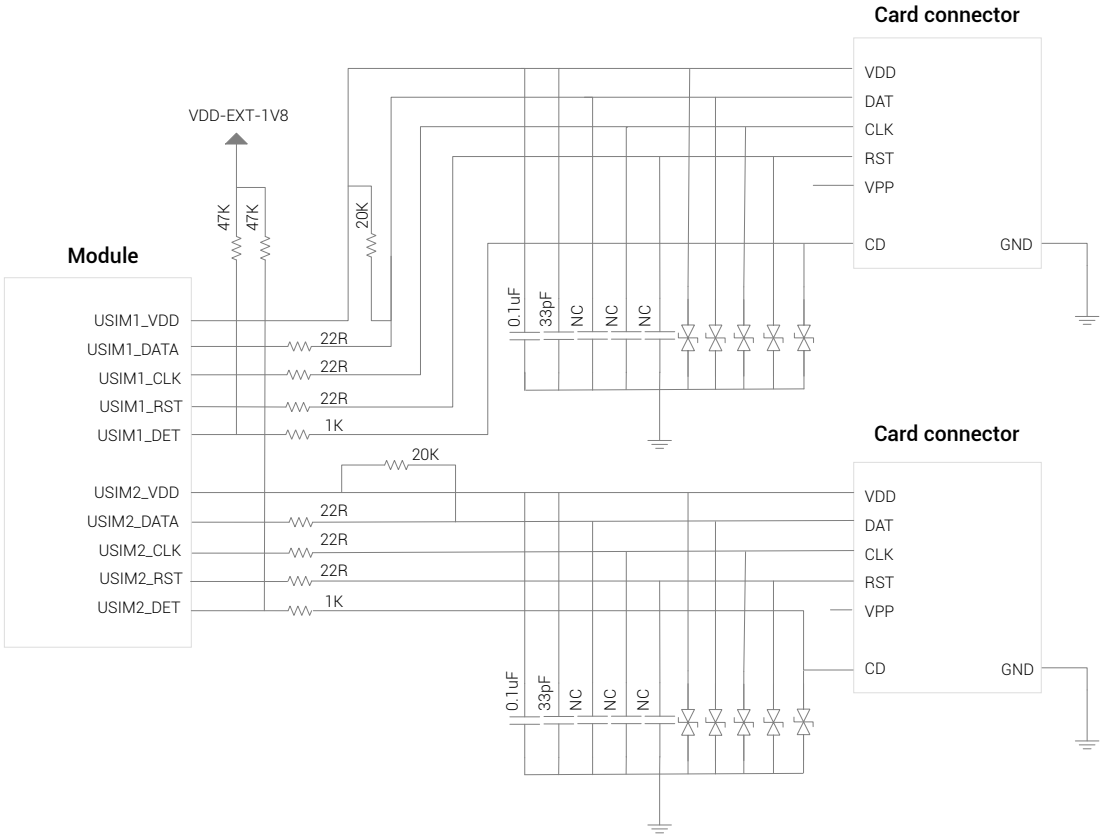


Figure 12. (U)SIM card slot with card detection signal

5.4.3. (U)SIM Card Hot Plug

The FM101-CG series module supports the (U)SIM card hot plug function. The module detects the status of the USIM1_DET/USIM2_DET pin to determine whether a (U)SIM card is inserted or removed.

USIM1_DET/USIM2_DET is active high by default (if the card is at high level, the card is inserted; otherwise, the card is removed). The hot plug detection can be enabled/disabled by the AT command as follows.

Table 19. (U)SIM card hot plug function configuration

AT Command	Function	Remark
AT+MSMPD=1	(U)SIM card hot plug detection is enabled	Default setting

AT Command	Function	Remark
AT+MSMPD=0	(U)SIM card hot plug detection is disabled	Effective after restart

5.4.4. (U)SIM Design Requirements

(U)SIM circuit design must meet EMC standards and ESD requirements, and at the same time, EMS capability must be improved to ensure that the (U)SIM can work stably. The following points need to be strictly observed in the design:

- (U)SIM card slot should be located as close to the module as possible, and kept away from the RF antenna, DCDC power, clock signal lines and other strong interference sources.
- (U)SIM card slot is covered by metal shield shell to improve EMS.
- The routing length from the module to the (U)SIM card slot shall not exceed 100 mm. Longer cable will reduce signal quality.
- The USIM_CLK and USIM_DATA signal lines are grounded and isolated to avoid mutual interference. If conditions do not permit, at least the (U)SIM signal must be grounded as a set.
- The filter capacitor and ESD device of the (U)SIM card signal line are placed close to the (U)SIM card slot.
- The total capacitance of the equivalent capacitance and the parallel filter capacitance of the ESD device is less than 47pF.
- USIM_DATA requires a pull-up resistor of 20KΩ to USIM_VDD.
- Refer to the specification of (U)SIM card slot for PCB packaging design. The PCB surface layer under the 6 contactors should be keepout to avoid short circuit caused by the contactor pricked to the copper plane.

5.5. USB Interface

FM101-CG module supports USB 3.0 (5 Gb/s) ultra-high-speed data transmission, and is also compatible with USB high-speed (480 Mb/s) for download, debugging, data transmission and other functions.

USB pin definition is shown in the following table.

Table 20. USB pin definition

Pin Name	I/O	Pin Number	Description
USB_DP	AIO	7	USB 2.0 differential data signal (+)
USB_DM	AIO	9	USB 2.0 differential data signal (–)
USB_SS_TX_M	AO	29	USB 3.0 differential transmitting signal (–)
USB_SS_TX_P	AO	31	USB 3.0 differential transmitting signal (+)
USB_SS_RX_M	AI	35	USB 3.0 differential receiving signal (–)
USB_SS_RX_P	AI	37	USB 3.0 differential receiving signal (+)

5.5.1. USB Interface Circuit

The USB interface reference circuit is shown in the following figure.

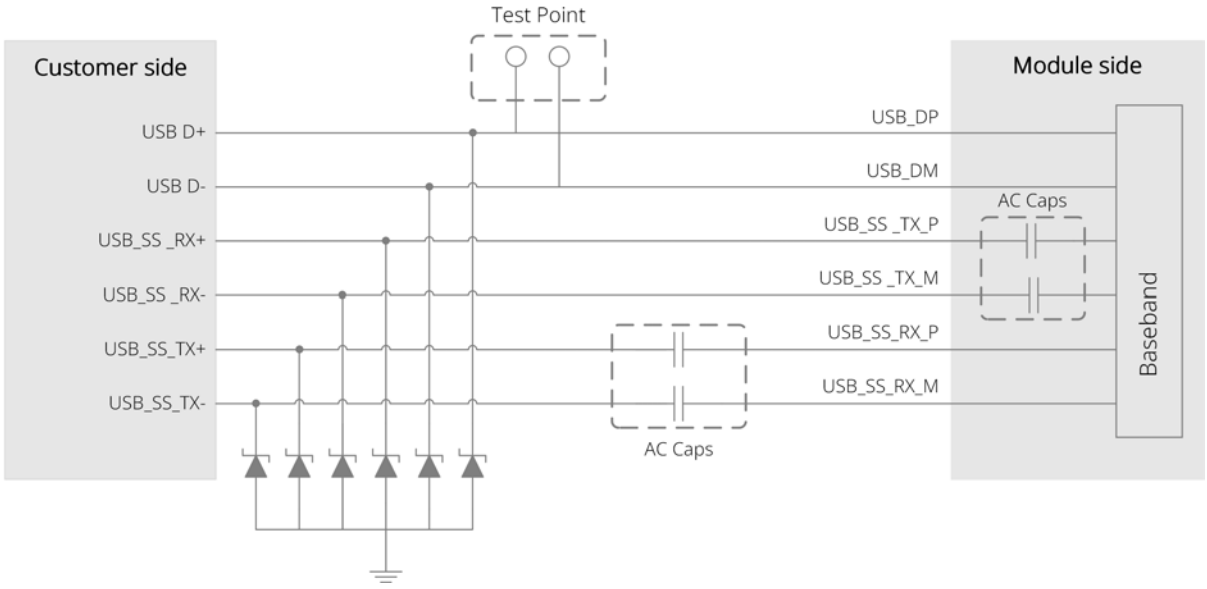


Figure 13. Reference design of USB interface circuit

5.5.2. USB Routing Rules

5.5.2.1. USB 2.0 Routing Rules

Since the module supports USB 2.0 High-Speed, TVS Junction capacitance on the USB_D+/D– differential signal line must be less than 1 pF, and a 0.5 pF TVS is recommended.

USB_D– and USB_D+ are high speed differential signal lines with the maximum transmission rate of 480 Mbit/s. The following rules must be strictly followed in PCB layout:

- USB_D– and USB_D+ signal lines should have the differential impedance of 90Ω±10Ω.
- USB_D– and USB_D+ signal line difference must be less than 2mm in length and parallel, avoiding the right-angle routing.
- USB_D– and USB_D+ signal lines should be routed on the layer that is closest to the ground layer, and protected with GND all around.

5.5.2.2. USB 3.0 Routing Rules

USB_SS_RX_P/USB_SS_RX_M and USB_SS_TX_P/USB_SS_TX_M are two groups of differential signals, with differential impedance controlled at 90Ω±7Ω; the trace length difference within the differential pair is controlled to ≤ 0.15 mm, and the trace length difference between the differential groups is controlled to ≤ 10 mm.

Minimize vias during high-speed cabling to ensure continuous impedance.

USB 3.0 signals are super speed differential signal lines with the maximum theoretical transfer rate of 5Gbps. The following rules shall be followed carefully in PCB layout:

- USB_SS_TX_P/USB_SS_TX_M and USB_SS_RX_P/USB_SS_RX_M are two pairs of differential signal lines, and their differential impedance should be controlled as 90Ω±7Ω.
- Traces in the differential pair must be parallel with equal length, and the length

difference should be controlled less than 0.15 mm, avoiding right-angle traces.

- Traces between differential pairs must be parallel with equal length, and the length difference should be controlled less than 10 mm, avoiding right-angle traces.
- The two pairs differential signal lines should be routed on the layer that is closest to the ground layer, and protected with GND all around.

5.6. I²C Interface

FM101-CG series module supports 1-way I²C interface, and the standard I²C specification, version 3.0 is applied.

I²C external pull-up is required. See Figure 14 for reference design.

Table 21. I²C pin definition

Pin Name	Pin Number	Type	Description
I2C_SDA	42	OD	I²C data signal
I2C_SCL	43	OD	I²C clock signal

5.7. PCM and I²S Digital Audio Interface

The FM101-CG module provides a digital audio interface (PCM/I²S) for communication with external codec and other digital audio devices.

5.7.1. PCM Interface Definition

PCM interface signals include transmission clock PCM_CLK, frame synchronization signal PCM_SYNC, and input and output PCM_IN/PCM_OUT.

Table 22. PCM pin definition

Pin Name	I/O	Pin Number	Description
I2S_SCK	IO	20	PCM clock signal, I2S_SCLK(Reserved), UART1_RTS(Reserved)
I2S_RX	DI	22	PCM input signal, I2S_D0(Reserved), UART1_RX(Reserved)
I2S_TX	DO	24	PCM output signal, I2S_D1(Reserved), UART1_CTS(Reserved)
I2S_WA	IO	28	PCM sync signal, I2S_WS(Reserved), UART1_TX(Reserved)
I2S_MCLK	DO	68	I^2S main clock signal (reserved)

Default transmission clock frequency is TBD MHz, sampling rate is TBD KHz, and resolution is TBD bit. The PCM channel can also be configured as I^2S interface. Please contact Fibocom technical support for adjustment.

5.7.2. PCM Application Circuit

The application reference circuit of the external Codec chip of the PCM interface is shown in the following figure.

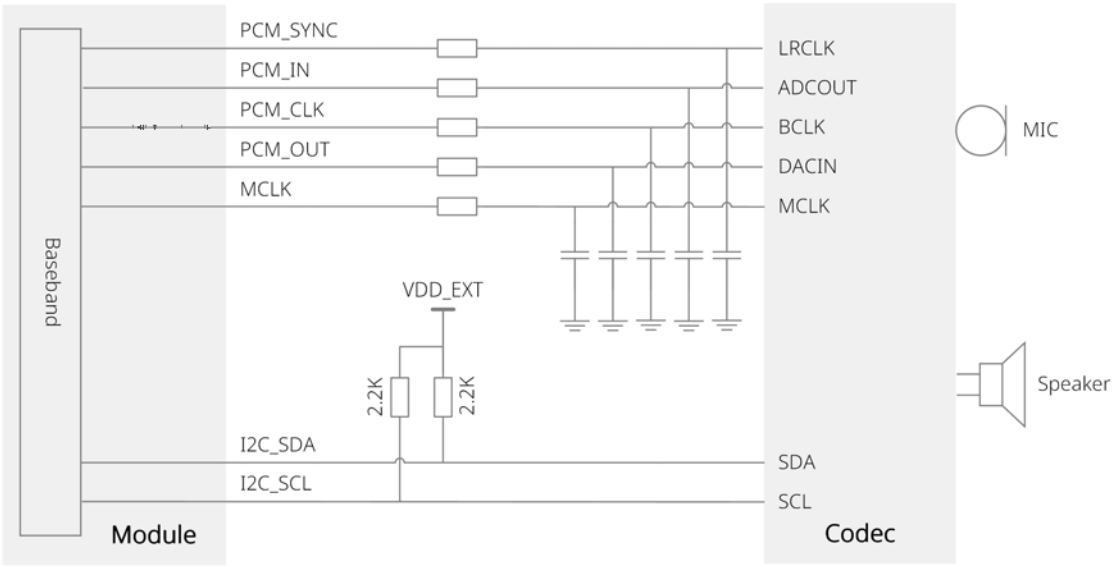


Figure 14. Reference circuit of the PCM interface external Codec chip

5.8. PCIe Interface

FM101-CG module supports a group of PCIe GEN 2.0 x 1 lanes.

Table 23. PCIe pin definition

Pin Name	I/O	Pin Number	Description
PETn0	DO	41	PCIe data transmitting signal negative
PETp0	DO	43	PCIe data transmitting signal positive
PERn0	DI	47	PCIe Data receiving signal negative
PERp0	DI	49	PCIe Data receiving signal positive
PERST#	DI	50	PCIe mode reset signal
CLKREQ#	DIO	52	PCIe clock request signal with external pull-up
REFCLKN	DIO	53	PCIe reference clock signal negative
PEWAKE#	DO	54	PCIe RC mode wake-up signal with external pull-up
REFCLKP	DIO	55	PCIe reference clock signal positive

5.8.1. PCIe Routing Rules

FM101-CG module supports PCIe 2.0 x1, including three differential pairs: transmitting pair TXP/N, receiving pair RXP/N and clock pair CLKP/N.

PCIe can achieve the maximum transmission rate of 5GT/s. The following rules must be strictly followed in PCB layout:

- The differential signal pairs are required to be parallel traces with equal length, and the difference in length is less than 0.15 mm.
- The differential signal pair traces shall be as short as possible and be controlled within 15 inch (380 mm) for AP end.
- The impedance of differential signal pair traces is controlled to be 100Ω±10%.
- Avoid discontinuous reference ground, such as segment and space.
- When the differential signal traces go through different layers, the via hole of ground signal should be close to that of signal, and generally, each pair of signals require 1-3 ground signal via holes and the traces shall never cross the segment of plane.
- Try to avoid bended traces and avoid introducing common-mode noise in the system, which will influence the signal integrity and EMI of differential pairs. As shown in the following Figure, the bending angle of all traces should be equal to or greater than 135°, the spacing between differential pair traces should be larger than 20mil, and the traces caused by bending should be greater than 1.5 times trace width at least. When a serpentine route is used for length match with another route, the bended length of each segment shall be at least 3 times the route width (≥ 3W). The largest spacing between the bended part of the serpentine trace and another one of the differential traces must be less than 2 times the spacing of normal differential traces (S1 < 2S).

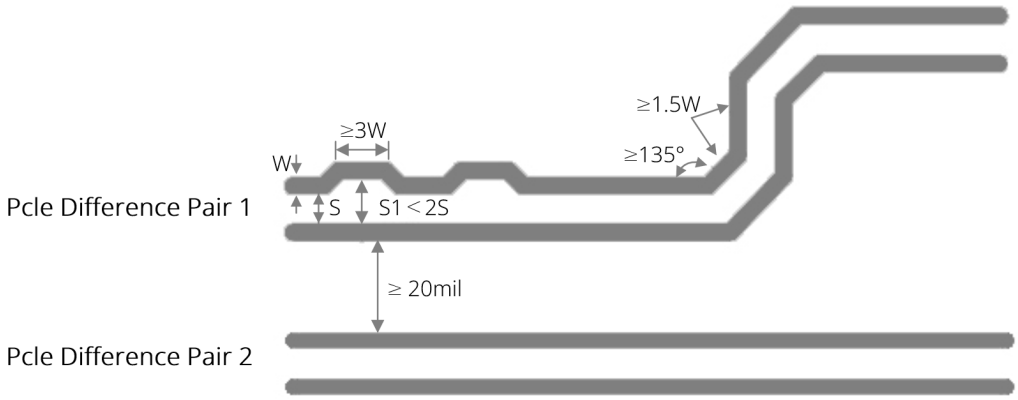


Figure 15. PCIe routing requirements

- The difference in length of two data lines in differential pair should be within 0.15 mm, and the length match must be met for all parts. When the length match is conducted for the differential lines, the designed position of correct match should be close to that of incorrect match, as shown in the following figure. However, there is no specific requirements for the length match of transmitting pair and receiving pair, that is, the length match is only required in the internal differential lines rather than between different differential pairs. The length match should be close to the signal pin and pass the small-angle bending routing design.

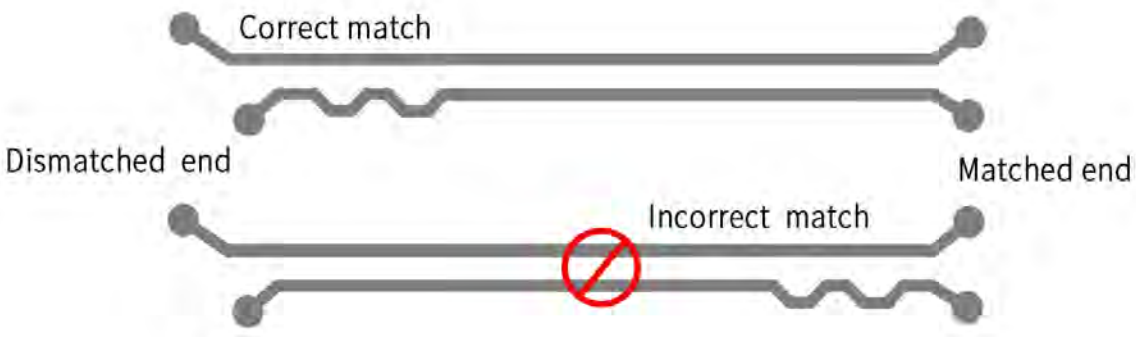


Figure 16. Length match design of PCIe difference pair

5.8.2. PCIe Application Circuit

Please refer to the following figure for PCIe application circuit, and *Fibocom_FM101-NA_Reference Design* for details.

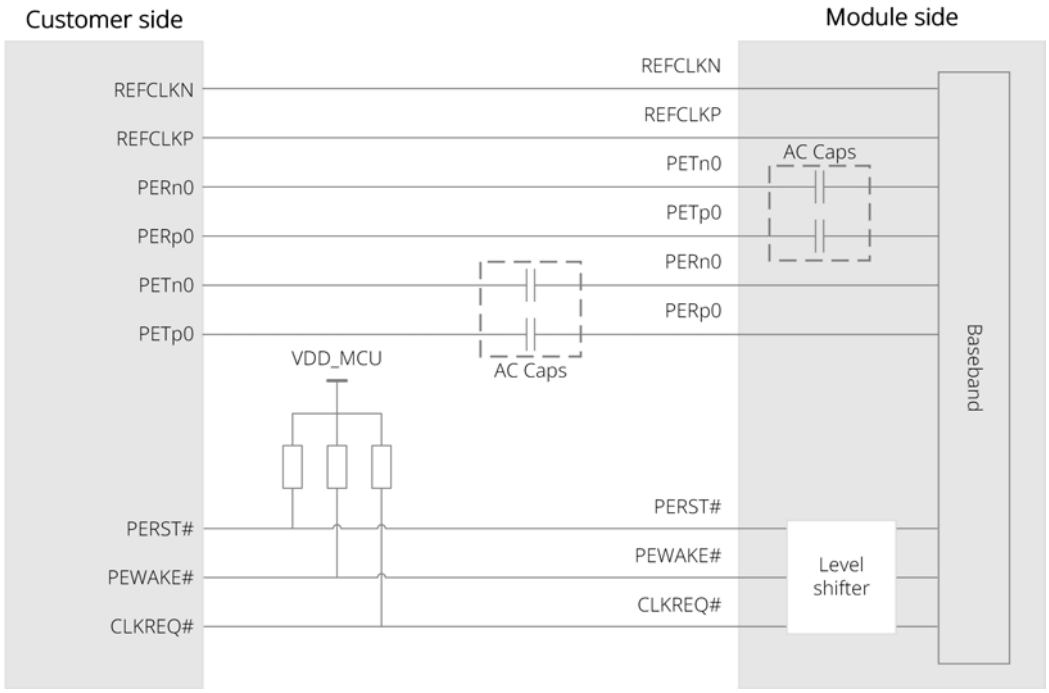


Figure 17. PCIe application circuit

5.9. Flight Mode Control Interface

W_DISABLE_N pin is described in the following table.

Table 24. W_DISABLE_N pin description

Pin Name	I/O	Pin Number	Description
W_DISABLE_N	DI	26	Module flight mode control (internal pulled up by default)

FM101-CG module supports two ways as described in the following table to enter flight mode:

Table 25. Ways for module to enter flight mode

1	Hardware GPIO interface control	Send AT+GTFMODE=1 to turn on the hardware control flight mode function; pulled up or float the pin The module is in normal mode when W_DISABLE# pin is pulled up by default. When this pin is pulled down, the module enters flight mode.
2	AT command control	The module uses software to control the flight mode by default. When AT+GTFMODE=0: run the AT+CFUN=0 command to enter flight mode. run the AT+CFUN=1 command to enter normal mode.

5.10. Sleep/Wakeup Interface

When the module is in sleep mode, the module can be awakened by pulling down WAKEUP_IN pin.

Table 26. Sleep/wakeup interface

Pin Name	I/O	Pin Number	Description
WAKEUP_IN	DI	38	External device wake-up module, active low by default

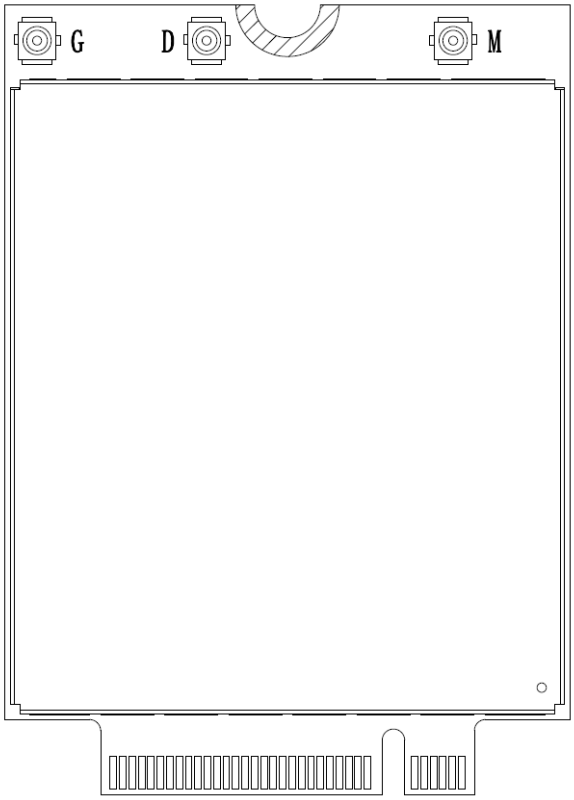
The module supports setting wake-up mode and waking up active level through AT commands. For details of configuration method, see
Fibocom_FM101-NA_AT Commands User Manual.

6. Radio Frequency

6.1. RF Interface

6.1.1. RF Interface Function

The FM101-CG module supports three RF connectors used for external antenna connection. As shown in the following figure, "M" refers to the RF main antenna for receiving and transmitting RF signals; "D" refers to the diversity antenna for receiving diversity RF signals; "G" refers to GNSS antenna.



6.1.2. RF Connector Performance

Rated Condition		Environmental Condition
Frequency range	Characteristic impedance	Temperature range
DC to 6 GHz	50Ω	–40℃ to +85℃

6.1.3. RF Connector Dimensions

FM101-CG module adopts standard M.2 module RF connectors, the model name is 818004607 from ECT company, and the connector dimensions are 2 mm × 2 mm × 0.6 mm, as shown in the following figure.

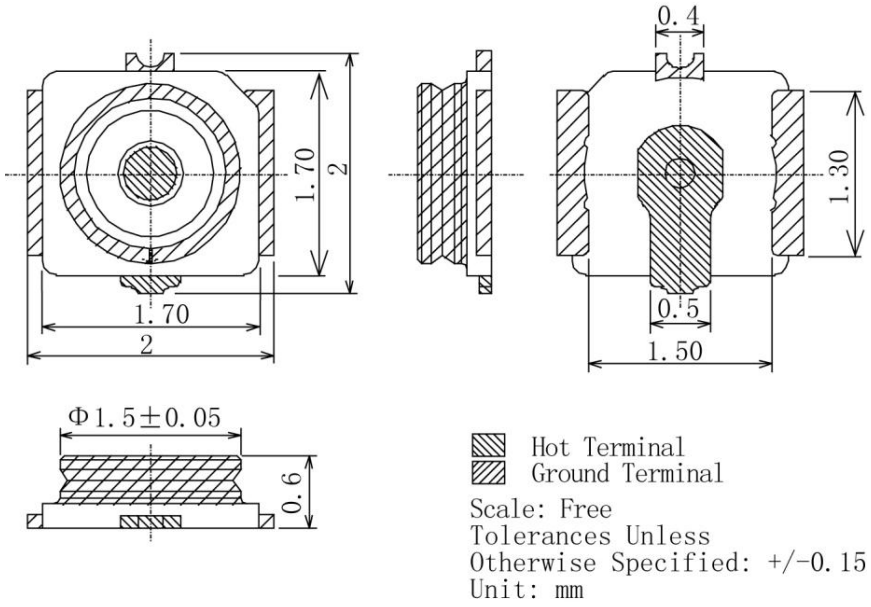


Figure 18. RF connector dimensions

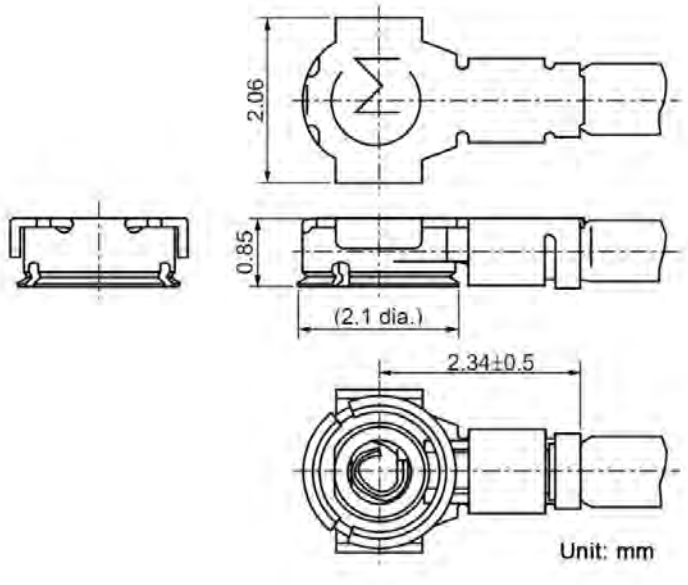


Figure 19. 0.81 mm coaxial cable matched RF connector dimensions

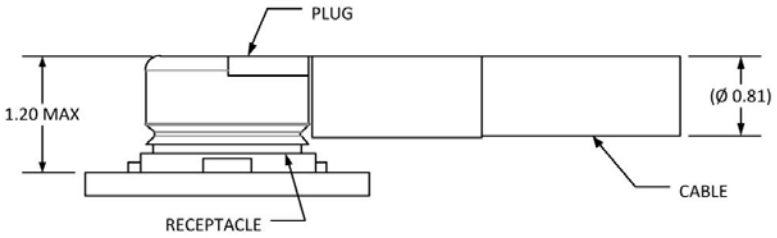


Figure 20. 0.81 mm coaxial cable snap-in RF connector dimensions

6.2. Operating Bands

Table 27. Operating bands

Band	Mode	Transmit (MHz)	Receive (MHz)
Band 42	LTE TDD	3400~3600	3400~3600
Band 43	LTE TDD	3600~3800	3600~3800
Band 48	LTE TDD	3550–3700	3550–3700

6.3. Transmitting Power

The following table describes the RF output power of FM101-CG module.

Table 28. Output power

Band	Minimum Value	Maximum Value
LTE TDD	< –40 dBm	23 dBm ± 2 dB

6.4. Receiving Sensitivity

Table 29. FM101-CG dual antenna receiving sensitivity

Mode	Band	Main Set Sensitivity Typ (dBm)	Diversity Sensitivity Typ (dBm)
LTE TDD	Band 42	-97	-98
	Band 43	-97	-98
	Band 48	-97	-98

6.5. GNSS Receiving Performance

The GNSS of FM101-CG module supports GPS/GLONASS/BDS/GALILEO, and the performance parameters of GNSS are shown in the following table.

Table 30. GNSS performance parameters

Indicator Performance	Description	Result	Unit
Sensitivity	Cold start	39	dB-Hz
	Acquisition	-145	dBm
	Tracking	-156	dBm
TTFF	Cold Start	40	s
	Warm Start	35	s
	Hot Start	3	s
Static Accuracy	Nominal accuracy	3	m

The above data is an average value obtained by testing some samples at 25°C.

6.6. Antenna Design

Antenna indicators

The antenna requirements for FM101-CG module are described in the following table.

Table 31. Module Antenna Requirements

FM101-CG module main antenna requirements	
LTE	VSWR: ≤ 2 Input power: > 28dBm Input impedance: 50Ω Antenna gain: < 3.6dBi Antenna isolation: > 25dB Antenna correlation coefficient: < 0.5
GNSS	Frequency range: 1559 MHz–1609 MHz Polarization direction: right-circular or linear polarization VSWR: < 2:1 Passive antenna gain: > 0dBi

6.7. PCB Routing Design

6.7.1. Routing Rules

For modules that don't have a RF connector, customers need to route a RF trace to connect to the antenna feeding point or connector. It is recommended to use a microstrip line. The shorter the better. The insertion loss should be controlled less than 0.2dB; and impedance should be controlled within 50Ω.

Add a π-type circuit (two parallel-component- grounded pins are connected directly to the main GND) between the module and antenna connector (or feeding point) for antenna debugging.

This signal line impedance is controlled within 50Ω during PCB cabling, and the RF

performance is closely related to this cabling. PCB parameters that will affect the cabling impedance include:

- Trace width and thickness
- Dielectric constant and thickness of media
- Thickness of pad
- Distance from ground line
- Nearby traces

6.7.2. Impedance Design

The RF impedance of the two antennas' interface should to be controlled within 50Ω.
In practical application, RF routing mode is designed according to other parameters of PCB, such as reference layer thickness, number of layers and stacking. Different reference GND layer will lead to different routing design.

6.7.3. 3W Principle

During antenna RF signal cabling design on PCB, the first thing you need to consider is to follow "3W principle".
In order to reduce crosstalk between the lines, please ensure that line spacing is large enough. If the line spacing is at least 3 times of the line width, 70% of the electric field between the lines will not interfere with each other, and this is called "3W principle".

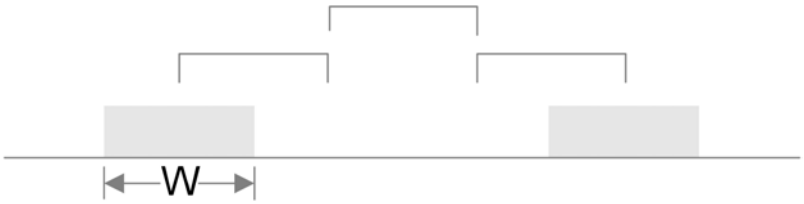


Figure 21. 3W principle

6.7.4. Impedance Design for Four-layer Board

The thickness of four-layer board is 1.0 mm. RF line is routed on Lay 1, and reference

layer is on Lay 2 (GND layer).

The stacking varies with PCB vendor, the following figure is taken as an example.

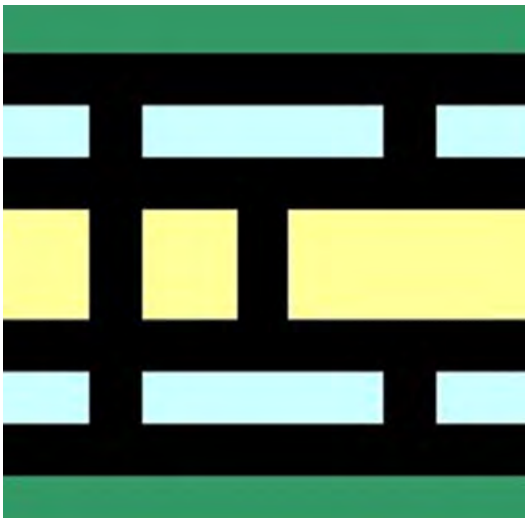


Figure 22. Four layers (1+2+1) thickness

Table 32. Four-layer board stacking thickness

Layer	Material	Thickness (um)
- -	Solder Mask	- -
Lay 1	0.33OZ+Plating	25
- -	PP 1080	65
Lay 2	0.5OZ+Plating	25
- -	0.510 mm (H/H OZ)	508
Lay 3	0.510 mm+Plating	25
- -	PP 1080	65
Lay 4	0.33OZ+Plating	25
- -	Solder Mask	- -

The thickness from Lay 1 to Lay 2 is 65 um, RF trace is 4 mil, and the distance from RF to GND is greater than 3 times of RF line width.

The blue area is Lay 1 and the red area is Lay 2, the highlighted part is RF line.

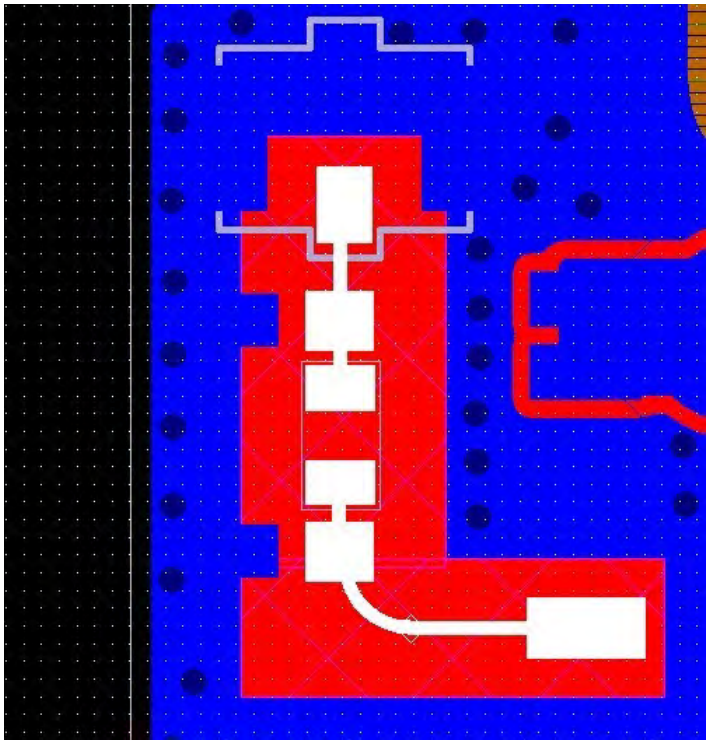


Figure 23. RF traces

50Ω impedance calculation:

If the value of D1 exceeds 3 times of W1, it has weak effect on impedance.

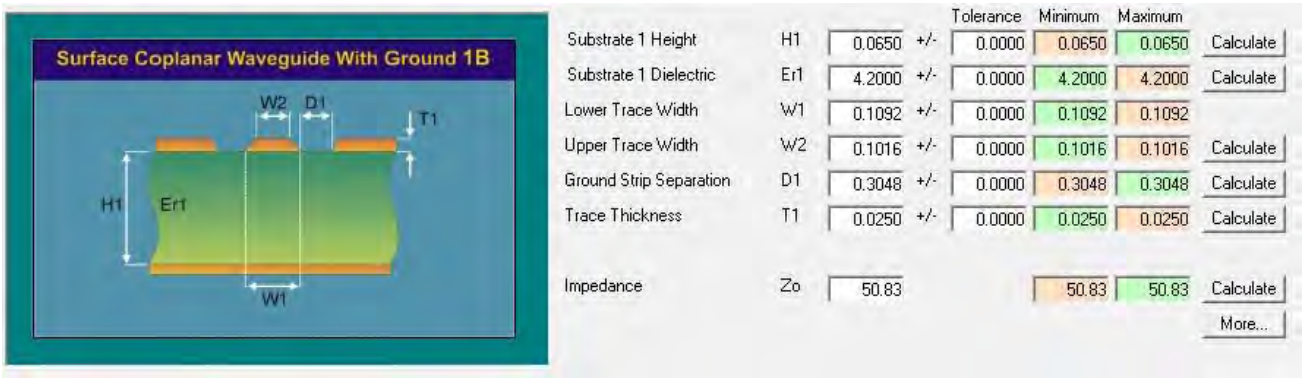


Figure 24. Impedance calculation for four-layer board top layer trace

6.8. Main Antenna Design

6.8.1. External Antenna

The external antenna has good performance. The antenna is placed outside the complete machine, the antenna space is large, and the antenna performance is not easy to be

affected by the internal environment of the complete machine, so that the antenna does not need to be independently designed for each project. The compatibility is good. Most of the interfaces of such antennas are SMA interfaces.

Figure 25. External antenna

6.8.2. Internal Antenna

6.8.2.1. Design Principle of Internal Antenna

Placement

- The antenna shall be arranged in the corners of the module.
- Avoid placing metal elements near the antenna.
- The shielding parts shall be as neat as possible. Do not use long strip shaped hole slots.
- Components with metal structure, such as horn, vibrator, and camera base plate shall be grounded.
- Avoid using long FPC. If a long FPC is required, add grounding shields on both sides.

Routing

- When connecting RF routing, apply circular arc treatment at the turning, take grounding and pay attention to characteristic impedance.

- RF ground shall be designed properly, PCB board and edge of ground shall be provided with "ground wall", and antenna led from RF module shall be made into microstrip line.
- The antenna RF feeding point pad is a round rectangular pad with the size of 2 mm × 3 mm. All layers of PCB that include the pad and surrounding and that are equal to and greater than 0.8 mm are not covered with copper.
- The center distance between RF and ground pad shall be between 4 mm and 5 mm.

6.8.2.2. Internal Antenna Classification

There are three kinds of internal antennas: PIFA, IFA and monopole. Internal antennas may form interference and other potential problems in the product, so there are more requirements in the design.
The following table describes the differences of these three types of antennas.

Table 33. Antenna differences

Antenna Type	Below Antenna Projection	Antenna Feed	Antenna Volume	Electrical Property	SAR
PIFA	Ground	2	Large	Very good	Low
MONOPOLE	No ground	1	Small	Good	Slightly high
IFA	Ground	2	Medium	About good	Medium

PIFA antenna

- Antenna structure

  There are two feeding points between the antenna and main board, one is module output, and the other is RF ground. It is recommended to design the antenna on the top of the device. The distance between the signal point and GND point should be at least 4 mm to 5 mm. The signal point and GND point can be put in different places, and more GND points mean more choices during antenna design.

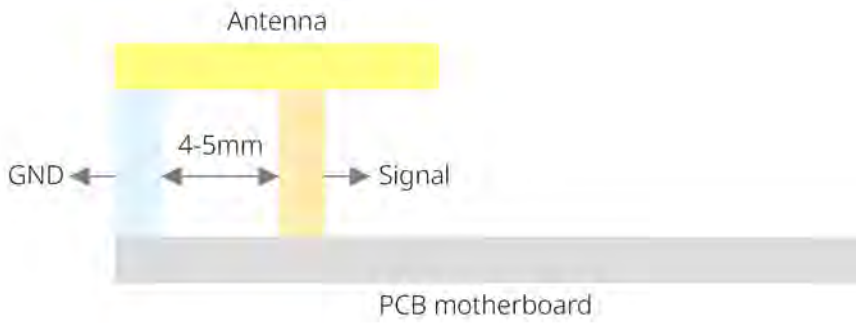


Figure 26. Location of the signal point and GND point of PIFA

- Main board

  There is complete paving in the antenna projection area. Do not place any component in the antenna area. The recommended length of PCB board should be 90 mm to 110 mm. The antenna performance is better if the board length is 105 mm.

- Structure of PIFA antenna

  - Bracket

    The antenna consists of plastic bracket and metal sheet (radiator). Plastic bracket and metal sheet are fixed by hot melt method. The plastic is made of BS or PC material, the metal sheet is beryllium copper, phosphor copper, or stainless steel. If you want to use FPC, add two pins in the main board, which boasts a higher cost.

  - Attached

    Attach the metal sheet (radiator) to the back cover of the module.

- Feed point of PIFA antenna

  The feeding point must be greater than 2mm × 3mm. Try to place it at the edge of the PCB board, and adopt round shape. Square with rounded corners is also preferred. The distance between feeding point pad and ground should be equal to or greater than 1mm.

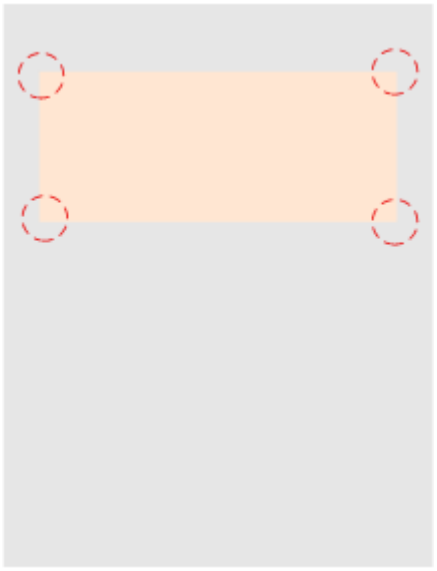


Figure 27. Pad design requirement

- Requirements on height and area

Operating Band	Height	Area
GSM/DCS	> 6mm	> 15mm × 40mm
GSM/DCS/PCS	> 6.5mm	> 17mm × 40mm
GSM850/GSM900/DCS1800/PCS1900	> 8mm	> 20mm × 45mm

For details about LTE antenna design, refer to the area requirement of GSM antenna.

Monopole antenna

- Antenna structure

  There is one feeding point between the antenna and main board, which is module output. It is recommended to design the antenna on the top of the device. The following figure shows the monopole antenna design.

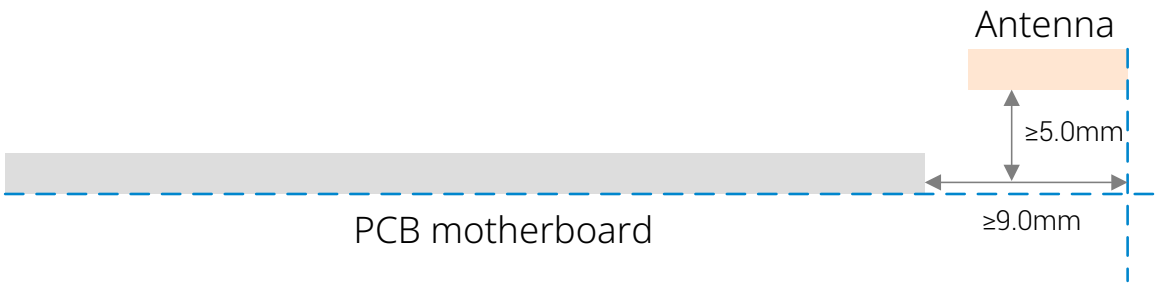


Figure 28. Antenna location

- Main board

  There should be no paving or PCB in the antenna projection area. Do not place any component in the antenna area. The recommended length of PCB board should be 80 mm to 100 mm. The antenna performance is improved if the board length is 95mm.

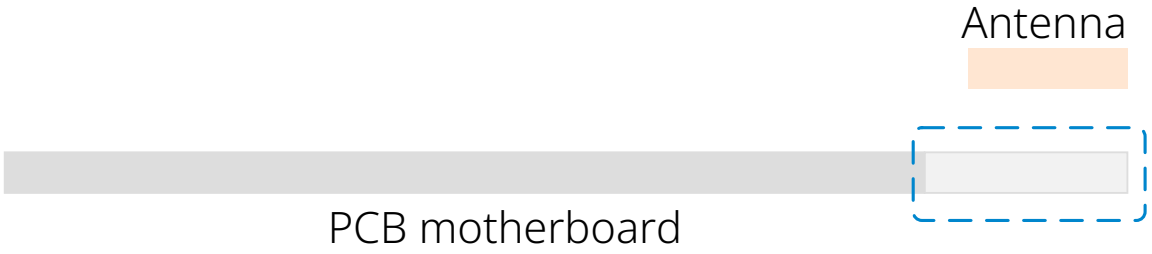


Figure 29. Requirements for antenna projection area

- Structure of monopole antenna

  For details, see Structure of PIFA antenna.

- Feed point of monopole antenna

  For details, see Feed point of PIFA antenna.

- The height and area requirements for monopole antenna are described in the following table.

Operating Band	Height	Area
GSM/DCS	> 5 mm	> 35 mm × 7 mm
GSM/DCS/PCS	> 6 mm	> 35 mm × 8 mm

Operating Band	Height	Area
GSM850/GSM900/DCS1800/PCS1900	> 6 mm	> 40 mm × 10 mm

For details about LTE antenna design, refer to the area requirement of GSM antenna.

IFA antenna

IFA antenna shares similarity with Monopole antenna and PIFA antenna. IFA antenna has two feeding branches, and allows ground under the antenna. The antenna has better stability than Monopole antenna, and the antenna space requirement is between Monopole antenna and PIFA antenna.

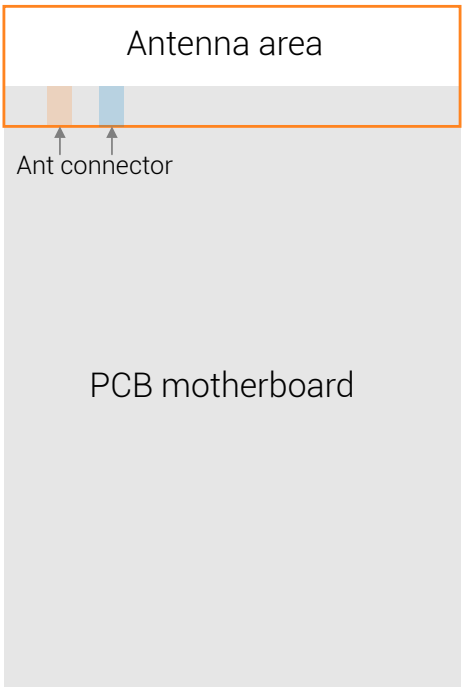


Figure 30. Location of signal point and GND point

Antenna space requirement: monopole < IFA < PIFA. For other requirements, refer to the PIFA and monopole requirements.

6.8.3. Surrounding Environment Design of Internal Antenna

6.8.3.1. Handling of Speaker

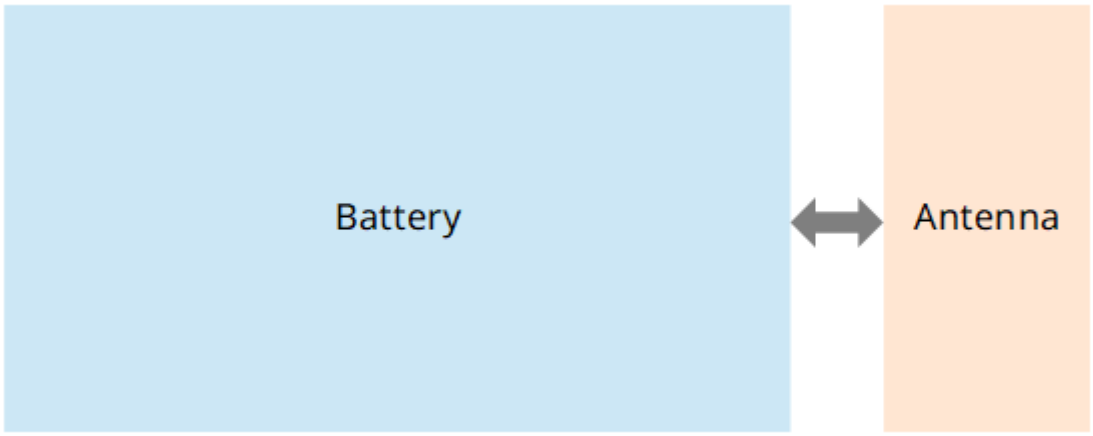
Connecting beads or inductors on speaker can reduce the impact on RF.

6.8.3.2. Handling of Metal Structural Parts

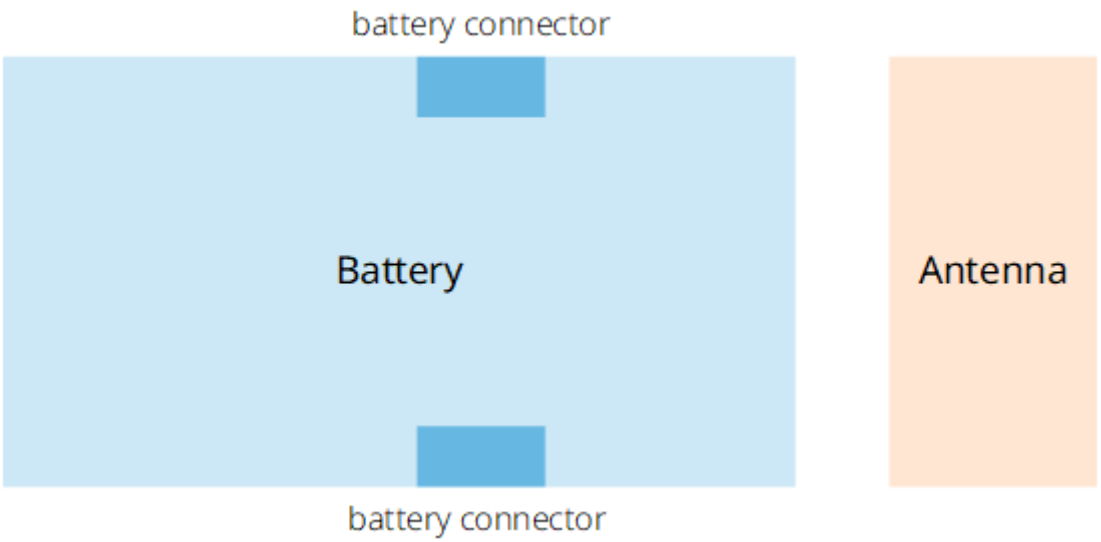
All the metal structural parts must be grounded correctly and reliably, and the circuit part must be shielded.

6.8.3.3. Handling of Battery

- The battery should be far away from antenna.



  - Monopole antenna: The distance between battery and antenna is equal to or greater than 5 mm.
  - PIFA antenna: The distance between battery and antenna is equal to or greater than 3 mm.
- Do not put the battery connector right beside the antenna.



6.8.3.4. Location of Large Components in Antenna Area

Do not place large metal components such as oscillator, speaker, and receiver around the antenna; they may greatly affect the electrical performance of antenna. Do not spray the cover of the antenna with conductive paint; be cautious when you use plating.

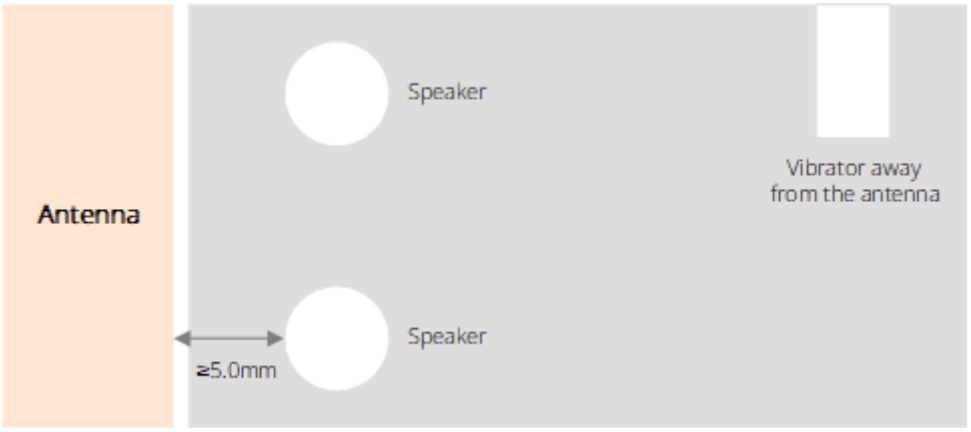


Figure 31. Location of large components

6.8.4. Common Problems of Internal Antenna Overall Design

Factors that would affect transmitting performance

- As the internal antenna is sensitive to the nearby medium, so the design of shell is closely related to antenna performance.

- Poor speaker layout will affect antenna performance.
- Poor battery layout will affect antenna performance.

Factors that would affect receiving performance

- If both the conductive performance of module and the radiated power of antenna meet requirement, then low sensitivity may be caused by main board design issue.
- Poor coupling sensitivity is caused by poor circuit design of LCD, LDO, and DC/DC.
- Device receiving performance is affected by VCXO or TVCXO harmonic of 19.2MHZ, 26MHZ, and 38.4MHZ systems.
- Poor coupling sensitivity is caused by SIM card clock.
- Poor FPC layout affects the receiving performance of the device.

Factors that would affect electromagnetic compatibility (EMC)

- Poor FPC layout affects EMC performance of the device.
- The metal element may absorb the antenna radiated power and produce a certain amount of secondary radiation, and coupling frequency is associated with the size of metal parts. Therefore, this kind of component should have a good grounding to eliminate or reduce secondary radiation.

6.9. Diversity and MIMO Antenna Design

- Diversity receiving technology is a main anti fading technology, which can greatly improve the transmission reliability in multipath fading channels. Its essence is to use two or more different methods to receive the same signal to overcome the fading and improve the receiving performance of the system.
- Diversity antenna can also multiplex different transmission paths in space using division multiplexing technology and receive data from the multiple different paths in parallel to improve the receiving throughput.
- The function of MIMO antenna is similar to that of diversity antenna, and they both

can resist against fading and improve throughput.

- The customer is recommended to design the corresponding antenna according to the antenna requirements of each module antenna port.
- The design method of diversity antenna and MIMO antenna is consistent with that of main antenna. It is recommended to control the difference of the efficiency of diversity antenna and MIMO antenna from that of main antenna by no more than 3dB.
- The isolation of each antenna shall be greater than 25dB, and the antenna correlation coefficient shall be less than 0.5. High isolation does not mean good correlation coefficient. Customers need to evaluate two indexes separately. The isolation and correlation coefficient of antenna generally depend on:
    - Antenna isolation
    - Antenna type
    - Antenna directivity

6.10. GNSS Antenna Design

The GNSS antenna can use a passive antenna or an active antenna. If the active antenna is used, the module supports the internal power supply to the active antenna, with the power supply voltage of 2.928V, and the power supply needs to be started with the AT command.

6.11. Other Interfaces

For the application of other interfaces, please refer to the recommended design. If the application scenario and the recommended design are not consistent, please contact FIBOCOM technicians for confirmation.

7. Thermal Design

FM101-CG module is designed to be workable on an extended temperature range, to make sure the module can work properly for a long time and achieve a better performance under extreme temperatures or extreme working conditions, such as high temperatures and high speed data transfer, it is required to add a exposed copper area at the corresponding motherboard position on the back of the FM101-CG module, and use a thermal conductive material to connect the module and the motherboard in this area to ensure that the heat of the module can be released through the motherboard. The following fogure shows the design.

Other measures to improve heat dissipation performance are as follows:

- Heat devices and other heat sources on the motherboard are as far away from the module as possible.
- The ground plane of the motherboard under the module is as complete as possible, and as many ground holes are drilled as possible to increase heat dissipation capability.
- Use screws to secure the module and motherboard to ensure good contact between the motherboard and the module.
- The use of heat sinks above the module is preferred, followed by the motherboard below the module.

8. Electrostatic Protection

Although the ESD problem has been considered and ESD protection has been completed in the FM101-CG module design, the ESD problem may also occur in transportation and secondary development. Developers should consider ESD protection in the final product. In addition to ESD in packaging, customers should consider the recommended circuit of the interface design in the document during module application.

The following table describes the ESD discharge range allowed by the FM101-CG module.

Table 34. Allowed ESD discharge range

Location	Air Discharge	Contact Discharge
VBAT, GND	±15 KV	±8 KV
Antenna interface	± 15 KV	± 8 KV
Other interfaces	± 2 KV	± 1 KV

9. Structural Specifications

9.1. Product Appearance

The appearance of the FM101-CG module is shown in the following figure.

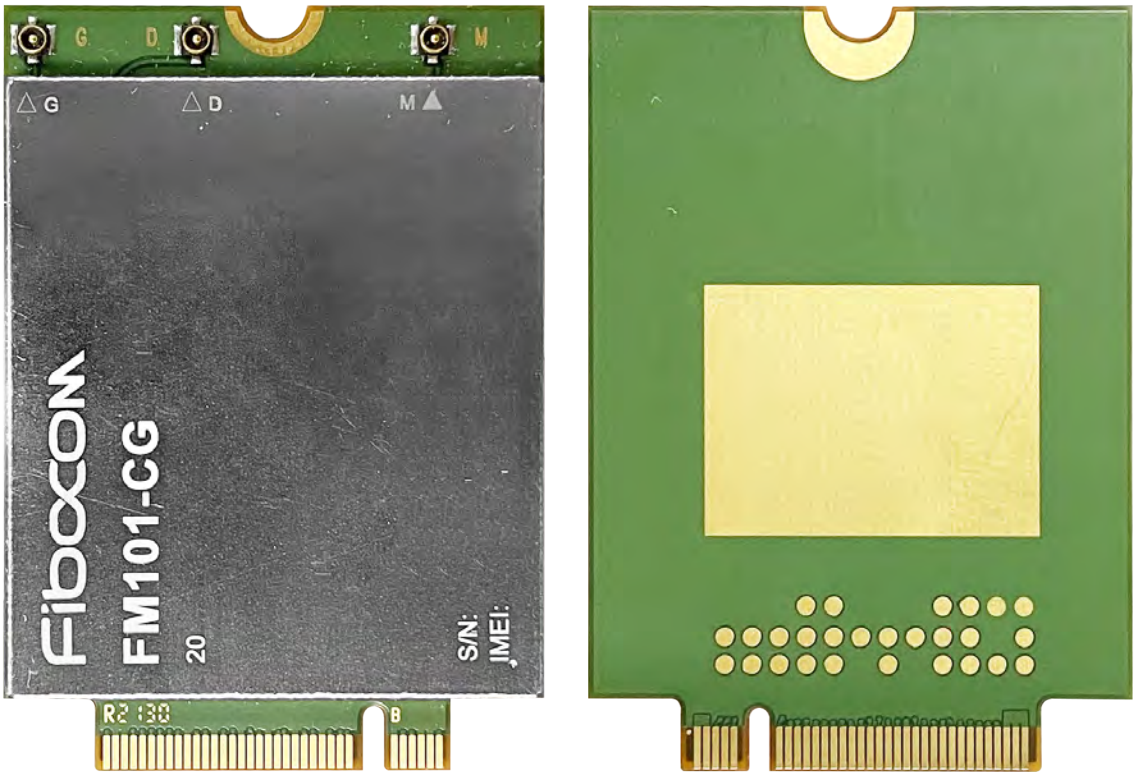


Figure 32. Product appearance

9.2. Structural Dimensions

The structural dimensions of the FM101-CG module is shown in the following figure. The unit is mm.

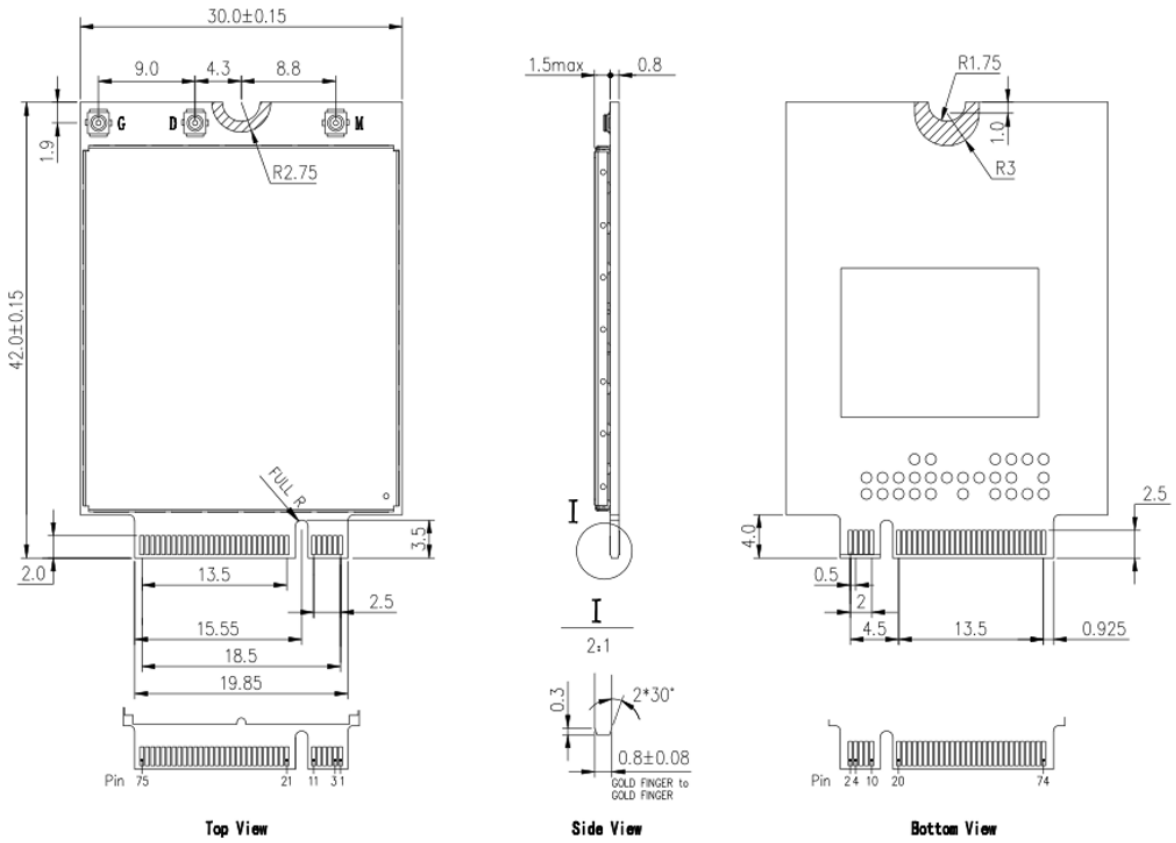


Figure 33. Structural dimensions

9.3. Package

The FM101-CG module uses the tray sealed packing, combined with the outer packing method using the hard cartoon box, so that the module can be protected to the greatest extent in the processes of storage, transportation and usage.

The module is a precision electronic product, and may suffer permanent damage if no correct electrostatic protection measures are taken.

Tray Package

The FM101-CG module uses tray package. 20 pcs are packed in one tray. 5 trays covering an empty tray on top are packed in one box. 5 boxes are packed in one case.

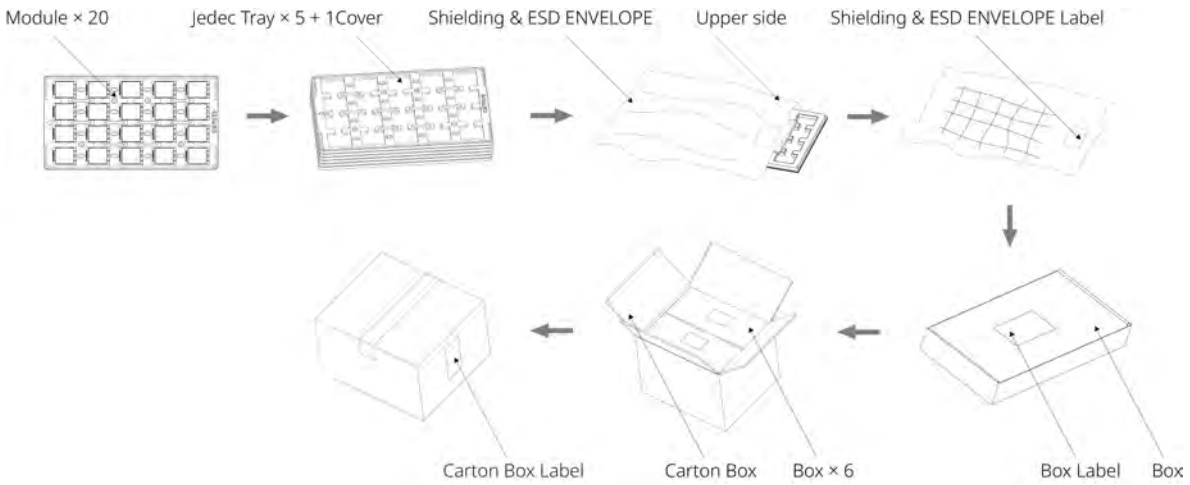


Figure 34. Tray package

Tray Size

The tray size of FM101-CG module is 330 mm × 175 mm × 6.5 mm, as shown in the following figure.

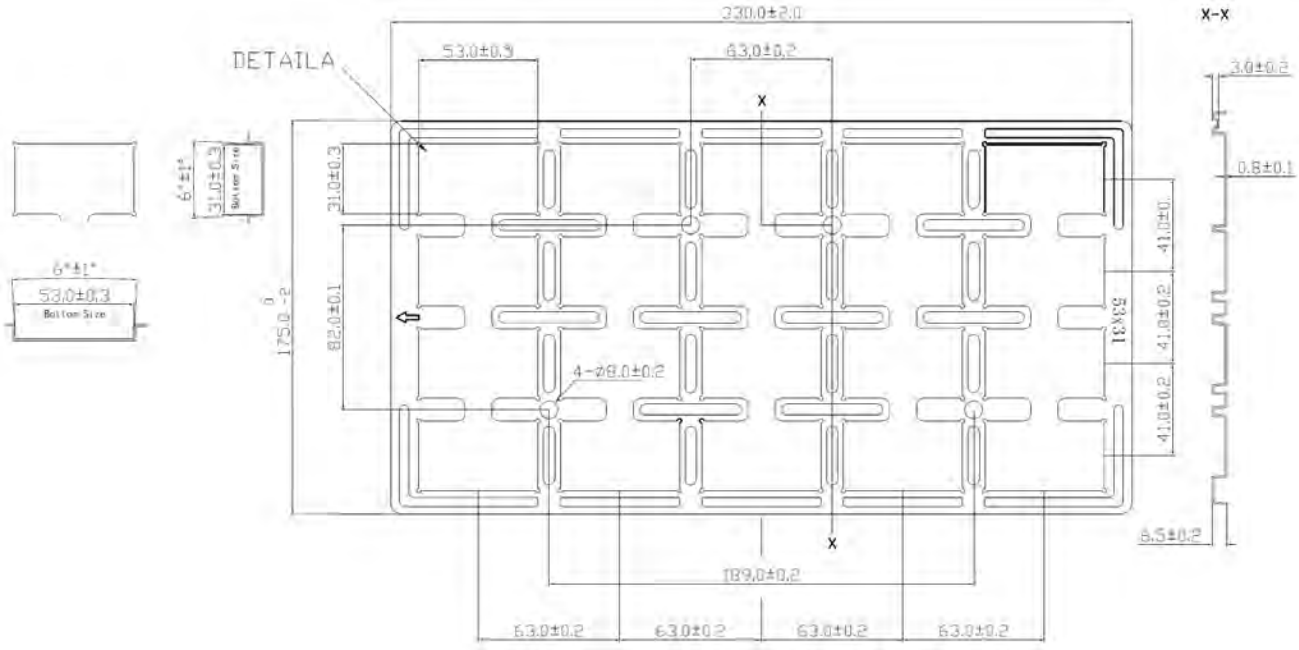


Figure 35. Tray size (unit: mm)

9.4. Storage

Storage conditions (recommended): The temperature is 23℃ ± 5℃, and the relative humidity is less than RH 60%.

Storage period: Under the recommended storage conditions, the storage life is 12 months.

Appendix A: Acronyms and Abbreviations

bps	Bits Per Second
CA	Carrier Aggregation
DLCA	Downlink Carrier Aggregation
DRX	Discontinuous Reception
Imax	Maximum Load Current
LED	Light Emitting Diode
LTE	Long Term Evolution
ME	Mobile Equipment
MS	Mobile Station
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
RF	Radio Frequency
RMS	Root Mean Square
RTC	Real Time Clock

Rx	Receive
SMS	Short Message Service
TE	Terminal Equipment
TX	Transmitting Direction
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value

VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio

OEM/Integrators Installation Manual

Important Notice to OEM integrators 1. This module is limited to OEM installation ONLY. 2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b). 3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations 4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting, and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Fibocom that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: ZMOFM101CG” . The FCC ID can be used only when all FCC compliance requirements are met.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, part 96 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.