Flexible 2D Layout Decomposition Framework for Spacer-Type Double Pattering Lithography

Yongchan Ban, Kevin Lucas* and David Pan
Department of ECE, The University of Texas at Austin, Austin, TX USA
*Synopsys Inc., Austin, TX USA
ycban@cerc.utexas.edu, kevin.lucas@synopsys.com, dpan@ece.utexas.edu

ABSTRACT

A spacer-type self-aligned double pattering (SADP) is a pitch-splitting sidewall image method that is a major option for sub-30nm device node manufacturing due to its lower overlay sensitivity and better process window compared to other double patterning processes, such as litho-etch-litho-etch (LELE). SADP is in production use for 1D patterns in NAND Flash memory applications but applying SADP to 2D random logic patterns is challenging. In this paper, we describe the first layout decomposition methods of SADP lithography for complex 2D layouts. The favored type of SADP for complex logic interconnects is a two mask approach using a core (mandrel) mask and a trim mask. This paper describes methods for automatically choosing and optimizing the manufacturability of base core mask patterns, generating assist core patterns, and optimizing trim mask patterns to accomplish high quality layout decomposition in SADP process. We evaluate our technique on 22nm node industrial standard cells and logic designs. Experimental results show that our proposed layout decomposition for SADP effectively decomposes many challenging 2D layouts.

Categories and Subject Descriptors

B.7.2 [**Hardware, Integrated Circuit**]: Design Aids

General Terms

Algorithms, Design, Performance

Keywords

Double patterning, SADP, Decomposition, Lithography, DFM

1. INTRODUCTION

Double patterning technique (DPT) with traditional ArF lithography tools has been a promising alternative of a layout patterning for sub-30nm nodes. The main idea of DPT is to decompose a single layout into two masks in order to increase pitch size and improve process tolerance of focus and dose variations [1–4]. DPT largely consists of two types: a litho-etch-litho-etch (LELE) double patterning and a spacer type self-aligned double patterning (SADP). LELE has two lithography steps with one or two etch steps after decomposing the target mask layout into two mask layouts [3–6]. As shown in Figure 1, some polygons should be split into two or more polygons to resolve layout decomposition conflicts, which will introduce *'stitch'* points.

DAC'11, June 5-10, 2011, San Diego, California, USA

The critical limitation of LELE is the inevitable overlay error between the two sequential exposure steps. The mask placement, alignment and magnification errors on the second mask exposure might induce patterning variation which directly causes significant performance and yield degradation [7–9]. In addition, a stitch can be regarded as a line-end which is highly sensitive to lithography process variation and is prone to line-end shortening, CD shrinking, etc [3,6].

SADP is a pitch-splitting sidewall image method that also utilizes two masks: a *core* mask and a *trim* mask. The core mask defines core mandrel patterns, and the sidewall spacer is deposited onto all sides of a mandrel pattern to enable pitch doubling in the patterning. The trim mask removes unnecessary patterns by blocking or unblocking with photoresist (PR). Since the most critical patterning control in SADP is not governed by lithography, but by the deposition of the sidewall spacer, it has less overlay error (less than 3nm in SADP vs. more than 6nm in LELE) and excellent variability control compared to LELE [9,10].

However, SADP allows only a single width of sidewall spacer which forms either a single wire width or a single wire space. Therefore, SADP was previously limited by the lack of flexibility in terms of layout decomposition. Thus, SADP is only in production use for 1D patterns in NAND Flash memory applications but applying SADP to 2D random logic patterns is challenging [1,10,11]. Due to its limitation, SADP might require three mask for 2D-type application. Since the manufacturing cost of logic products is dominated by the patterning cost, a two-mask SADP approach is necessary for successful product application. Thus, layout decomposition for random 2D logic features, which have various wire widths and spaces, is a primary challenging issue for a manufacturable SADP process.

In this paper, we propose rigorous layout decomposition methods on SADP technique for sub-30nm random shaped metal layouts. The major contributions of this paper include the following:

- This paper, to our best knowledge, develops the first systematic framework SADP layout decomposition for 2D layout structures.
- The layout coloring is a crucial step in SADP decomposition. Despite not any stitches, we can resolve coloring conflicts with the proposed approaches. Moreover, we propose mask friendly coloring methods for the best manufacturability.
- We can make random 2D patterns by introducing layout regargeting rule and assist mandrel at the first core mask which can be generated in a lithography friendly manner.

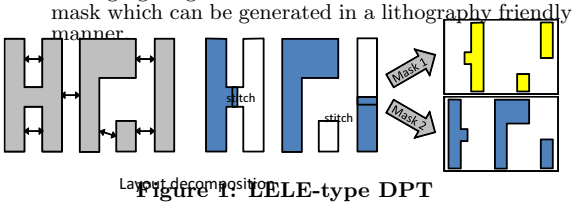


Figure 1: LELE-type DPT

The rest of the paper is organized as follows. Section 2 describes SADP lithography process and the challenging issues. Section 3 presents several layout coloring approaches for DRC-free decomposed mast layouts. Section 4 proposes algorithms of the core mask generation. Experimental results are discussed in Section 5, followed by conclusions in Section 6.

2. SPACER-TYPE DOUBLE PATTERNING

We first introduce some terminologies and notations which are used throughout this paper:

- *Core mask*: the first mask in the SADP process flow.
- *Mandrel ($M_\forall$)*: the printed patterns generated by the core mask where the sidewall spacers are subsequently formed. It is used as a synonym for core mask.
- *Main mandrel (M_m)*: the base mandrel layout which is a chosen subset of the original design intent.
- *Assist mandrel (M_a)*: the extra mandrel layout newly generated, i.e., assist features.
- *Secondary pattern (P_s)*: the pattern except the main mandrel in the original layout.
- *Spacer (S_p)*: the sidewall spacer, which is deposited on the mandrel, is formed at the both sides of mandrels.
- *Trim mask (T_m)*: the second mask in the SADP flow, which is used for removing unnecessary patterns.

A favored type of SADP is SID-type SADP due to its more cost effective patterning where SID is an abbreviation of "spacer is dielectric" [1, 10]. Figure 2 shows a flow of SID SADP. The first core mask layout is chosen from the original layout in (2). Then, the sidewall spacers are generated nearby the mandrel layout in (3). After removing mandrels, we deposit substrate materials (purple in (4)). Then, the second trimming mask is used for getting the final patterns in (4). Since the main mandrel layout in (2) becomes final patterns, SID-type SADP enables various metal widths.

Like conventional LELE, SID SADP uses two mask steps: a core mask and a trim mask. Since the main mandrel layout is a subset of the original design intent, a layout coloring technique can be used for decomposing dense target patterns [3–6]. The two-color mapping for SADP is less intuitive but similar to LELE. The two mask layouts of LELE correspond to main mandrel and secondary pattern of SADP, yet SADP requires a core mask and a trim mask for patterning.

In Figure 2, one can see an assist mandrel layout which is added on the main mandrel and will not be printed on wafer to eventually make the secondary pattern ('*not mandrel*') using a trim mask. By applying layout coloring, one color can become the main mandrel. The selection of main mandrel color affects the shapes of the assist mandrel layouts. In random 2D layout application, inserting assist mandrel polygons is an essential part because those allow various wire widths and various pattern shapes in SADP layout decomposition. Therefore, one can make random 2D shape patterns by building assist mandrel layouts.

However, a major drawback of SADP is the fact that features in SADP does not allow any stitch points as in LELE. It means that splitting a polygon into two or more polygons can not be considered in SADP. Thus, one polygon should have one particular color. The reason is that the selected mandrel will make spacer patterns which will be etched out after the trim mask patterning. The spacer acts like a layout separator among main mandrels and secondary patterns. Thus, if we split a polygon into two polygons and select one

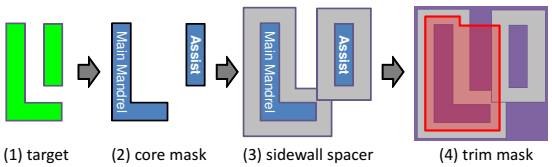


Figure 2: A 2D flow of SID-type SADP

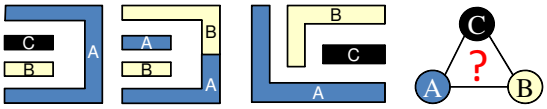


Figure 3: Coloring conflict in layout decomposition

polygon as a main mandrel, it would result in disconnecting the final patterning results due to spacer blocks.

Even though stitching can have side effects such as yield loss due to mask overlay, a stitch insertion gives a decomposition flexibility in LELE. Without stitch insertion, some coloring conflict is usual in a random 2D layout. Figure 3 shows some cases of coloring conflict. By inserting a stitch point in LELE DPT, the coloring conflict can be resolved as in (1). Not all the conflicts can be resolved by inserting stitches even in LELE. The undecomposable conflict in (2) is called an inherent or native conflict [6, 12]. Since SADP does not allow any stitch insertion, both (1) and (2) in Figure 3 can be regarded as native conflict cases. Therefore, resolving coloring conflicts is another critical step in SID SADP process for random 2D layouts.

There are many challenges involved with creating a core mandrel mask and a trim mask for complex 2D layouts. In particular, layout coloring and assist mandrel generation are of utmost important steps in an SADP mask synthesis process:

Layout Coloring Since the main mandrel is chosen from the design intent after assigning a color mapping, the manufacturability on both core mask and trim mask is significantly dependant on layout coloring. A core mask layout can be easily generated from the main mandrel, yet the trim mask layout is relatively less intuitive. Moreover, since SADP does not allow any stitch insertion, it is crucial to resolve any odd-cycle coloring conflicts in SADP layout decomposition.

Assist Mandrel Assist mandrel gives SADP more flexibility which allows to make random shaped layout. Thus, it requires an intelligently designed mandrel layouts as a good starting point. Since the first core mask is usually more complex than the trim mask, it highly affects a lithographic printability on wafer. Thus, a lithographic friendly mandrel generation is necessary for less process variation.

3. MASK AWARE LAYOUT COLORING

3.1 Problem Formulation

Given: In a given layout L, let $F = \{f_i | 1 \leq i \leq n\}$ be a set of polygon features and $E = \{e_j | 1 \leq j \leq m\}$ be a set of edge segment in a feature f_i, d be the minimum coloring distance between two polygon features.

Find: To minimize the sum of connections among polygons on a layout.

Subject to: (1) A connection weight in a feature f_i is the sum of the assigned weights of all edges e_j, (2) A positive connection between two polygons encourages placement on opposite color. (3) A negative weight encourages placement on the same color.

Even in a polygon, every branch of a polygon might have different neighboring layout connection. By calculating connection weight on edge segments instead of on every polygon node [4, 6, 12], we can consider the layout connection constraint. Reasons that we use an edge segment based coloring are as follows:

- SADP mask decomposition does not allow '*stitch*' points. Every polygon should have a single color without division. Thus, we should more accurately calculate connection weights in a layout. Edge segments can consider every local layout constraints for SADP mask decomposition.
- In SID-type SADP, the 1^{st} core mask layout is decided from target polygons, meanwhile the shape of the 2^{nd}

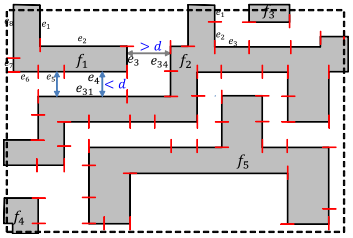


Figure 4: Edge segment based layout coloring

trim mask layout is highly related to layout spaces between two polygons (refer to the Section 3.2). Edge segments of polygons provides better layout information for the trim mask.

Figure 4 shows a color assignment based on an edge segment approach. The first step is to divide every edge of polygons into multiple segments based on the polygon itself and neighboring polygons, that is a similar way of layout segment of a conventional model-based OPC. Then, each edge in a polygon calculates the connection weight. For example, in Figure 4, the distance between an edge e_4 of a feature f_1 and an edge e_{31} of a feature f_2 is less than the minimum coloring distance d. Thus the edges e_4 and e_{31} have positive weight. Whereas, since the space of an edge e_3 of a feature f_1 is larger than d, no weight value is given. The connection weight of a polygon can be the sum of connection weights of all edge. Our overall layout coloring for SID-type SADP is given in Algorithm 1.

Algorithm 1 Mask aware layout coloring

```
1: Dummy Layer Insertion in Section 3.5
2: A set of polygon features F in a layer
3: Find self-conflict areas in Section 3.4
4: A set of self-conflict area S in a layer
5: for each polygon f ∈ F do
6:    Weight_f ← 0
7:    Decompose segments E ∈ f
8:    for each segment e ∈ E do
9:       weight_e ← 0
10:      detect conflict c with min. distance d
11:      if c < d then
12:         determine whether conflicted layout ∈ S or not
13:         update weight_e, shortest-path coloring in Section 3.3
14:      end if
15:      Weight_f += weight_e
16:   end for
17: end for
18: assign a color for polygons with sparse matrix solver
19: check grouping in Section 3.2
```

3.2 Grouping and Merging Coloring

Since SADP mask decomposition does not allow stitch insertion, some coloring conflict is usual. As shown in Figure 5, the target design has a native coloring conflict which represents an undecomposable layout even in LELE [4, 12]. To resolve this coloring conflict, we introduce a grouping and merging algorithm. Once two same colored polygons are within the minimum coloring distance d, we make a group for the polygons and merge them into one polygon. By merging the two conflicted polygons, we can make a core mask without any DRC and lithography violation. This merged region between two grouped polygons should be trimmed out at the 2^{nd} trim mask patterning step.

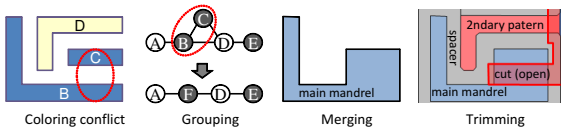


Figure 5: Grouping and merging coloring

Note that since the spacer patterns nearby mandrels will become dielectric after the trim mask patterning, the spacer acts like an overlay-free region. It implies that if the edge of a trim mask layout is on the spacer region, the trim layout can be free from mask overlay variations without any impact on target metal lines. In the other words, we should carefully control the mask overlay if the trim mask edge is on metal lines.

Thus, we should note the following issues if a trim mask should cut the merged area:

- The width of a trim mask should meet the trim mask width constraint which is usually the same as the minimum target layout width or slightly larger.
- Since the edge of a trim mask layout is passing over the main mandrel not the safe spacer region, the overlay error of the trim mask should be carefully controlled.

3.3 Shortest-path Coloring

After merging two conflicted polygons into one polygon, the trim mask should remove the merged region at the cost of mask overlay. Therefore, shorter trim mask for removing merged region is preferable for smaller overlay impact on the 2^{nd} patterning. So, in addition to a grouping and merge coloring, we propose a shortest-path coloring as shown in Figure 6. The shortest-path coloring is achieved by reflecting the length of an edge segment when we assign a connection weight on an edge. In Figure 6, the region between polygon A and B has a longer interacting length of coloring conflict. Meanwhile, between polygon A and C has the shortest interacting length. The interacting length is multiplied by the interacting weight for both two polygons. Thus, the polygons having smaller interacting length have less interacting weight for coloring that makes the shortest interacting polygons having the same color.

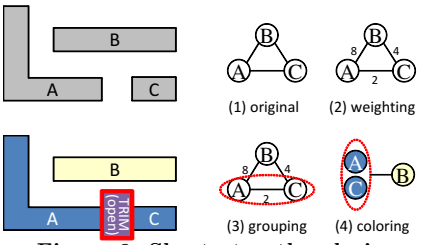


Figure 6: Shortest-path coloring

3.4 Self-conflict Aware Coloring

Even though we assign the same color on the polygons which have less polygon interference, the corresponding trim mask might have internal DRC errors on the mask itself because the trim mask should meet single patterning constraints as shown in Figure 7. In order to avoid this self-conflict violation, we identify self-conflict regions of the trim mask and put more interacting weight in layout coloring. The self-conflict region on a trim mask usually happens when three or more consecutive polygons have the same color where the width of middle polygon is less than the trim mask space constraint. We can detect the trim self-conflict

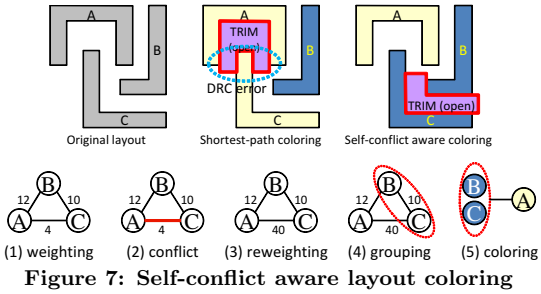


Figure 7: Self-conflict aware layout coloring

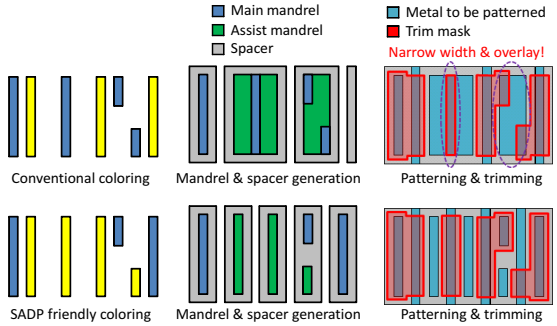


Figure 8: Trim mask friendly coloring

region by twice checking the minimum space of the layout. By putting more connecting weight on the self-conflict region, we can avoid the internal DRC error on the trim mask.

3.5 Trim Mask Friendly Coloring

Since the sidewall spacer can be placed between two abutting metal polygons, it can exactly identify the edge position of different metal lines. It implies that the sidewall spacer prevents abutting metal lines from patterning faults, in particular, bridging fault. Moreover, it can give the trim mask more process tolerance. As shown in Figure 8, a conventional layout coloring might give smaller patterning margin, e.g., narrower trim width or width violation. In addition, the trim mask is prone to mask overlay. Where possible, *the best coloring for SID-type SADP is to assign a different color on polygons in every other layout pitch track.*

To assign the best coloring on the layout, we insert dummy layouts between two metal lines as shown in Figure 9. Once we put dummy metals into vacant areas, we assign two-map layout color with the shortest-path coloring and the self-conflict aware coloring approaches. After removing the dummy metals, we can get the trim mask friendly layout coloring for SID-type SADP process.

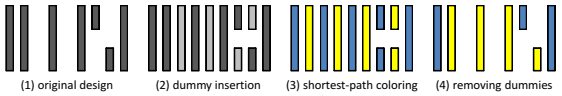


Figure 9: Dummy insertion for trim-aware coloring

4. LITHO. FRIENDLY MANDREL

4.1 Problem Formulation

Given: Let M_m be the main mandrel, P_s be the secondary patterns, L_m be the minimum mandrel width at wafer, L_s be the minimum spacer width at wafer, and L_b be the mask bias for the 1^{st} pattering.
Find: Find the assist mandrel, M_a, to make secondary patterns, P_s, at the final patterning by merging the sidewall spacer patterns, S_p near the core mandrel, $M_\forall$.
Subject to: (1) no DRC error is allowed between positively biased (increased) $M_\forall$ (M_m and M_a) as much as L_b on the 1^{st} core mask. (2) DRC error is allow between M_as itself because M_a will be removed at the 2^{nd} trim mask step.

Figure 10 illustrates a way to generate assist mandrel patterns in addition to the main mandrel. The goal of the assist

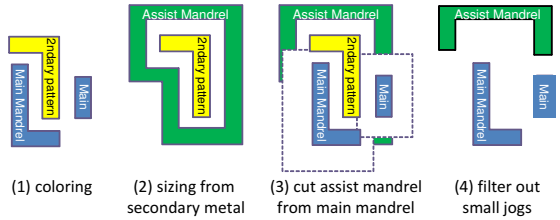


Figure 10: Generation of assist mandrel

Algorithm 2 Lithography friendly mandrel generation

Require: A set of colored layer L
1: Select M_m and P_s from L: # either color is allowed.
2: # initial M_a in Section 4.2
3: **if** longer **then**
4: $M_{af} \leftarrow$ all direction expanding from P_s
5: **else if** shorter **then**
6: $M_{af} \leftarrow$ edge expanding from P_s
7: **else if** directional **then**
8: $M_{af} \leftarrow$ edge expanding from P_s
9: remove small island patterns from M_{af}
10: **end if**
11: # cut M_{af}
12: $C_m \leftarrow$ expanding M_m as much as $L_s + 2L_b$
13: $M_a \leftarrow M_{af}$ - C_m
14: # post-processing of M_a in Section 4.3
15: **for** each small features $f \in M_a$ **do**
16: M_a merging or removal for manufacturability
17: define mandatory trim areas
18: **end for**
19: Metal retargeting in Section 4.4
20: DRC check with mask biasing, L_b

mandrel, M_a, is to make secondary patterns, P_s, by merging neighboring spacer S_p of nearby Mandrel, $M_\forall$. There should be spacer patterns next to every secondary metals P_s. Since $M_\forall$ makes S_p which also generates P_s, in an intuitive way we can make M_a in every neighboring P_s as much as L_s away. Meanwhile as M_m also generates S_p patterns, we can filter out overlapped M_a which lies on the interacting region of M_m within the distance $(L_s + 2L_b)$.

Algorithm 2 also shows a flow of our mandrel generation for 2D random layout. The assist mandrel is formed in a way of manufacturing requirements and usually made using polygon extending and boolean operation in line 2-10. After making additional mandrel patterns, we cut some overlapped region with the main mandrel in line 11-13. Once some small jogs and spaces in the additional mandrel are modified with a manner of manufacturing friendly in line 14-18, we adjust the final metal pattern with a metal retargeting rule in line 19.

4.2 Litho. Friendly Assist Mandrel

Figure 11 shows the final core mask layout ($M_m + M_a$) in different ways. We can generate assist mandrel patterns for 2D random layouts with different options, for example *the shorter* M_a, *the longer* M_a, and *the directional* M_a. The shorter M_a approach builds M_a polygons just at the area facing with the secondary metal, P_s. This approach induces lots of small island patterns. Some small patterns in the core mask are prone to be collapsed due to photoresist (PR) tension or moved away due to lithography proximity. Thus, one can also use the longer M_a approach which generate M_a patterns covering all surrounding areas of P_s.

Another option is the directional M_a approach which makes M_a by considering lithography illumination. Off-axis illumination (OAI) is a widely used for better lithographic printability. An oblique illumination improves patterning resolution of those features toward the illumination direction [13]. It directly implies that a single directional metal layout is desirable for lithography patterning. Thus, in the direc-

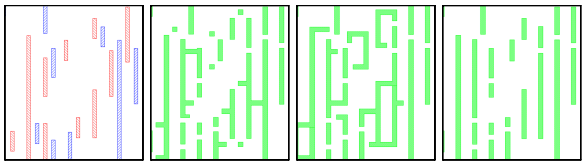
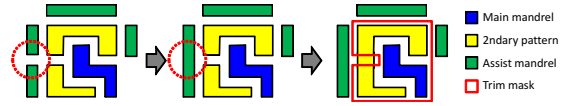


Figure 11: Lithography friendly assist mandrel: where blue layout in (a) becomes main mandrel.

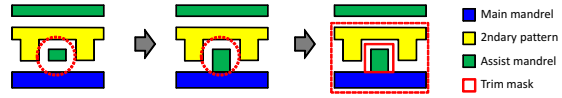
tional M_a approach we generate M_a at the area which has the same direction with the metal lines. This approach is similar to the shorter M_a approach at the first stage, yet by removing a small island, which is usually located at the metal line-end, we can achieve directional M_a polygons.

4.3 Assist Mandrel Post-processing

If the space among M_as is smaller than a certain constraint, we can fill a space and make a polygon by connecting M_as in order not to violate mask rule in the core mask. Once we connect between two M_as, the corresponding P_s might be also connected. Thus, the connected region at P_s should be removed at the 2^{nd} trim mask step (Figure 12(a)). In a similar way, if small pieces of M_a are conflicting with M_m, we can merge them into M_m or remove them. When small M_a is merged into M_m, both the merge area and small M_a should be cut at the trim mask, which might be an overlay burden to M_m. Meanwhile, when small M_a is removed, P_s region might be extended, thus it should be removed, which might give an overlay burden to P_s (Figure 12(b)).



(a) mandrel filling



(b) merging with main mandrel or removing

Figure 12: Options of assist mandrel polygons

4.4 Layout Retargeting for SADP

Since the width of a sidewall spacer is usually constant, in order to apply SADP process to 2D random logic, design retargeting may be necessary. A design retarget means to slightly modify the design intent in layout, and it usually induces a slight increase of a metal width in SID-type SADP. Slightly increased (thicker) metal lines are an improvement due to the following reasons:

- The thicker metal line is better for timing issues, in particular delay. Despite a small increase of coupling capacitance, a resistance decrease is more favorable for metal delay.
- It is even better for lithography patterning. Thicker metal lines have more tolerance due to lithography process for sub-30nm patterning.

Therefore, we define a forbidden space for layout retargeting between the two colored layouts, in particular, the main mandrel and the secondary metal. As shown in Figure 13, let S_{fbdn} be the forbidden space for SID-type SADP process, S_{trm} be the minimum allowable space of the trim mask, W_{mgn} be the trim mask overlay margin for the design intent, W_{spr} be the sidewall spacer width, and W_{rtg} be the width of the allowable retargeting. The forbidden space in SID-type SADP is as follows:

$$W_{spr} < S_{fbdn} < S_{trm} \quad (1)$$

Thus, if the S_{trm} is same as the W_{spr}, no forbidden space exists in an SADP mask decomposition. Since, W_{spr} and W_{mgn} are fixed in SADP lithography process, the maximum retargeting width of the design intent, W_{rtg}, is defined as follows:

$$W_{rtg} = S_{fbdn} - (W_{spr} - W_{mgn}) \quad (2)$$

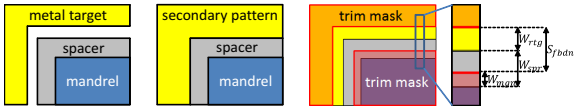


Figure 13: Metal retargeting rule

By introducing the maximal allowable retargeting width at the trim mask, we can have more flexibility on layout decomposition and lithography manufacturing in SID SADP.

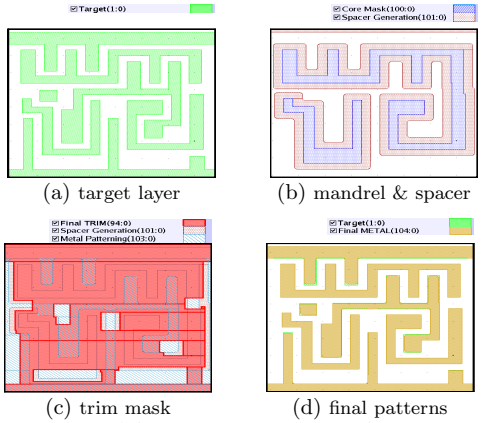
5. EXPERIMENTAL RESULTS

We implemented a mask decomposition automation for SID-type SADP process and tested with metal layers of industrial 22nm node standard cells and 22nm node logic devices. First, the minimum width, space, and sidewall spacer of 22nm node standard cells are all 34nm. The etch bias per edge for mandrels is 8nm which means the minimum width of the core mask for the 1^{st} lithography patterning is 50nm (34nm+2×8nm). The minimum space of the core mask layout and the minimum width and space of the trim mask layout are all 50nm. The overlay margin of between the trim mask and the design intent is 5nm in our experiments.

Figure 14 shows the results of our SADP decomposition for 22nm node standard cells which are already finished with their placement and routing design. As shown in Figure 14(a), the layout has multiple widths and spaces, and moreover the shape of the layout looks arbitrary so that the mask decomposition for SADP process is challenging. Based on our layout coloring for SADP decomposition, we select the main mandrel by considering the trim mask layout and define the assist mandrel layout in Figure 14(b). After making the core layout without any DRC violations, we shrink the core layout with the following etch step, and than generate the sidewall spacer pattern nearby the mandrel in (b). The trim mask patterning is followed by the BARC deposition in (c), then we can get the final patterning after some etch process in (d). As Figure 14(d) shows, the final metal pattern meets the target design with slightly thicker patterns due to the retargeting rule.

We also tested our SADP layout decomposition for the industrial 22nm node full-chip logic metal layer. Eight layout blocks which have the same area (20um×20um) are evaluated. The minimum width and space of the layout are 35nm and 45nm, respectively. The width of a sidewall spacer is 45nm, and the etch bias per edge for mandrels and the overlay margin of the trim mask are all 5nm. The minimum width and space of the trim mask are 45nm and 55nm, respectively. We used a commercial tool for model based OPC and lithography simulation. Our optical parameters are wavelength = 193nm, numerical aperture (NA) = 1.25 immersion, and dipole illumination σ = 0.85/0.55. Following industrial practice, we first performed full OPC for all mask layouts and ran lithography simulation with a process variation: focus = ±50nm.

Table 1 shows the number of DRC errors both on core mask and trim mask with the different layout coloring approaches: the edge segment based coloring ($EDGE$) in Fig-



(a) target layer (b) mandrel & spacer

(c) trim mask (d) final patterns

Figure 14: SADP decomposition for 22nm cells

Table 1: DRC error on both Core and Trim mask

Layout	EDGE[a]		STST[a]			TMFC[a]		
	C[b]	T[b]	C[b]	T[b]	%[c]	C[b]	T[b]	%[c]
Layout1	2	13	2	10	23.1	2	3	76.9
Layout2	1	25	1	19	24.0	0	5	80.0
Layout3	2	32	2	29	9.4	0	12	62.5
Layout4	0	34	0	29	14.7	0	10	70.6
Layout5	0	18	0	16	11.1	0	9	50.0
Layout6	2	31	2	27	12.9	1	14	54.8
Layout7	3	31	3	28	9.7	2	11	64.5
Layout8	1	34	1	32	5.9	1	12	64.7
average	1.4	27.3	1.4	23.8	13.8	0.8	9.5	65.5

[a] $EDGE$: edge segment based coloring. $STST$: $EDGE$ + shortest-path coloring. $TMFC$: $STST$ + self-conflict coloring + trim friendly coloring
[b] C: the 1^{st} core mask, T: the 2^{nd} trim mask
[c] Improvement the errors on the trim mask from $EDGE$

ure 4, the shortest-path coloring ($STST$) in Section 3.3, and the mask friendly coloring ($TMFC$) in Section 3.5. The DRC conflicts mean both width and space violation given the minimum requirement for the core and the trim mask. The DRC conflicts on the core mask are very small, yet $TMFC$ has slightly fewer conflicts than other approaches. Meanwhile, the improvements on the trim mask is large when we use $TMFC$. $STST$ at the trim mask has around 14% improvement, yet $TMFC$ has as much as 65% improvement on average compared to $EDGE$. Table 1 shows that our SADP automation can decompose random 2D layout with just a few DRC conflicts which can be easily fixed by slightly modifying the target design.

Next we compared various approaches of the mandrel generation and evaluated lithographic printability in Table 2: *Shorter*, *Longer*, and *Directional* mandrel in Section 4.2. After performing OPC and lithography simulation, we calculated edge placement error (EPE) of the printed image. EPE is a popular metric to evaluate lithography simulated image. It means the difference between resulting simulated image and target design of an edge of layout. We measured the number of locations with EPE larger than $3nm$ at the best process condition, and $6nm$ at the out-focus (defocus) process condition. *Longer* mandrel shows the largest EPE at the both best and defocus conditions. This is because *Longer* mandrel has more horizontal and vertical patterns and some patterns are not well printed by dipole illumination. However, when we use *Longer* mandrel for the core mask, the patterning failures, in particular, missing small island pattern, is decreased compared to *Shorter*. It implies that *Shorter* mandrel is prone to removal at the 1^{st} patterning. Meanwhile when we applied *Directional* mandrel to the core mask, we achieved much smaller EPE variation without failing patterns. Even though EPE maybe dependent on input lithographic conditions, in our experiments *Directional* mandrel is the best option for the core mask in SID SADP decomposition.

Last, we compared the lithographic printability of SADP with that of LELE. The mask decomposition of LELE was performed by Proteus-DPT from Synopsys. According to [10, 14], since the 2^{nd} mask of LELE suffers from wafer topography effects, the lithographic process tolerance of LELE is around 30% less than SADP. Thus, we put more focus variation into the 2^{nd} mask of LELE, then counted the number of EPE variations of both two masks. The result shows that SADP has much smaller patterning variation despite not having stitch points. Thus we can say that SADP is promising for metal and other random layout patterning at the next lithography node.

Table 2: Printability check

Layout	Shorter			Longer			Directional		
	BF[a]	DF[a]		BF[a]	DF[a]		BF[a]	DF[a]	
	$3n$[b]	$6n$[b]	F[b]	$3n$[b]	$6n$[b]	F[b]	$3n$[b]	$6n$[b]	F[b]
Layout1	139	44	20	459	397	0	27	55	0
Layout2	216	54	3	669	593	1	15	52	0
Layout3	137	45	4	547	477	0	9	44	0
Layout4	111	68	0	502	473	0	9	70	0
Layout5	135	61	1	503	411	1	14	58	0
Layout6	138	71	2	536	438	2	15	66	0
Layout7	141	52	9	558	466	2	25	51	0
Layout8	91	39	1	451	401	0	5	40	0
average	139	54.3	5	528	457	0.8	14.9	54.5	0

[a] BF: at the best focus, DF: at the out focus variation
[b] $3n$: 3nm<EPE, $6nm$: 6n<EPE, F: patterning fail

Table 3: Comparison with LELE DPT

Layout	LELE DPT				SADP			
	BF[a]	DF[a]		S	BF[a]	DF[a]		S
	$3n$[b]	$6n$[b]	$9n$[b]		$3n$[b]	$6n$[b]	$9n$[b]	
Layout1	537	715	515	109	28	40	35	0
Layout2	822	1101	746	143	16	39	13	0
Layout3	626	833	598	148	9	39	12	0
Layout4	635	855	644	167	9	64	25	0
Layout5	541	750	525	78	14	43	24	0
Layout6	703	937	705	115	16	55	26	0
Layout7	666	948	671	87	26	40	20	0
Layout8	610	916	551	151	7	38	2	0
average	642.5	881.9	619.4	125	15.6	44.8	19.6	0

[a] BF: at the best focus, DF: at the out focus variation
[b] $3n$: 3nm<EPE, $6n$: 6nm<EPE≤9nm, $9n$: 9nm<EPE, S: # of stitch

6. CONCLUSION AND ONGOING WORK

In conclusion, we have shown several methods and options to produce manufacturable mask decompositions for sub-30nm metal random logic layouts with the SID style of SADP. The value of intelligent optimization methods for core and trim masks in SID SADP is clearly seen. Experimental results with industry designs show that the layout decomposition of SADP for 2D random layout is promising for the future lithography patterning. For future work, we plan to study SADP-aware routing and the electrical impact of SADP variation.

7. ACKNOWLEDGMENTS

This work is supported in part by SRC, NSF CAREER Award, and equipment donations from Intel.

8. REFERENCES

[1] Y. Chang et. al. Full Area Pattern Decomposition of Self-Aligned Double Patterning for 30nm Node NAND FLASH Process. In *Proc. SPIE 7637*, 2010.
[2] M. Gupta et. al. Timing Yield-Aware Color Reassignment and Detailed Placement Perturbation for Bimodal CD Distribution in Double Patterning Lithography. *IEEE Trans. on CAD*, 29, Feb 2010.
[3] M. Cho et. al. Double Patterning Technology Friendly Detailed Routing. In *In Proc. ICCAD*, Nov 2008.
[4] A. Kahng et. al. Layout Decomposition for Double Patterning Lithography. In *In Proc. ICCAD*, Nov 2008.
[5] G. Bailey et. al. Double pattern EDA solutions for 32nm HP and beyond. In *Proc. SPIE 6521*, 2007.
[6] J. Yang et. al. A New GraphTheoretic, MultiObjective Layout Decomposition Framework for Double Patterning Lithography. In *In Proc. ASPDAC*, Jan 2010.
[7] J. Yang et. al. Overlay Aware Interconnect and Timing Variation Modeling for Double Patterning Technology. In *In Proc. ICCAD*, Nov 2008.
[8] P. Leray et. al. Overlay metrology for double patterning processes. In *Proc. SPIE 7272*, 2009.
[9] L. Liebmann et. al. Taming the final frontier of optical lithography: Design for sub-resolution patterning. In *Proc. SPIE 7641*, 2010.
[10] Y. Ma et. al. Decomposition strategies for self-aligned double patterning. In *Proc. SPIE 7641*, 2010.
[11] W. Shiu et. al. Advanced self-aligned double patterning development for sub-30-nm DRAM manufacturing. In *Proc. SPIE 7274*, 2009.
[12] K. Yuan et. al. Double Patterning Layout Decomposition for Simultaneous Conflict and Stitch Minimization. In *In Proc. ISPD*, Mar 2009.
[13] K. Agarwal. Frequency Domain Decomposition of Layouts for Double Dipole Lithography. In *In Proc. DAC*, Jun 2010.
[14] S. Tseng et. al. Process Capability Comparison between LELE DPT and Spacer for NAND Flash 32nm and below. In *Proc. SPIE 7140*, 2008.