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#### ABSTRACT

Random testing is frequently an attractive alternative to deterministic test generation. How to estimate the coverage obtained by random testing is an important problem. This paper considers a possible technique for combinational circuits. Random testing properties of several combinational circuits are examined.

#### INTRODUCTION

INTRODUCTION

With increasing complexity of integration, deterministic test-generation is becoming very costly! In several instances random testing appears to be a very attractive alternative, as it requires no test generation. The problem with random testing is well known-given a number of randomly generated test vectors, how can an estimate of the coverage be obtained2,3,4? The converse problem is to obtain the number of random vectors which will obtain a specific coverage. A possible approach is examined here. Initially, an empirical approach is briefly considered. Random testing properties of combinational circuits are examined using a parameter-vector termed detectability-profile. An expression for the expected coverage obtained in terms of the detectability-profile is given. The expression is applicable for any coverage range, however for high coverage, a very convenient approximation can be used. Accuracy of the approximation is examined. Two measures for testability of combinational circuits are given. In the final section two heuristic procedures are outlined, which are based on general observations of the random testing properties.

## AN EMPIRICAL APPROACH

Several researchers have recently reported results of testing digital components which give the coverage obtained (also referred as testability<sup>5</sup>) against the number of vectors applied<sup>5</sup>,6,7. Tests can be generated using one of several methods. In purely random testing, the

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tests are generated and applied randomly (or at least pseudo randomly). In semi-random testing, the random process is modified by using additional information (e.g. obtained by simulation)<sup>7,8,9</sup>. In deterministic test generation, the tests are generated for specific sets of faults which constitute the fault-model. The deterministically generated tests may be applied in a random sequence, or the sequence may be obtained according to some criteria. For all these, the curves of coverage obtained against the number of vectors appear to have similar shapes. The coverage rises rapidly in the beginning, the slope then gradually declines and then the curve approaches unity practically asympotically. If additional information is used, it is possible to maximize the performance for a specific number of vectors, the coverage obtained by optimization declines as coverage approaches unity. tests are generated and applied randomly (or at

vectors, the coverage obtained by optimization declines as coverage approaches unity.

The general regularity of the curve suggests that a simple empirical relationship may be possible. One approach is to use a polynomial of limited degree with coefficients as parameters<sup>10</sup>. However, as the curve has a general shape of a l-exp(-x) curve, it might be better to start with a resemble bypothesis, which will a start with a resonable hypothesis which will yield this shape. A simple hypothesis can be that the rate of increase of coverage C, with the number k of vectors applied, is proportional to some power of the fraction of faults still not covered, i.e.

$$\frac{dC}{dk} = a(1-C)^{b} \tag{1}$$

where a and b are some parameters. This has the solution:

$$C = 1 - [1 + a(b-1)k]^{-1/(b-1)}, b \neq 1$$
 (2)

= 1-exp(-ka) , b=1 (3
A preliminary check of consistency of this relationship was done by using the curves reported in [5]. The values of a and b were evaluated for different ranges in a curve by choosing two points in the range and evaluating a and b using equation 2. As closed form relations are not obtainable, numerical search was used. As very limited amount of data was used. used. As very limited amount of data was used, the results cannot be stated very definitely. The relation does not seem to hold well for coverage below 0.5 or above 0.99. This has the possible explanation that the numbers below 0.5 or above 0.99 represent situations which are quite random, where general rules should not be expected to hold. The parameter 'a' can be

considered a scale factor for  $k,\ as\ equation\ 1$  can be rewritten as

$$\frac{dc}{dk^{T}} = (1-c)^{b} \tag{4}$$

where k'=ak. The parameter 'b' is harder to interpret directly. Its value seems to be in the neighborhood of 1.6 to 3.0 for different devices examined in [5]. Although equation 2 appears to hold only for a limited range; this range is perhaps the range of interest. It may be useful in predicting the increase in coverage with the increase of test cost allowed. It is interesting to notice here that if b=2 and k>1/a, then k(1-c)=1/a. Then having twice as many test-vectors will leave only half as many uncovered faults. Further study is needed to evaluate usefulness of equation 1. evaluate usefulness of equation 1.

## THE DETECTABILITY PROFILE

In order to mathematically examine the In order to mathematically examine the random testing properties of combinational networks, another approach is considered here. It uses a parameter-vector called detectability-profile. It is applicable to any assumed fault model, and thus can be used for both gate-level and transistor-level faults. The detectability-profile I of a circuit is given by profile I of a circuit is given by

a partitioning of all the faults assumed in the chosen fault model. We have obtained detectability-profiles for a number of commonly used combinational functions, as shown in Figures 1-7. Notice that Figure 4 uses data about transistor level faults, given in [17]. As the figures indicate, the detectability profile is often a sparse vector. Generally it takes considerable effort to evaluate a detectability profile. It is hoped that examination of representative combinational circuits will provide better understanding of random testing properties of understanding of random testing properties of general combinational circuits.

# COVERAGE OBTAINED BY RANDOM TESTING

Here, an expression will be obtained for the number of new faults tested when k-th vector is applied. This expression will be in terms of  $\boldsymbol{\pi};$ it corresponds to equation 1, which was in terms of the empirical parameters a and b. Let

If the vectors are selected randomly with replacement (i.e. a vector can be chosen again), then the probability that any vector is a test for fault f<sub>1</sub> is equal to ni/N where ni is the number of vectors which test for fault f<sub>1</sub>. For this case equation 6 gives

this case equation 6 gives
$$p_k^{i} = \frac{ni}{N} (1 - \frac{ni}{N})^{k-1}.$$
(7)

It is useful to examine the case when the random vectors are chosen without replacement. A vector once applied will not be chosen again. To arrive at an expression for pk for thie case, let us define

$$\chi_1^i = \text{Pr } \{f_i \text{ is tested by the 1th vector}\}$$
  
= ni/N-1+1. (8  
e it should be noticed that for 1=N-ni+1,

$$p_{k}^{i} = \begin{bmatrix} k-1 \\ 1-1 \end{bmatrix} (1-X_{1}^{i}) \end{bmatrix} X_{k}^{i}, 1 \leq k \leq N$$
(9)

(10)

$$p_3^i = \frac{ni}{N} \cdot \frac{(N-ni)}{N-1} \cdot \frac{(N-ni-1)}{N-2}$$
, etc. In this

= ni/N-1+1. Here it should be noticed that for l=N-ni+1,  $X_1^1=1$ . This is because all the remaining nivectors at this stage, test for  $f_1$ . Corresponding to equation 7 we have  $p_k^1=\begin{bmatrix} \pi & (1-x_1^1) \end{bmatrix}.X_k^1, \ 1 \le k \le N \\ p_k^1=\begin{bmatrix} \pi & (1-x_1^1) \end{bmatrix}.X_k^1, \ 1 \le k \le N \\ 1-1 \end{bmatrix}$  This gives  $p_1^1=\frac{ni}{N}$ ,  $p_2^1=\frac{ni}{N}\cdot N-1$ ,  $p_3^1=\frac{ni}{N}\cdot\frac{(N-ni)}{N-1}\cdot\frac{(N-ni-1)}{N-2}, \ \text{etc. In this}$  form, equation 9 can be rewritten as  $p_k^1=n_1^1\frac{(N-ni)!}{N!/(N-k)!}, \ 1 \le k \le N.$  (10) Let us now define random variables  $d_k^1$ , i=1 to M, where M is the total number of faults possible. The r.v.  $d_k^1=1$  if the fault  $f_1^1$  is first detected by the k-th vector, otherwise  $d_k^1=0$ . The total number of new faults tested by the k-th vector is given by

$$F_{k} = \sum_{i=1}^{M} d_{k}^{i}.$$
 (11)

The ensemble average or the expected number of new faults tested by the k-th vector is then,

$$\overline{F}_{k} = E\{F_{k}\} = E\{\sum_{i=1}^{M} d_{k}^{i}\}.$$

As mean of a sum is the sum of the means, regardless of the statistical dependence 1, we may write

$$F_{k} = \sum_{i=1}^{M} p_{k}^{i}$$

$$= \sum_{n_{i}=1}^{N} \pi_{n_{i}} p_{k}^{i}.$$
(12)

The last form of the R.H.S. uses the detectability-profile partiioning of the faults. When the vectors are chosen with replacement, then from equations 8 and 12 we obtain

$$F_{k} = \sum_{\substack{n=1\\ n \neq 1}}^{N} \pi_{ni} \cdot \frac{ni}{N} (1 - \frac{ni}{N})^{k-1}.$$
 (13)

then from equations 8 and 12 we obtain 
$$F_k = \sum_{\substack{n \text{ ini} = 1 \\ n \text{ ini} = 1}} \pi_{\text{ini}} \cdot \frac{ni}{N} (1 - \frac{ni}{N})^{k-1}. \tag{13}$$
 The total expected coverage (as a fraction of total faults covered) is then obtained as 
$$\overline{C}_k = \{\sum_{l=1}^{K} \sum_{\substack{n \text{ ini} = 1 \\ l=1 \text{ ini} = 1}} \pi_{\text{ini}} \cdot \frac{ni}{N} (1 - \frac{ni}{N})^{l-1} \} / \tag{14}$$

Σπni=1

The denominator of equation 14 is equal to M, the total number of faults. Equation 14 can be simplified by reversing the order of summation, to

$$\overline{C}_{k} = \{ \sum_{n=1}^{N} \pi_{ni} [1 - (1 - \frac{ni}{N})^{k}] \} / \sum_{n=1}^{N} \pi_{ni}.$$
 (15)

 $\begin{array}{c} R \\ \overline{C}_k = \{\sum\limits_{i=1}^N \pi_{ii}[1-(1-\frac{ni}{N})^k]\}/\sum\limits_{i=1}^N \pi_{ii}. \end{array}$  (15)
 It is interesting to compare this with equations 2 and 3. It will be difficult to reduce equation 15 to equations 2 or 3 except in special situations. This suggests that equations 2 or 3 should not be expected to hold over a wide range of values.

range of values.
A similar expression can be obtained for

A similar expression can be obtained for random testing without replacement of vectors. Using equations 8, 9 and 12, we have 
$$\frac{k}{C_k} = \{ \sum_{j=1}^{K} \sum_{n_i = 1}^{K} (\pi_{n_i} \begin{bmatrix} j-1 \\ 1=1 \end{bmatrix} (1-X_1^i) \end{bmatrix}, X_j^i \} / (16)$$

$$\frac{N}{\sum_{n_i = 1}^{K} \pi_{n_i}}.$$

Some pseudo-random test pattern generation techniques will not generate a vector twice if less than the exhaustive number of vectors is generated. In such a case equation 16 can be used. In most cases, except for smaller circuits and when extremely high coverage is required, both equations 15 and 16 will yield about the same result.

### A USEFUL APPROXIMATION

The equation 15 contains a  $[1-(1-ni/N)^{k}]$ The equation 15 contains a [1-(1-ni/N)^n] term for each fault. This allows us to examine the effects of individual faults with different testability. Its compliment, (1-ni/N)k, which may be termed the uncoverage factor, is given in Table 1 for different detectability values and number of vectors. Similarly individual terms in equation 13, given by ni/N(1-ni/N)k-1, can be called increase factor; its values are given in Table 2.

Number of	Detectability of fault (ni/N)					
vectors	0.01	0.1	0.5			
1	0.990	0.900	0,500			
5	0.951	0.590	3.12E-2			
10	0.904	0.348	9.76E-4			
50	0.605	5.15E-3	8.88E-16			
100	0.366	2.65E-5	7.88E-31			
500	6.57E-3	1.32E-23	0.0			

Table 1: Uncoverage factor for faults with different detectability.

Number of	Detectabi	lity of fault	(ni/N)
vectors	0.01	0.1	0.5
1	0.01	0.10	0.5
5	9.60E-3	6.56E-2	3.12E-2
10	9.13E-3	3.87E-2	9.76E-4
50	6.11E-3	5.72E-4	8.88E-16
100	3.69E-3	2.95E-6	7.88E-31
500	6.63E-5	1.468E-24	0.0

Table 2: Increase factor for faults with different detectability.

It is apparent that in the beginning of the It is apparent that in the beginning of the test experiment, most of the increase in coverage will be due to faults with small ni. As testing proceeds, only faults with low detectability are likely to be left uncovered. In the region of very high coverage, further increase in expected coverage is mainly due to fault with low detectability. This observation is significant. This suggests that the behavior at very high coverage can be approximated by considering only coverage can be approximated by considering only a suitable set of faults with lowest detectability. Thus only the lower components of the detectability profile need to be evaluated or estimated to predict the behavior in the high coverage region.

This approximation is consistent with the Inis approximation is consistent with the conclusions reached by other researchers. David et al.12 have used an effectiveness measure for random testing called detection quality, which is the probability of detecting the least detectable fault. Savir and Bardell have used a measure called escape probability, which is the probability that at least one fault will not be described by the test experiment. By examining the bility that at least one fault will not be detected by the test experiment. By examining the testing process involving two faults with conjoint (i.e. not disjoint) test sets, they have observed that the fault with significantly higher detectability has no practical effect on the number of vectors to be used to achieve given escape probability. The technique suggested by Agrawal 16 to see if a circuit is suitable for random testing can be justified by using similar considerations as fan-in and the number of levels will characterize the faults most difficult to will characterize the faults most difficult to

For a preliminary examination of the validity of this approximation, let us assume that the two least detectable sets of faults have detectability A/N and B/N, and let the corresponding components of the detectability profile be  $\pi_A$  and  $\pi_B$ . Let us assume that the contribution of the second set is insignificant when its contribution is one tenth or less, i.e.

$$\pi_{A}(1-A/N)^{k} \geq 10.\pi_{B}(1-B/N)^{k}.$$
 (17)

This can be used to evaluate k when the assumption just starts to hold. The corresponding uncoverage (1-coverage) can be computed by this approximate form of equation 15.

$$U = 1/M \left[ \pi_A (1-A/N)^k + \pi_B (1-B/N)^k \right]$$
 (18)

Three devices were examined: a double 4-to-1 MUX (745153), Schneider's example 13, and a (3x6x3) PLA. The results are given in Table 3. The value of k and the uncoverage, for which assumption holds, is given. The approximation always holds for the MUX and for the Schneider's example at and above the coverage of 0.93; however for the PLA, it does not hold until the coverage of 0.996 has been obtained. The major reason for the difference is the relative values of the first two components of the detectability profile. The conclusion is that at least in some profile. The conclusion is that at least in some cases considering only the set of most undetectable faults may not be enough.

	200					min.			
Device	М	N	Α	В	$\pi_A$	$\pi_{B}$	k	U	
1	112	4096	256	512	72	6	1	0.65	
2	48	16	1	2	23	19	31	0.07	
3	98	8	1	2	6	15	21	0.004	

Table 3: Examination of approximation.

It should be observed from the above that the expected coverage asymptotically approaches unity with increasing number of vectors applied, but is never exactly one, if the vectors are selected with replacement. When vectors are selected without replacement, coverage of one is always obtained with the conductive number of is always obtained with the exhaustive number of

## MEASURES OF TESTABILITY

Recently, considerable attention has been given to measures of testability. Some measures define testability of a node in terms of its controllability and observability. However correlation of such measures with experimental behavior may not be very highl4. It has been shown by Savir, the testability may not directly depend on the number of vectors which control the fault and the number of vectors which observe the fault15. It rather depends on the number of vectors in the intersection of the two sets. From the very definition, a detectability profile is a vector-measure of testability. It is possible to define a scalar measure for a combinational circuit using detectability profile concept.

Concept.

Let us define a testability measure T1, which is the average number of vectors (normalized by dividing by the total number of possible vectors) needed to detect a fault. It is assumed that only one of all possible faults

Let us assume that a fault  $f_i$  exists. Then,  $Pr\{k-th \ vector \ will \ detect \ f_i \cap f_i \ was not \ detected before} = <math>Pr\{k-th \ vector \ will \ detect \ f_i | \ it \ was \ not \ detected \ before} = ni/N(1-ni/N)k-1.$ 

If the average value of k, which will detect the fault is shown by  $K_1$ , then,

$$\overline{K}_{1} \approx \sum_{k=1}^{\infty} k \cdot \frac{ni}{N} (1 - \frac{ni}{N})^{k-1}$$

$$= \frac{N}{N}.$$

If all faults are equally likely, then the average value of K for all the faults is given by
$$\overline{K} = \sum_{i=1}^{M} (\frac{1}{M}) \cdot \frac{N}{ni} = \frac{1}{M} \sum_{n=1}^{N} \pi_{ni} \cdot \frac{N}{ni}$$
(19)
$$= \frac{N}{M} = \frac{1}{M} \pi_{ni}$$

Then the measure T1 is

$$T1 = \frac{1}{M} \sum_{\substack{n = 1 \\ n \neq -1}}^{N} \frac{\pi_{ni}}{ni}.$$
 (20)

 $T1 = \frac{1}{M}\sum_{\substack{n_1=1\\ n_1=1}}^{N}\frac{\pi_{n_1}}{n_1}. \tag{20}$  The values of T1 for some devices is found to be as follows. Double 4-to-1 MUX = 0.003 (11.8/4096), 1-of-4 decoder: 0.76 (3.04/4), Schneider's example 0.75 (12/16), 3x6x3 PLA: 0.46 (3.6/8) and 3-level NAMD tree 0.04 (9.5/256). The low value of the measure for the 1-of-4 decoder and the Schneider's example are because of the higher values of the detectability profile at the low end.

Another measure, T2, can be the fraction of vectors needed to obtan a specific expected coverage, say 0.99. It can be easily obtained using equation 15, and numerical search. The using equation 15, and numerical search. The results for devices considered are given here. Double 4-to-1 MUX: 0.016 (65/4096), 1-of-4 decorder: 3.5 (14/4), Schneider's example 3.87 (62/16), 3x6x3 PLA: 2.75 (22/8) and 3-level NAND tree 0.195 (50/256). The devices with T2>1 are clearly not suitable for random testing. However if the random test patterns are generated without replacement, then T2 will always be at most one. Result of a simulation will greatly depend on the algorithm used to generate the without replacement, then 12 will always be at most one. Result of a simulation will greatly depend on the algorithm used to generate the random or pseudo-random vectors. The numbers obtained by Agrawal by simulation for the MUX and the Schneider's example show little correlation with T216.

Another perhaps even more directly usable measure (if it can be evaluated) can be the expected number of vectors which will provide complete coverage. Following the approach of Savir and Bardell<sup>4</sup>, the complexity involved can be illustrated by considering only two faults. Let nl and n2 be the number of vectors testing for faults f<sub>1</sub> and f<sub>2</sub>. Let n12 be the number of vectors which test for both f<sub>1</sub> and f<sub>2</sub>. Consider Pr{total coverage obtained with exactly k vector} = Pr{Both detected with k-1 vectors} = Pr{Both detected with k-vectors} - Pr{Both detected with k-vectors} - Pr{Both detected with k-vectors} = 1-(1- \frac{n1}{N})^k - (1- \frac{n2}{N})^k + (1- \frac{n1+n2-n12}{N})^k = 1-e\_k \quad (22)

$$=1-(1-\frac{n1}{N})^{k}-(1-\frac{n2}{N})^{k}+(1-\frac{n1+n2-n12}{N})^{k}$$

$$=1-e_{k}$$
(22)

where ek represents the three terms. Using equation 22, equation 21 can be written as Pr{total coverage obtained with exactly k vectors}  $= e_{k-1} - e_k$ . (23) The expected number of vectors needed for total coverage is then

$$K = \sum_{k=1}^{\infty} k(e_{k-1} - e_k)$$

$$= \frac{N}{n1} + \frac{N}{n2} - \frac{N}{n1 + n2 - n12},$$
(24)

obtained after some arithmetic manipulations. Here presence of n12 must be noticed. This shows

the conjointness among the faults must be taken into account. As most practical combinational circuits have a large number of faults, an expression corresponding to equation 24 will be too complex to obtain.

#### TEST GENERATION PROCEDURES

Based on the observations in the previous Based on the observations in the previous sections, two heuristic procedures can be outlined. They are useful if a major assumption is satisfied. The assumption is that the major classes of combinational circuits have been examined, and the circuit to be tested either belongs to one of the known classes (and thus two lowest components of the detectability profiles can be estimated), or is unknown except for its functional behavior. A test experiment will have one of these objectives:

(i) Total coverage is required. This would

have one of these objectives:

(i) Total coverage is required. This would be necessary for ultra-high reliability applications and for manufacturing testing of newly developed devices. In this case the objective of using random testing would be to reduce the cost of deterministic test generation. Procedure 1 below outlines a possible procedure.

(ii) Moderately high coverage (90-99%) is required. This would be the case when a low field unacceptance rate is not catastrophic and is cost effective. Procedure 2 presents a possible procedure.

ble procedure.

ble procedure.

(iii) An unknown circuit is to be tested to an 'acceptable' degree. In thie case, although the functionality of the circuit is known, its internal design is unknown. Obviously, Procedures 1 and 2 cannot be applied directly. It is necessary to first obtain a reasonable, assumed set of faults, and then use a modification of Procedure 1 or 2. There are two options. One is to define a set of functional faults. The other is for the test engineer to implement the functional behavior as a logic diagram, and then identify the physically possible faults. The second option would always be at least as good as the first option, as the test set for the produced logic diagram will always exercise the functionality.

Procedure 1: Test-generation
for total coverage

1. Partition the combinational circuit into
disjoint parts if possible. Consider each part
separately for the following steps.
2. Make a preliminary determination of
random testability of the circuit. Attempt random
test generation only if the circuit is suitable
for random testing.

test generation only if the circuit is suitable for random testing.

3. Identify the hardest to test faults using methods like in [18], corresponding to the lowest element of the detectability profile.

Deterministically generate tests for these.

4. By simulation, obtain set of faults which will be detected by tests generated in step 4.

Remove these from further consideration.

5. Generate a number of random tests. The

5. Generate a number of random tests. The number of random tests to be generated can be obtained as the number necessary to obtain

coverage of 0.95, using the second lowest element of the detectability profile. Accuracy in this computation is not required.

6. By simulation, obtain the set of faults covered in step 5.
7. Use deterministic test generation for the rest of the faults.

## Procedure 2: Test generation

for high coverage
Here it is assumed that the expected coverage to be obtained is given. The first four steps are same as in Procedure 1.

5. Recompute the coverage to be obtained in

terms of the remaining number of faults.
6. Using the second lowest element of the detectability profile, obtain the number of random vectors needed to obtain the required coverage.
If necessary, simulation can be used after step 6 to verify the coverage obtained, and

appropriate corrective action may be taken.

The two procedures above will have advantage over deterministic test generation only if total cost of obtaining and running a simulator is less than the alternative. [1] suggests it may not always be so.

### CONCLUSION

From the above discussion, it is seen that From the above discussion, it is seen that the defectability profile can provide significant information about random testing properties of combinational circuits. Although the defectability profile does not contain information about conjointness of test-sets for individual faults, some useful expressions can be obtained. The validity of the assumption that only the lowest component of the detectability profile is needed to estimate coverage has been examined. It apto estimate coverage, has been examined. It appears that the data from a large number of circuits must be examined before definitive observations can be made.

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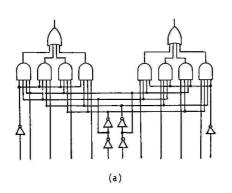
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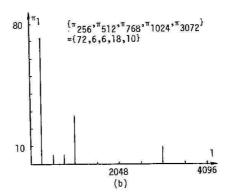


Fig.1: a. Logic diagram of a double 4-to-4 MUX(74153)

b. Detectability profile

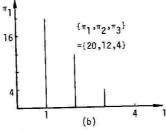
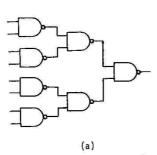


Fig.2: a. Logic diagram of a 1-of-4 decoder

b. Detectability profile



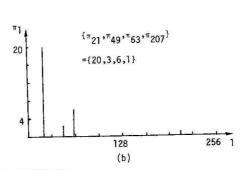
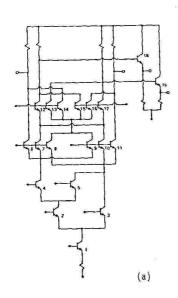


Fig.3: a. Logic diagram of a 3-level NAND-tree

b. Detectability profile



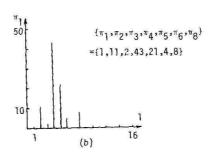
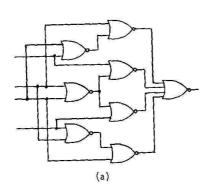


Fig.4: a. Logic diagram of a CECL full adder  $^{\mbox{\scriptsize 17}}$  b. Detectability Profile



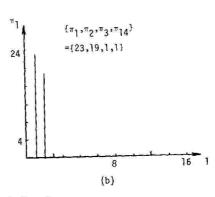


Fig.5: a. Logic diagram of Schneider's Example b. Detectability profile

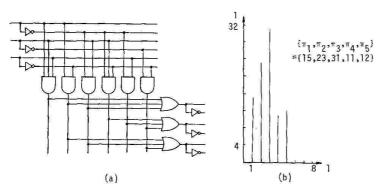


Fig.6: a. Logic diagram of a 3x6x3 PLA b. Detectability Profile

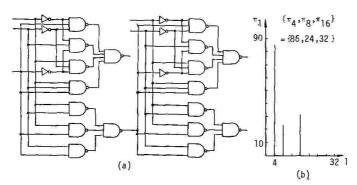


Fig.7: a. Logic diagram of a 2-stage adder b. Detectability Profile