An X-Band Radar Transceiver MMIC with Bandwidth Reduction in 0.13 μm SiGe Technology

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***Abstract*—This paper presents an X-band chirp radar transceiver with bandwidth reduction for range detection. The radar transceiver includes a super-heterodyne receiver including an ADC, a direct-digital synthesizer (DDS) based transmitter and a phase-locked loop (PLL) synthesizer. In a modified Weaver architecture, the down-converted baseband signal is further mixed with another chirp signal through stretch processing. The resulting waveform bandwidth is greatly reduced and thus relaxes the power and bandwidth requirements of the on-chip ADC. Therefore, the proposed radar transceiver achieves power and bandwidth reductions without degrading its range resolution. The radar-on-chip (RoC) MMIC was implemented in a 0.13 μm SiGe technology with die area of 3.5 × 2.5 mm². With a 2.2 V supply for analog/RF circuits and a 1.5 V supply for the digital portion, the chip consumes 326 mW in the receive mode and 333 mW in the transmit mode, respectively.**

***Index Terms*—Chirp, DAC, DDS, FM, PLL, PM, SiGe, stretch processing, radar, receiver, transmitter.**

I. Introduction

INTEGRATED radar transceivers have been recently explored for ranging detection in mobile environments [1]–[9]. Pulse radar and ultra-wideband (UWB) radar require high peak-to-average power ratios (PAPR) or wideband operation to transmit or receive narrow pulse signals [1]. The direct-conversion receiver topology is popular in frequency modulated continuous wave (FMCW) radars due to its simple architecture and low cost for both area and power [2], [3]. The heterodyne receiver architecture is known as the most reliable reception technique due to its excellent sensitivity and selectivity. Applying an off-chip surface acoustic wave (SAW) filter eliminates the out-of-band interferences. In voltage-controlled oscillator (VCO)-based and analog PLL-based FM radars, the chirp signal is generated at the VCO output [1]–[5]. Therefore chirp signal mixing occurs at the radio frequency (RF) band. Our DDS-based chirp radar generates the chirp signal in the baseband. Thus chirp signal processing is done in the receiver baseband, which relaxes the design requirements for the signal processing circuitry and reduces power consumption [6]. When compared with VCO and PLL-based chirp radars, the DDS based RoC is featured with fast modulation, fine frequency steps, and a flexible output frequency range, especially in generating the baseband chirp signal [10]. The relative delay, the frequency slope and the initial phase of the transmitted chirp are all programmable and controllable, which adds flexibility to the design of these radar systems.

In pulse-compression radars, the narrow width pulse is recovered after pulse decompression in the receiver. A narrow pulse width in the time domain corresponds to a wide bandwidth in the frequency domain. Since the radar range resolution is inversely proportional to the transmitted bandwidth, it is thus desirable to transmit the chirp waveform with as wide a bandwidth as possible. Recently, ultra-high-speed DDS monolithic microwave integrated circuits (MMICs) have become capable of generating waveforms with ultra-wide bandwidth [11]. However, receiving and processing the received signal with such a wide bandwidth imposes tremendous challenges upon the receiver circuits, e.g., the design of the ADC.

The proposed RoC transceiver with stretch processing mixes the received chirp signal with a stretch chirp signal, resulting in a much reduced bandwidth at the ADC input. Therefore, the proposed transceiver achieves receiver bandwidth reduction without compromising the transmitted chirp bandwidth, which is needed to achieve fine range resolution.

II. Architecture of Radar Transceiver

A. Stretch Processing Radar

In the subsequent analysis, the following terms are employed (referring to Fig. 1): $\mathrm{B_{RX}}$ is the bandwidth of the reference chirp (or stretch chirp) in the receiver, $\mathrm{B_{TX}}$ is the bandwidth of the transmitted chirp, α is the slope of the chirp, $\mathrm{t_{TX}}$ is the duration time of the transmitted chirp, $\mathrm{t_{REF}}$ is the start time of the stretch chirp in the receiver, $\mathrm{t_D}$ is the time that the transmitted chirp has travelled before reaching the receiver, and $\mathrm{t_{MAX}}$ is the time at which the stretch chirp stops. For fixed-chirp-rate stretch processing, a high bandwidth linear chirp is transmitted toward the target. The product of the transmit period and the chirp rate yields the effective transmitted bandwidth $\mathrm{B_{TX}}$, which defines the range resolution of the radar, namely, $R_{\mathrm{res}} = c/(2B_{\mathrm{TX}})$, where c is the speed of light. As shown in Fig. 1, a stretch chirp with the same chirp rate α as the transmitted chirp is produced by the transceiver with a longer time duration t_{RX} which is required to demodulate the received signal. A single-tone signal with a frequency of Δf, which contains the target range information, is obtained after stretch processing. The chirp rate for

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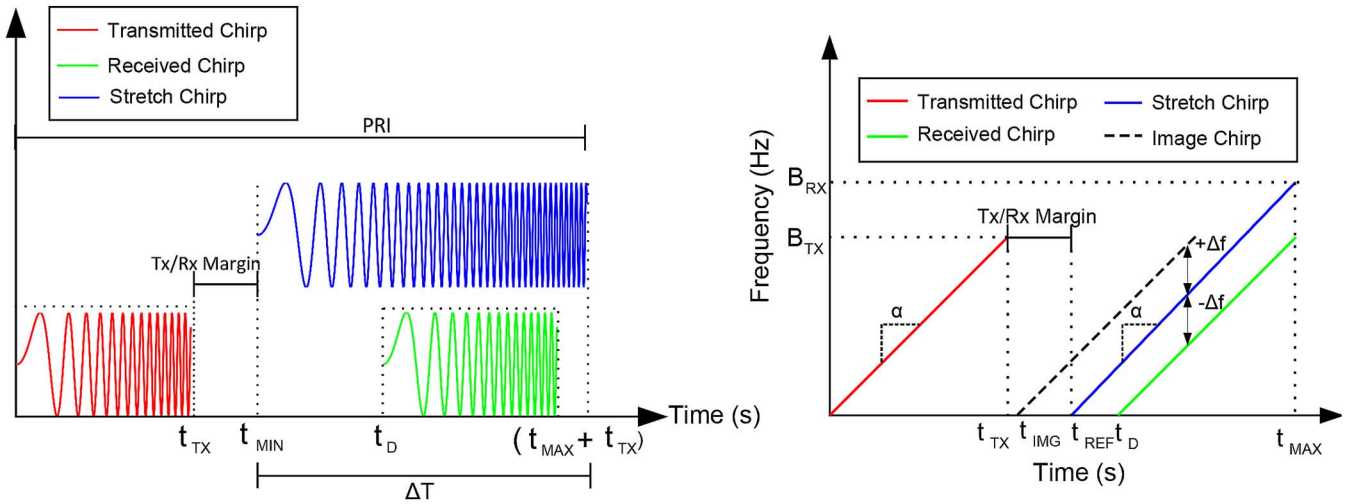

Fig. 1. An illustration of stretch processing in time domain (left) and frequency domain (right).

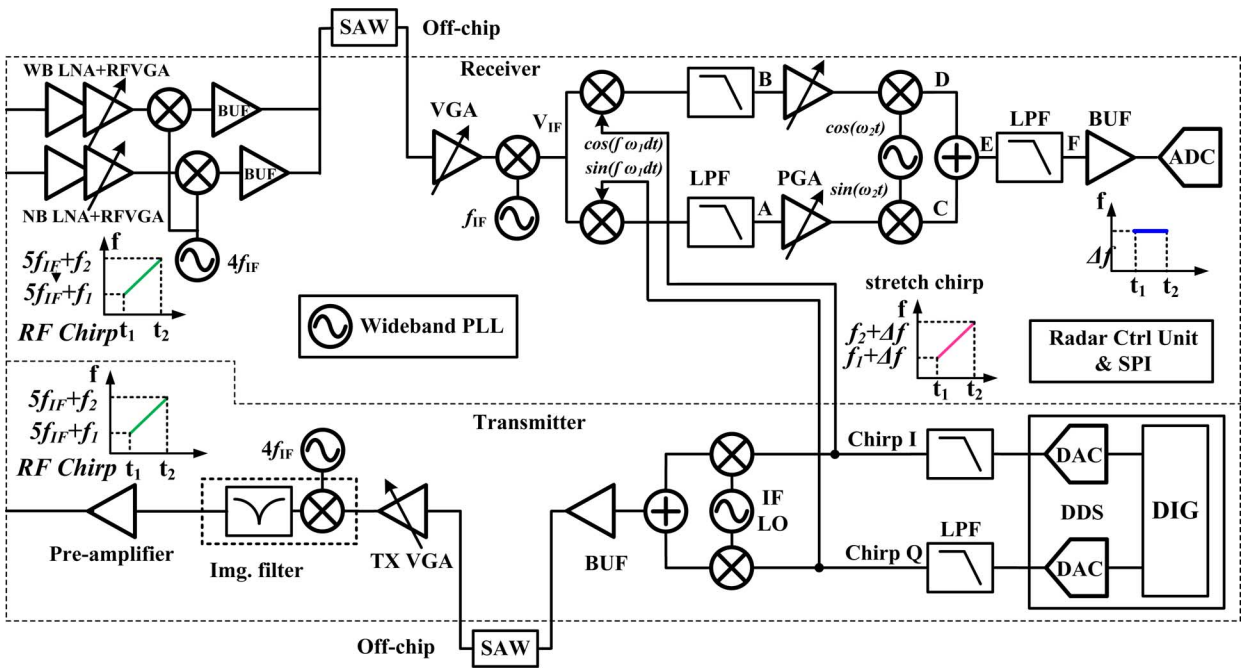

Fig. 2. Block diagram of the chirp radar transceiver with stretch processing.

the stretch chirp can also be different from the transmitted chirp, and in fact a chirp signal with slower chirp rate will be generated after the stretch processing.

As shown in Fig. 2, the proposed super-heterodyne radar transceiver is comprised of a receiver front-end, a modified Weaver receiver baseband, an ADC, a quadrature DDS-based transmitter, a PLL, and a Radar Control Unit (RCU). The proposed radar transceiver exhibits the following characteristics: 1) a reduced bandwidth (20 MHz) at the input of the ADC is achieved through stretch processing, while a wider bandwidth (150 MHz) is transmitted to obtain high range resolution; 2) a low-IF detection is implemented by mixing the baseband signals with an offset frequency, which allows for the use of a single ADC; and 3) the above improvements result in greatly reduced receiver bandwidth and power consumption, as well as the complexity of the ADC.

B. Modified Weaver Receiver

Super-heterodyne receivers with a low-IF output present challenges with image cancellations. The modified Weaver receiver is featured with two-stage down conversion and image rejection. In order to implement stretch processing in the receiver baseband circuitry, the Weaver receiver architecture is revised by replacing the quadrature LO signals at the 1st IQ demodulator with the stretch chirp generated by the transmitter, as shown in Fig. 2. Multiple LO paths may generate a dc offset at mixer output. In a super-heterodyne receiver, the mixing from RF to IF will not cause dc offset since the IF signal

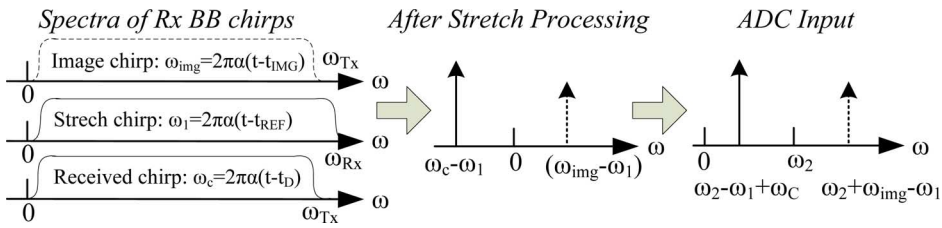

Fig. 3. Spectral analysis of the modified Weaver receiver architecture.

is band-pass filtered. The dc offset may occur at the mixing stage from IF to baseband signals. However, the dc offset at lowered frequency has much lower magnitude due to reduced EM coupling and no presence of large gain stages at input of the IF mixer. Moreover, baseband chirps can be set to start at non-zero frequencies, which allow ac-couple for the baseband signals and thus eliminate the dc offset. Therefore, the modified Weaver receiver has ignorable dc offset effect.

The adoption of the modified Weaver receiver with stretch processing is justified through the following spectral analysis. The low-pass filters, buffer, mixer and amplifier in the derivations below are assumed to be ideal with unit gain for simplicity. Both the stretch chirp and second LO (V_2) have unit amplitude. The input chirp, stretch chirp and second LO signal can be expressed as $V_{\rm IN} = A_{\rm sig}\cos(\int \omega_c dt) + A_{im1}\cos(\int \omega_{\rm img} dt)$, $V_{\rm strech\_I} = \cos(\int \omega_1 dt)$, and $V_{2\_I} = \cos(\omega_2 t)$, respectively. $A_{\rm sig}$ and $A_{\rm img}$ represent the amplitudes of the input chirp and image chirp signals. As shown in Fig. 1, the frequencies of the input chirp, stretch chirp and image chirp are defined as $\omega_c = 2\pi\alpha(t - t_D)$, $\omega_1 = 2\pi\alpha(t - t_{\rm REF})$ and $\omega_{\rm img} = 2\pi\alpha(t - t_{\rm IMG})$, where $t_{\rm IMG}$ is the time when the image chirp arrives at receiver. Input signal ($V_{\rm IN}$) is mixed with the quadrature stretch chirp signals. The low-pass filtered signals are mixed with the low-IF LO (ω_2) in the second IQ modulators, and the resulting signals are $V_F = (A_{\rm sig}/2)\cos(\omega_2 + \omega_c - \omega_1)t + (A_{\rm img})/(2)\cos(\omega_2 + \omega_{\rm img} - \omega_1)t$. The frequency of the desired signal at the receiver output reads $\omega_2 + \omega_c - \omega_1 = \omega_2 + 2\pi\alpha(t_D - t_{\rm REF})$, from which the time delay t_D can be extracted and the range of the target is given by $(1/2)ct_D$. The component $(A_{\rm img}/2)\cos(\omega_2 + \omega_{\rm img} - \omega_1)t$ represents the output of the image signal which otherwise falls into desired signal band without Weaver receiver when $\omega_{\rm img} = 2\omega_1 - \omega_c$ holds. Also, without the presence of an image chirp, it is possible to identify whether t_D is less or larger than $t_{\rm REF}$ by using Weaver architecture. The modified Weaver receiver performance can also be understood through the spectral analysis shown in Fig. 3.

The proposed RoC MMIC needs to meet various specifications including range resolution and detectable range, which determine the required ADC bandwidth, namely, $\rm BW_{ADC} = c(l_2 - l_1)/[R_{res}(l_2 + l_1)]$, where $\rm l_1$ and $\rm l_2$ are the minimum and maximum ranges. Since range resolution$\rm R_{res} = c/2\alpha t_{TX}$, chirp rate α is determined by $\rm R_{res}$. Should chirp rate is reduced, it is necessary to increase transmission time $t_{\rm TX}$ to keep the same resolution. Meanwhile, the transmission time is limited since receiver needs to have the stretch chirp ready when radar signal is echoed back from the target.

C. Impact of Group Delay on Radar System Performance

Since the chirp signal possesses wide bandwidth and is vulnerable to nonlinearity, special attention was given to the investigation of the impact of circuit nonlinear properties on radar system performance, such as range resolution. In particular, the impact of group delay (GD) will be analyzed in this section. Assume phase variation can be expressed by a second-order polynomial $\theta = k_1\omega^2 + k_2\omega + k_3$, where $\omega = 2\pi\alpha t$. The group delay can then be derived as $GD = 2k_1\omega + k_2$. The resulting waveform after stretch processing is given by $e^{j(2\pi\alpha t_D t + \theta)}$ with its frequency being expressed as $f = (1/2\pi)(d(2\pi\alpha t_D t + \theta)/dt) = \alpha t_D + 4k_1\pi\alpha^2 t + k_2\alpha$, where $k_2\alpha$ is a constant shift, while $4k_1\pi\alpha^2 t$ varies with time and thus extends the spectrum. Therefore in the presence of group delay, the time resolution of the radar is degraded to $|(\alpha t_D + 4k_1\pi\alpha^2 t)/\alpha| \le t_D + |4k_1\pi B_{\rm TX}|$. $4a\pi B_{\rm TX}$ is the error term caused by the group delay. Accordingly, the range resolution of the radar system is degraded to $(t_D + |4k_1\pi B_{\rm TX}|)\times(c/2) = t_D(c/2) + |2k_1\pi B_{\rm TX}c|$.

Because the current bandwidth specification is 150 MHz, which translates to a resolution of 1 meter, it is safe to assume that the range resolution tolerance $2k_1\pi B_{\rm TX}$c to be 0.1 m. Therefore, $k_1 = 0.1/2\pi B_{\rm TX}c$. The tolerable GD variation is thus given by

$$GD_{\rm variaion} = 2k_1 \times 2\pi B_{\rm TX} = \frac{0.1}{\pi B_{\rm TX}c} \times 2\pi B_{\rm TX} = \frac{0.2}{c} \approx 666 \text{ ps}. \quad (1)$$

With careful design, simulations showed that the two critical blocks, the LNA and the PA driver, demonstrate GD variations of 20 ps and 70 ps, respectively, which are negligible compared to the tolerable $\rm GD_{variaion}$ estimated in (1). Throughout the design, all building blocks of the proposed radar transceiver MMIC are carefully checked for group delay variations to ensure the total group delay introduced through the transmitter and receiver are within the above established maximum tolerable GD variation.

D. Gain of Stretch Processing

In concert with other spread-spectrum operations, the chirp signal also occupies a wide bandwidth and thus high signal-to-noise ratio (SNR) can be gained.

Assuming the transmitted chirp signal is expressed as: $s(t) = \cos[\pi\alpha(t - t_D)^2], 0 \le t_D \le t \le t_D + t_{\rm TX} \le t_{\rm MAX}$. The received chirp signal SNR is given by $\rm SNR = 1/2N_0\alpha t_{TX}$,

where N_0 is the single-side band power spectral density of the noise, assuming a white noise power spectral density in $(-\alpha t_{\rm TX},\ \alpha t_{\rm TX})$ frequency range. Stretch processing can be expressed as

$$[s(t)+n(t)]\times\cos(\pi\alpha t^2),\quad 0\le t\le t_{\rm MAX}. \tag{2}$$

The signal content after filtering and stretch processing is given by $s'(t)=(\cos(\pi\alpha t_D^2-2\pi\alpha t_D t))/(2), t_D\le t\le t_D+t_{\rm TX}$. Its power can be calculated as $\mathrm{P_s}=t_{\rm TX}^2 16$ assuming αt_D is very large. After stretch processing, the noise part has the power of $\mathrm{P_n}$ expressed as $P_n{=}E|\int n(t)c(t)e^{-j\omega t}dt|^2$, where $\mathrm{E}(\cdot)$ denotes the mathematical expectation. By letting $\mathrm{c(t)}=\begin{cases}\cos(\pi\alpha t^2), & 0\le \mathrm{t}\le t_{\rm MAX}\\ 0, & \text{others}\end{cases}$, thus noise power can be calculated as

$$\begin{aligned}P_n&=\frac{N_0}{4\pi}\int_{-2\pi\alpha t_{\rm TX}}^{2\pi\alpha t_{\rm TX}}|C(j(\omega-\omega_1))|^2d\omega_1\\&\approx\frac{N_0}{4\pi}\int_{-2\pi\alpha t_{\rm TX}}^{2\pi\alpha t_{\rm TX}}|C(j\omega_1)|^2d\omega_1\end{aligned} \tag{3}$$

where $\mathrm{c(t)}=(1/2\pi)\int \mathrm{C(j\omega)e^{j}\omega t d\omega}$. If we consider $\mathrm{C(j\omega)}$ as the Fourier transform of $\mathrm{c(t)}$ from $0\sim t_{\rm TX}$, the frequency content never goes beyond $2\pi\alpha t_{\rm TX1}$. The above expression can be rearranged as: $P_n\approx(N_0/2)\int_{-\infty}^{\infty}|c(t)|^2dt=(N_0/2)(t_{\rm TX})/(2)$, and $\mathrm{SNR}=(t_{\rm TX}^2/16)/((N_0/2)(t_{\rm TX})/2)=(t_{\rm TX}/4N_0)$. The SNR improvement is given by $\Delta_{\rm SNR}=(t_{\rm TX}/4N_0)/(1/2N_0\alpha t_{\rm TX})=\alpha t_{\rm TX}^2/2$. Substituting RoC specification parameters into the above equation yields a 30 dB SNR improvement, which is verified by MATLAB simulation. Stretch processing with a chirp signal proves to offer a substantial performance boost over traditional processing.

III. Receiver With Stretch Processing

In order to provide a large dynamic range with improved linearity, a low-noise amplifier (LNA) is designed with an RF variable gain amplifier (VGA) prior to the mixer. The down-converted 1.72 GHz IF signal passes through an off-chip SAW filter that removes harmonics, image signals and LO leakages presented at the RF mixer output. In order to reduce the bandwidth with less power penalty, the stretch processing technique is implemented in the modified Weaver receiver, rather than the RF band.

A. Receiver Circuitry

The design of a low power, wide-band radar front-end is challenging because of the tradeoff between the noise figure and bandwidth performance [12]. A block diagram of the receiver RF and IF architectures are given in Fig. 2. The input stage of the LNA is a cascode common-emitter amplifier that is designed to simultaneously achieve both power and noise matching, as shown in Fig. 4(a). This radar receiver employs a reconfigurable front-end and the wideband front-end is designed for scanning the background. Once the target is identified, the receiver can be reconfigured to a narrow-band mode with increased sensitivity and anti-jamming capability, which are desired for tracking the targets. The receiver front-end has separate components, i.e., LNA, VGA, mixer and buffer, for the wide-band and narrow-band signal paths, which are connected at the SAW filter input. These two paths are switched via bias and controlled by the RCU. As shown in Fig. 5, the wideband LNA and narrowband LNA have simulated noise figures of 4.5 dB and 2.4 dB, respectively.

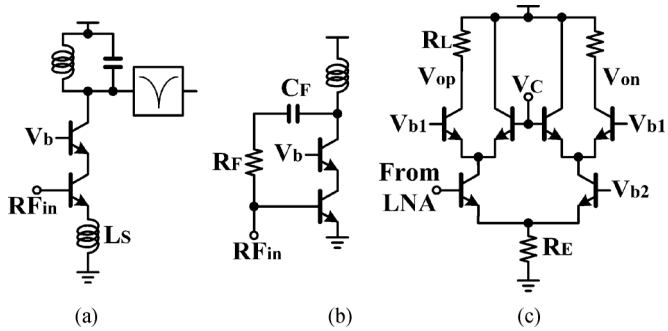

Fig. 4. Circuit schematic of the (a) narrowband LNA, (b) wideband LNA, and (c) RF VGA for single-to-differential converter.

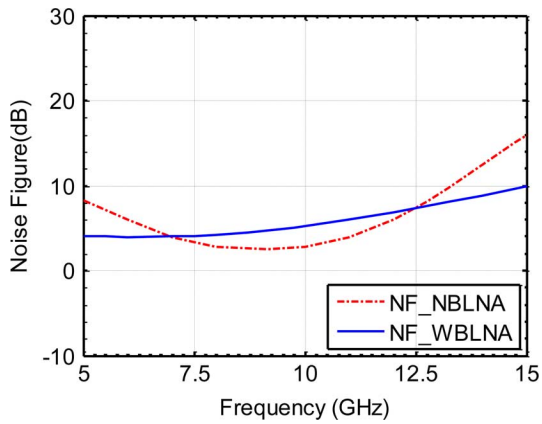

Fig. 5. Simulated noise figure of wideband LNA and narrowband LNA.

The RF VGA is a differential cascode amplifier with a current steering branch connected to the upper cascode transistors, as shown in Fig. 4(c). A pair of current steering transistors under the control signal $(\mathrm{V_{ctrl}})$ adjusts the current flowing to the load. Thus the gain of the RF VGA can be continuously tuned. Traditional Gilbert cells are used for both RF and IF mixers.

The modified Weaver receiver baseband architecture, including two-stage down-conversion mixers, two baseband LPFs, and an IQ signal combiner, is utilized to produce the image rejected baseband signal. The 7th-order Butterworth baseband filter is a widely tunable $\mathrm{g_m}$-C low-pass filter with a cutoff frequency tunable from 4 MHz to 54 MHz. Programmability is achieved by tuning the bias current of the transconductance cells, i.e., the $\mathrm{g_m}$ of each stage.

B. 12-Bit Time Interleaved Pipeline ADC

A 12-bit time interleaved pipeline ADC is used to digitize the single tone at the receiver output and extract the frequency information, namely the range to target. The pipelined ADC architecture has been proven to be very suitable for high-speed operation and high-resolution ADC converters. A time interleaved pipeline ADC structure is proposed in this design using an op-amp sharing technique to reduce the large power

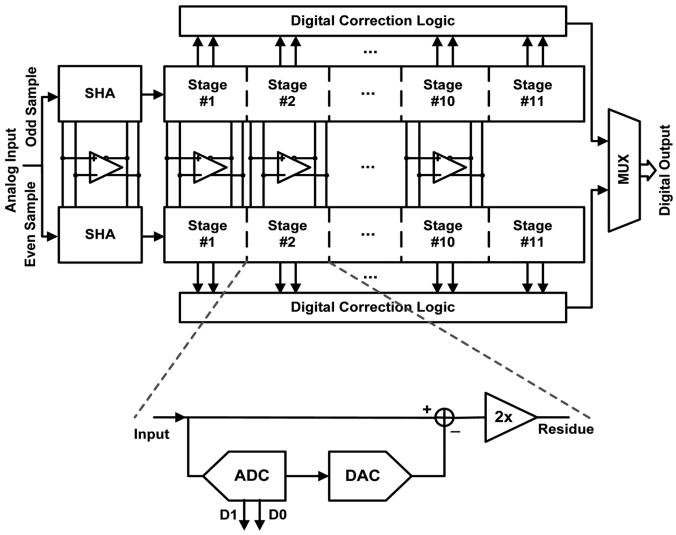

Fig. 6. Block diagram of the time interleaved pipeline ADC.

consumption from power hungry op-amps. The block diagram of the 12-bit time interleaved op-amp sharing pipeline ADC is shown in Fig. 6. It consists of two eleven-stage 1.5-bit/stage time-interleaved pipeline ADCs. One pipeline processes the even samples, while the other pipeline works on odd samples. For both pipeline ADC channels, two complementary clock phases are used to handle multiplying and sampling. However, the op-amp only works in the multiplying phase for every single channel, which is half of one complete clock cycle. Thus, both pipeline ADCs are capable of sharing their op-amps by only using the corresponding multiplying clock phase. This achieves a large power savings since the number of power hungry op-amps is cut in half. In addition, this also helps minimize offset and gain mismatches between pipelines that could degrade the ADC's performance. Each pipeline stage includes a flash sub-ADC, a sub-DAC, and a residue amplifier.

IV. DDS Based Chirp Transmitter

The transmitter consists of a quadrature DDS, two 5th-order Butterworth low-pass filters (LPFs) with tunable cut-off frequencies, an IF IQ modulator, an off-chip SAW filter, a transmitter variable gain amplifier (TX-VGA), a RF mixer with a notch filter and a RF pre-amplifier. In order to remove the harmonics and spurs, the chirp signals generated by the quadrature DDS are first filtered by the 5th-order Butterworth LPFs. Then the clean chirp signals are up-converted to a 1.72-GHz IF frequency by the IF IQ modulator. An off-chip SAW filter is employed to attenuate the LO leakage and other harmonics from the IF mixers. The TX-VGA amplifies the IF signal with a programmable gain from -16 dB to 12 dB and a step size of 4 dB. A notch filter is embedded in the RF mixer to provide attenuation for the image signals around 5.16 GHz. The transmitter finally transmits a clean chirp signal around 8.6 GHz.

A. Quadrature Direct Digital Synthesizer

A block diagram of the quadrature DDS architecture is given in Fig. 7. The quadrature DDS consists of a radar controller, a phase accumulator, a frequency accumulator, a phase modulator, a quadrature Coordinate Rotation Digital Computer (CORDIC) cell, inverse *sinc* filters and quadrature DACs. The high speed DAC implementation used in the DDS inherently applies a zero-order-hold (ZOH) operation on the output waveform. While the DDS generates a wide bandwidth "stretch" chirp signal that performs the stretch processing in the radar, it is important that the amplitude of the generated chirp not fluctuate with frequency. In order to achieve constant magnitude over the chirp bandwidth, an inverse *sinc* filter is designed to compensate the roll-off due to the structure of the DAC's ZOH transfer function. In the DDS, two FIR filters with 9-bit coefficient resolution, one for the I-path and the other for the Q-path, were implemented after the partial dynamic rotation (PDR) CORDIC. The phase to sinusoidal mapping function of the DDS uses the recently developed PDR CORDIC described below.

B. Partial Dynamic Rotation (PDR)CORDIC

The generalized CORDIC algorithm is able to calculate various nonlinear elementary functions by a series of vector rotations in circular, linear, and hyperbolic coordinate systems. Since the CORDIC algorithm can be implemented iteratively without involving multipliers, it is preferable for hardware logic implementation. Only the calculation of sine and cosine functions is of interest in DDS design. The vector rotation at the i-th iteration is given by $x_{i+1} = x_i - \sigma_i 2^{-i} y_i,\ y_{i+1} = y_i + \sigma_i 2^{-i} x_i, z_{i+1} = z_i - \sigma_i a_i$, where $\sigma_i = \mathrm{sign}(z_i)$ and $a_i = \tan^{-1}(2^{-i})$ represent the rotation direction and the rotation angle respectively. The CORDIC treats z_0 as a system input and its goal is to make z as close to 0 as possible through iterations. However, the non-ideal rotations in CORDIC increase the vector length and the i-th iteration increases the length by $k_i = (1)/(\cos a_i) = \sqrt{1 - 2^{-2i}}$. Therefore, after n iterations, the CORDIC will magnify the vector length by a factor of $K = \prod_{\mathrm{i}=0}^{\mathrm{n}-1} \mathrm{k_i}$, which approaches 1.64676026. . ., as the number of the iterations increases.

There are several major hindrances for high-speed CORDIC implementation with low area cost: 1) a great number of required rotations, 2) compensation of the scaling factor K, 3) carry propagation of adders, and 4) dependence of X and Y paths on the Z-path. In order to address these issues, a partial dynamic rotation (PDR)-CORDIC, illustrated in Fig. 8, is proposed. This architecture has a faster phase convergence speed than the conventional CORDIC while maintaining a constant scaling factor K. Thus it can be implemented with relatively low area overhead. In comparison with a conventional static stage, the extra hardware cost for a PDR-stage includes the dynamic rotation selection (DRS) logic and barrel shifters. The DRS logic finds the closest elementary rotation angle $\alpha \mathrm{j}$ from the set $\{\alpha_\mathrm{i}\}$ and passes j to the barrel shifter to perform programmable bit shifts on the X and Y paths. Such overhead is small compared to the benefits achieved by decreasing the number of rotations.

C. 12-Bit Current Steering DACs

Two fully differential, current steering 12-bit, 500 MHz CMOS DACs convert the digital output to an analog voltage. The DACs use a segmented architecture with 6 bits of thermometer coding for the MSB and 6-bits of binary coding for the

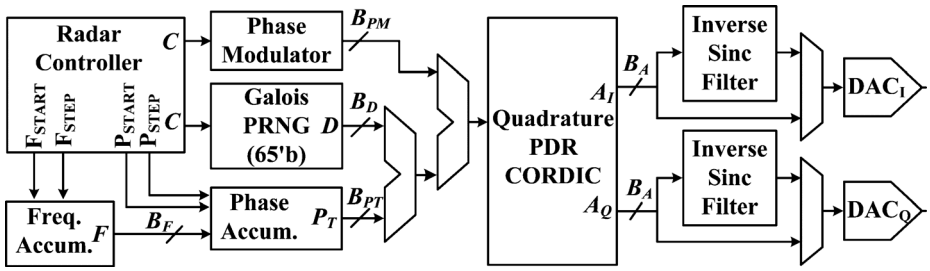

Fig. 7. Block diagram of the quadrature DDS.

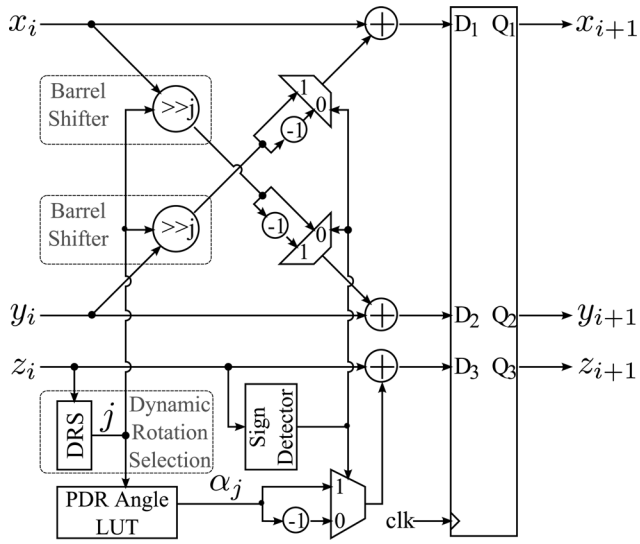

Fig. 8. Partial dynamic rotation (PDR)-CORDIC.

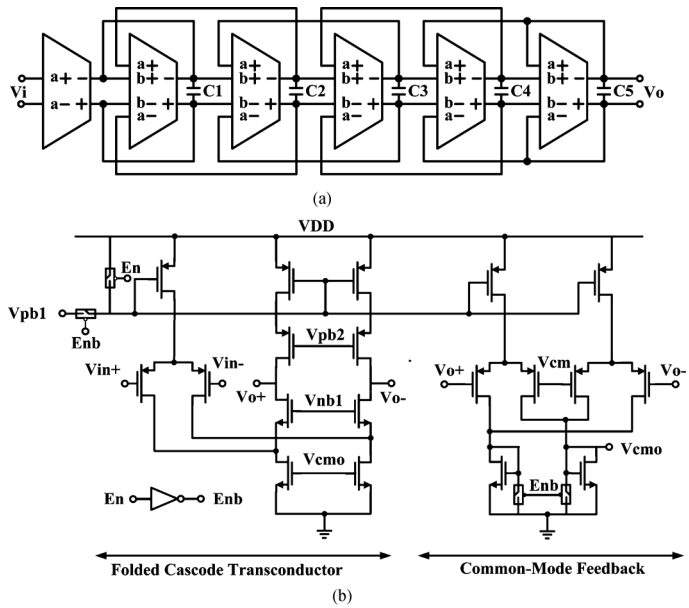

Fig. 9. (a) Fully differential 5th-order Butterworth filter and (b) schematic of the OTA cell.

LSB. The output of the DAC has 20 dB of digitally controlled, programmable gain. The gain is programmed by modifying the values of current reference. The DAC uses a triple-centroid switching scheme, which randomizes spurs due to current cell mismatch. The clock tree is a balanced H tree in an attempt to minimize clock skew along the wire paths. The SFDR of the DAC is approximately 55 dBc (better than 60 dBc at certain frequencies) through about two thirds of the Nyquist frequency.

D. 5th Order Butterworth Low-Pass Filter

The quadrature DDS generates harmonics and spurs at its output, and a low-pass filter is needed to remove them. In this application, a widely-tunable OTA-C low-pass filter with a cutoff frequency tunable from 23 MHz to 135 MHz is employed as shown in Fig. 9(a). The architecture of the filter is synthesized with the 5th-order low-pass Butterworth ladder prototype.

For OTA-C filter design, constant g_m topology usually exhibits large power consumption because the g_m must be high enough to satisfy the highest cutoff frequency requirement. In addition, a constant g_m topology requires the filter to meet the noise budget at the highest frequency, because the noise from the OTA cell is constant, and the smallest capacitor determines the overall noise performance of the filter. A large capacitor is required if low noise performance is needed. On the other hand, the constant C topology experiences the same noise performance over the tuning range. Therefore, a constant C topology is employed in this filter In order to make the g_m value tunable, binary-weighted unit g_m cells are adopted. Programmability is achieved by switching unit OTA cells on and off. Since the input and output swing of the filter need not be very large, a simple fully differential folded-cascode amplifier with common-mode feedback is used for the unit g_m cell, as shown in Fig. 9(b).

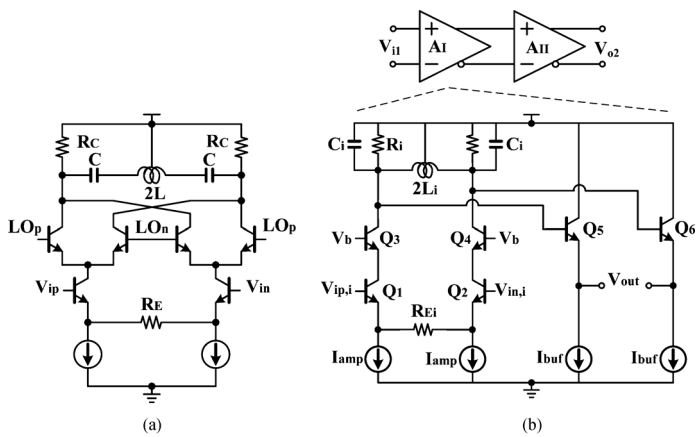

Fig. 10. Simplified schematic of (a) the RF mixer with notch filter and (b) RF pre-amplifier.

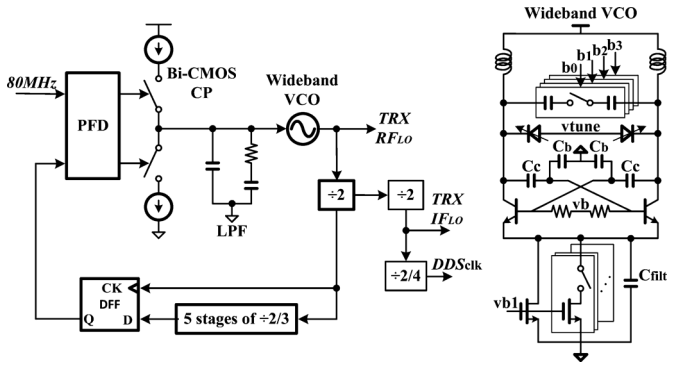

Fig. 11. Block diagram of the proposed PLL system and schematic of wideband VCO.

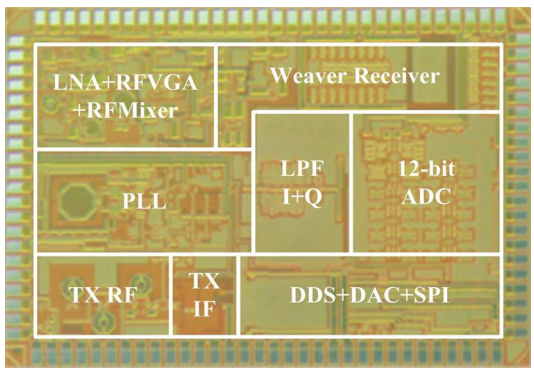

Fig. 12. Die photo of the proposed chirp radar IC.

E. RF Mixer and Pre-Amplifier

The RF mixer further up-converts the IF signal to an 8.6 GHz RF signal. In order to suppress the image signal, a notch filter was proposed and added to the mixer. As shown in Fig. 10(a), the notch filter is implemented with a series LC tank in parallel with the load resistor R_C. The resonant frequency of the LC tank is tuned to the image frequency. The spectrum of the RF mixer output contains the LO signal tone and the harmonics of the RF signal. In order to attenuate these undesired tones, a band-pass filter formed by the LC tank and its associated parallel resistor R_C is achieved within a two-stage pre-amplifier, as shown in Fig. 10(b).

V. Phase-Locked Loop

In the proposed radar transceiver, an integer-N PLL consisting of a wideband VCO, a divide-by-two cell (DTC), a multi-modulus-divider (MMD), a phase-frequency detector (PFD) and a charge pump (CP), as well as divider modules were used to generate clocks and LO signal for mixers, DDS, ADC and a digital interface. As shown in Fig. 11, the output of the VCO is first divided by 2 before being fed into the MMD in order to relax the time requirement. Five stages of the divide-by-2/3 cell are used to achieve a divide ratio from 32 to 63.

A multi-band VCO, with a 4-bit MIM capacitor array and a tunable current tail, is adopted to provide a wide tuning range as well as low phase noise performance. Fig. 11 presents the proposed bipolar NPN cross-coupled VCO. The frequency tuning range is simulated with an 18% increase. A noise filtering MIM capacitor is used to reduce the noise up-conversion from the current tail and the simulated improvement is 3.5 dB.

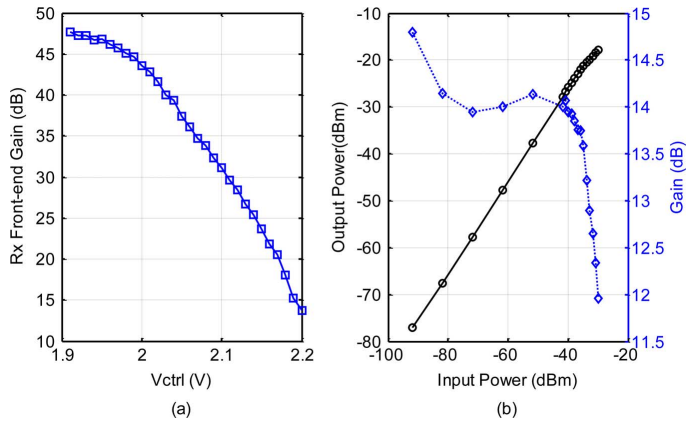

Fig. 13. (a) Measured narrowband receiver front end gain vs. the VGA Vctrl. (b) measured P1 dB and gain of Rx front-end.

In order to avoid breakdown, the bias voltage $\mathrm{V_b}$ as shown in Fig. 11 should be large. However, a large $\mathrm{V_b}$ will force the bipolar transistor into the saturation region, which is not desirable since the VCO phase noise will be degraded in this operating region. The following conditions should be met to maintain the largest signal swing for best phase noise and avoid breakdown:

$$\begin{cases} vb < V_{\mathrm{DD}} - (1+n)A_{\mathrm{VCO}} - V_{\mathrm{margin}} \\ vb > V_{\mathrm{DD}} + (1+n)A_{\mathrm{VCO}} + V_{\mathrm{th}} - V_{\mathrm{ceo}} \text{ breakdown} \end{cases} \quad (4)$$

where the voltage divider ratio $n = C_C/(C_C + C_b)$ is introduced to alleviate the requirement of breakdown voltage. $\mathrm{A_{vco}}$ is the single-ended VCO signal amplitude. $\mathrm{V_{margin}} = 0.2$ V and $\mathrm{V_{th}} = 0.5$ V are the voltage margin from saturation and threshold voltage of the bipolar transistor, respectively. As known, the larger the voltage divider ratio n, the better the phase noise. To prevent breakdown, $n = 2/3$ is chosen and the maximum differential signal amplitude A_{VCO} is thus 0.54 V.

VI. Implementation and Measured Results

The proposed chirp radar transceiver prototype chip was implemented in a 0.13 μm SiGe BiCMOS technology. Fig. 12 shows the die photo of the radar transceiver MMIC. This radar-on-chip transceiver was operated and tested with an extensive custom test fixture including a dedicated printed circuit board (PCB), and a digital control system, consisting of FPGA modules supported by a custom PC interface developed in Python.

Fig. 13(a) shows the measured receiver front end gain vs. the $\mathrm{V_{ctrl}}$ voltage. The gain tuning has the maximum gain of 47.7 dB, and its dynamic range is 34 dB. The gain control curve is saturated at the low control voltage. Fig. 13(b) shows the measured P1 dB of the receiver front-end. The input P1 dB is -35 dBm. The chirp radar receiver is also measured through a 1.8 GHz single-tone test signal applied to the IF circuit input, and the quadrature chirp signals from 27.5 to 30.9 MHz generated from the transmitter baseband. The chirp signal at

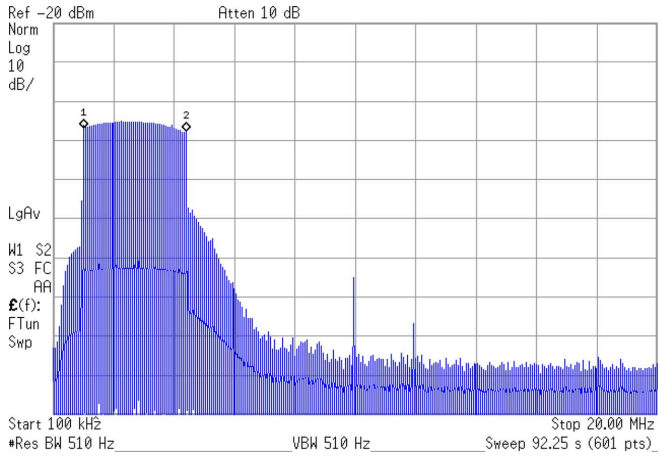

Fig. 14. Measured chirp spectrum at the Rx BB output.

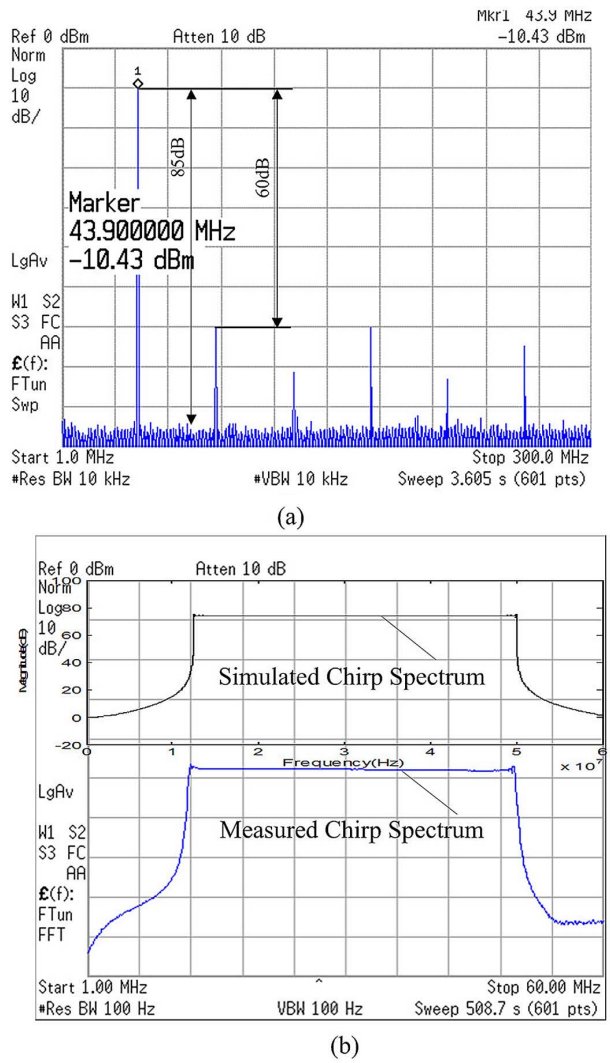

Fig. 15. (a) Measured DDS output spectrum showing a SFDR of 60 dBc ($\mathrm{Fclk} = 500$ MHz), and (b) measured and simulated chirp spectra at DDS output (12.5–50 MHz).

the receiver output is from 1.1 to 4.5 MHz. Fig. 14 shows the measured spectrum of the chirp signal at the receiver baseband output.

TABLE I
PERFORMANCE COMPARISON OF X-BAND RADAR TRANSCEIVER MMICS

Literature	[2]	[5]	[9]	This work
Technology	0.18μm CMOS	0.25μm CMOS	0.18μm SiGe BiCMOS	0.13μm SiGe BiCMOS
Frequency(GHz)	10.5	8.5~11	6~18	8-9
Area (mm^2)	2.6×3.3	1.8×1.5	2.2×2.45	3.5×2.5
Supply Voltage (V)	N/A	5	3.3	2.2/1.5 (analog/digital)
Power (mW)	350	315/350(Rx/Tx)	330~660(Rx)	326/333 (Rx/Tx)
VCO PN (dBc/Hz)	-93@1MHz	-77@10kHz	N/A	-114@1MHz
Rx FE Gain (dB)	-4.5	N/A	1.5~24.5	10.7~44.7
Rx FE Input P1dB(dBm)	-29	-11	N/A	-35
DDS SFDR(dBc)	N/A	N/A	N/A	-60
Tx BB Filter BW(MHz)	N/A	N/A	N/A	18~135
Rx BB Filter BW(MHz)	N/A	N/A	N/A	4~54

Fig. 15 illustrates the measured output spectrum of the quadrature DDS with a clock frequency of 500 MHz. The generated single-tone signal has a frequency of 43.9 MHz. Although the spur changes with output frequency, the spur level is 60 dB below the signal power. Fig. 15 also shows the comparison between simulated and measured chirp spectrums ranging from 12.5 MHz to 50 MHz at the DDS output. The measured chirp spectrum is consistent with the simulation results. An inverse sinc filter is implemented in the DDS to maintain the constant amplitude of the generated chirp over the entire frequency band. To test the filters, a 90 MHz sweep with the clock frequency at 200 MHz was generated using the DDS. With the inverse sinc filter enabled, the measured chirp magnitude variation across the spectrum is reduced from 2.77 dB to 0.21 dB.

Fig. 16(a) shows the measured transfer curves of the 5th-order Butterworth low-pass filter under all combinations of the 3-bit bandwidth control word. The DC gain is -6 dB and the gain rolls off at -100 dB/decade above the cutoff frequency, which is adequate to attenuate the harmonics at the DDS output if the start frequency is properly selected. Fig. 16(b) depicts the simulated and measured curves of filter bandwidth vs. bandwidth control word. A linearly controlled bandwidth has been obtained from 18 MHz to 135 MHz in measurement, compared to the bandwidth from 22.5 MHz to 180 MHz in simulation. The bandwidth reduction might be caused by the parasitic capacitance, OTA gain loss and the process variation in the MIM capacitor value. This filter has achieved good linearity. As shown in Fig. 16(c), the measured IIP3 is 4.9 dBm. Fig. 17 depicts the measured spectrum of the transmitter output. The transmitted chirp ranges from 8.65 GHz to 8.665 GHz. The chirp signal was up-converted from the DDS output with the start- and stop-frequencies of 62 MHz and 77 MHz, respectively.

As shown in Fig. 18, the measured phase noise of the PLL is -86 dBc/Hz and -114 dBc/Hz@10 kHz and 1 MHz offset with a center frequency of 6.56 GHz, respectively. The measured VCO tuning range is shown in Fig. 19. The overall frequency tuning range is around 34% and the VCO tuning gain is around 350 MHz/V. Table I summarizes the performance comparison of the X-band transceiver MMICs. The prototype chirp

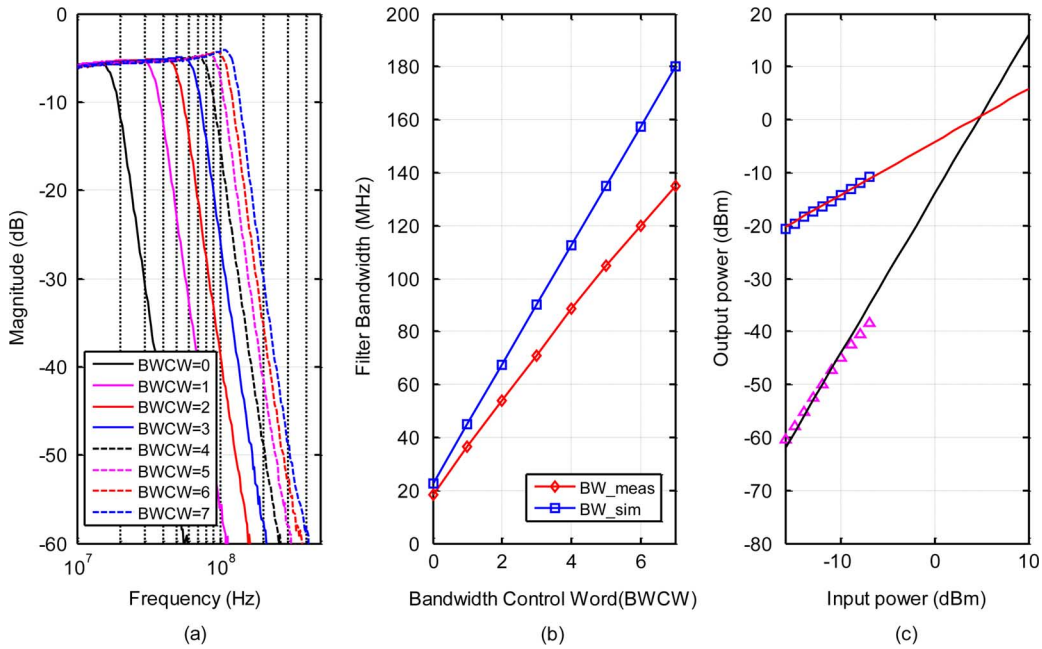

Fig. 16. (a) Measured transfer curves, (b) comparison between simulated and measured filter bandwidth vs. control word (BWCW) and (c) measured IIP3 of the 5th-order Butterworth LPF.

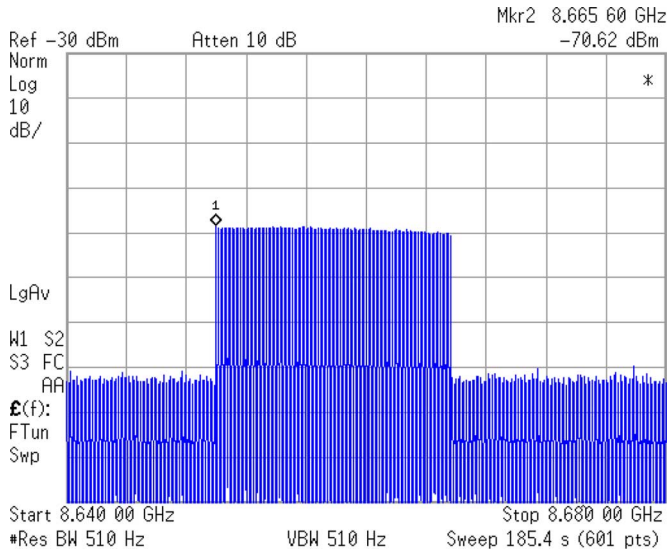

Fig. 17. Measured spectrum of the chirp radar transmitter RF output.

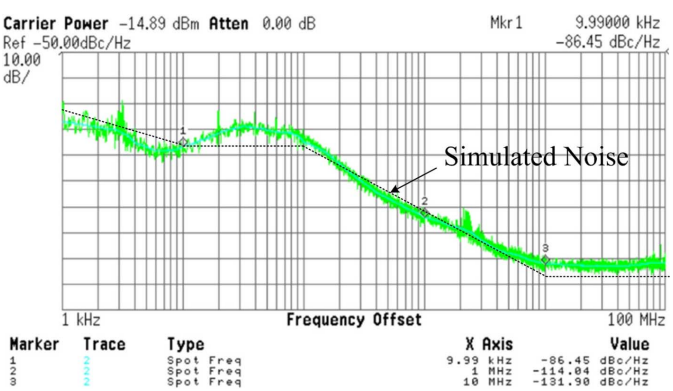

Fig. 18. Measured and simulated phase noise of PLL with BW = 100 kHz, Fref = 80 MHz.

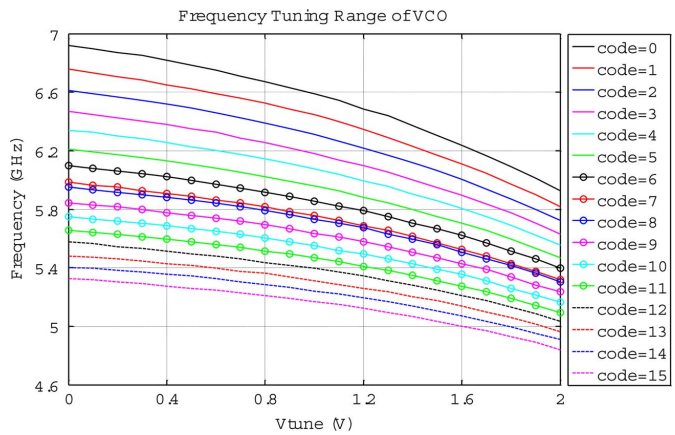

Fig. 19. Measured VCO frequency tuning curves versus the tuning voltage Vtune and the 4-bit band selection code.

radar transceiver occupied a die area of 3.5×2.5 mm^2 and it consumes a power of 333 mW and 326 mW under TX mode and RX mode, respectively.

VII. Conclusion

This paper has presented an X-band chirp radar transceiver implemented in a 0.13 μm SiGe BiCMOS technology. The proposed radar transceiver employed a stretch processing technique to reduce the receiver bandwidth and thus lower the sample rate and power of the ADC. Stretch processing was implemented in the receiver baseband within a modified Weaver architecture. The radar-on-chip (RoC) MMIC occupied a die area of 3.5×2.5 mm^2, and consumes 326 mW in the receive mode and 333 mW in the transmit mode, respectively.

Acknowledgment

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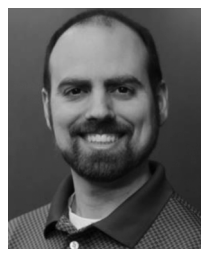

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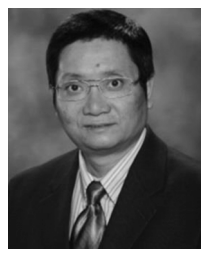

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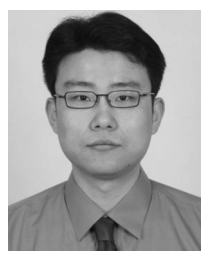

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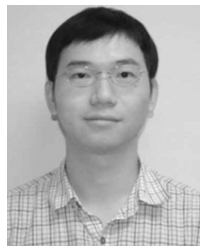

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