University of California
Santa Barbara

Collective Pulse Dynamics: A New Timing Circuit Strategy

A dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

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September 2018

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Dedicated to my Parents and Niharika

Acknowledgements

I would like to acknowledge my mentor, Prof. Forrest Brewer for daily discussions and guidance about my research. I would also like to acknowledge Prof. Jim Buckwalter for his support and belief in my research. His objective opinion and guidance helped me a lot throughout my research. Also I would like to acknowledge my committee members Prof. Luke Theogarajan and Prof. Tim Sherwood for their continuous support and guidance. In particular I would like to acknowledge Dr. Merritt Miller for his guidance and patience in explaining me this area of work. Members of Prof. Brewer and Prof. Buckwalter's lab groups for their support throughout my work. Particularly I would like to acknowledge Prashansa Mukim for her help and collaboration in the research.

I would like to acknowledge Prof. Joe Incandela for support during this research. Also, I would like to acknowledge the ARPA-E research grant and Prof. Buckwalter and Prof. Clint Schow for helping me with it for my research.

I thank my parents, Niharika, my sister and Pratyush to help me through this endeavour.

Curriculum Vitæ

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Publications

- **A.Dalakoti**, M.Miller, and F. Brewer: Pulse Ring Oscillator Tuning via Pulse Dynamics, IEEE ICCD 2017
- M.Miller, **A.Dalakoti**, P.Mukim, and F. Brewer: Low Phase Noise Pulse Rotary Wave Voltage Controlled Oscillator, IEEE ISOCC 2017
- **A.Dalakoti**, M.Miller, and F. Brewer: Design and Analysis of High Performance Pulse Ring VCO, IEEE NorCAS 2017
- **A.Dalakoti**, M.Miller, and F. Brewer: High Performance Pulse Ring Voltage Controlled Oscillator for Internet of Things, IEEE ISOCC 2017
- M.Miller, C.Segal, D.McCarthy, **A.Dalakoti**, P.Mukim and F. Brewer: Impolite High Speed Interfaces with Asynchronous Pulse Logic, IEEE GLSVLSI 2018
- **A.Dalakoti**, C.Segal, M.Miller, and F. Brewer: Asynchronous High Speed Serial Links Analysis using Integrated Charge for Event Detection, IEEE GLSVLSI 2016
- C.Segal, **A.Dalakoti**, M.Miller, and F. Brewer: Connectivity Effects on Energy and Area for Neuromorphic System with High Speed Asynchronous Pulse Mode Links, IEEE SLIP 2016
- A.Nishad, **A.Dalakoti**, A.Jindal, R.Kumar, and R.Sharma : Analytical Model for Inverter Design using Floating Gate Graphene Field Effect Transistors : ISVLSI 2014

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Abstract

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This work presents a novel CMOS behavior of self stabilization of ring oscillators using collective dynamics. It shows that phase error correction can occur in ring oscillators over multiple cycles without an external reference via the collective dynamics of pulses. In time domain this shows up as timing stability improvement in oscillators. Different timing stability metrics were analyzed to determine the correct methodology to analyze this stability improvement. Behavioral models were made to capture the effects of local dynamics and its collective effects. These models were shown to have a good correlation with the HSPICE circuit simulations and measured values.

Multiple oscillator topologies and architectures were fabricated to test the model, behavior and subsequent analysis. Different pulse amplifier based ring oscillators show trends similar to that predicted by simulations and empirical relationships developed using behavioral simulations. Further transmission line stabilized traveling wave version of the pulse oscillators show a higher stability improvement.

This work opens up a new design space in the timing circuits design where all the other conventional tricks are still applicable. It also opens up an application space due to the timing stability improvement in the order of 1000 cycles where conventional ADC's and TDC's work. Finally this work eases up the constraints of loop filter and source phase noise when oscillators are operated in a phase locked loop.

Contents

Chapter 1

Introduction

Timing Circuits are an essential and universal component of any CMOS design. Their applications range from microprocessors [2] to high precision Radio Frequency (RF) Circuits[3]. All the applications bring with them their own set of design constraints. In digital clocking applications, the total uncertainty of timing of an output event (e.g. the millionth rising edge) relative to an ideal time source is the most important quality factor for a local oscillator. Distribution of high frequency, low jitter timing over long distances is costly, motivating small localized synchronizing oscillators that maintain some global phase relation. Also, in applications like TDC's [4] [5], ADC's [6] [7] etc., phase stability improvement in an essential parameter. This work provides a novel methodology and implementation to improve the timing stability in CMOS oscillators. Self stabilization using collective dynamics of pulses traversing a ring of gates is shown to occur in CMOS oscillators for first time. It also develops a analysis methodology for designing such circuits. It also analyses existing timing stability measurements and then picks the one best suited for this application. In doing so, it brings forth the use of a technique (allan deviation [8] [9]) generally used for long time scale analysis, to analyze short term and self stabilization behaviors.

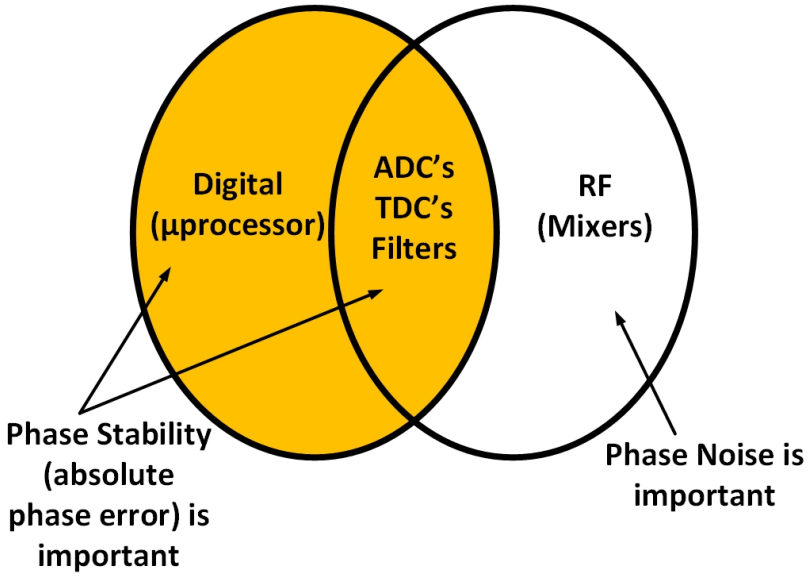


Figure 1.1: Application of Timing Circuits and Voltage Controlled Oscillators

1.1 Thesis Statement

Timing stability of free running ring oscillators is constrained to minimization of single cycle noise reduction. Pulse gates have predictable and controllable delay variations leading to different dynamical behaviors. We propose that the collective dynamics of pulse gates can be exploited to improve timing stability of free running ring oscillators. The analysis based on just the collective effects of local gate dynamics predicts the timing stability improvement. It opens a new design space of dynamical oscillators.

1.2 Background

The fundamental problem in the work was to analyze and determine the reasoning behind anomalous (good) timing properties of pulse based asynchronous circuits as observed in [1] and as shown in Figure 1.2. It was noted there that self timed asynchronous circuits with such high accuracy timing were not possible without special considerations,

none of which were made in the work.

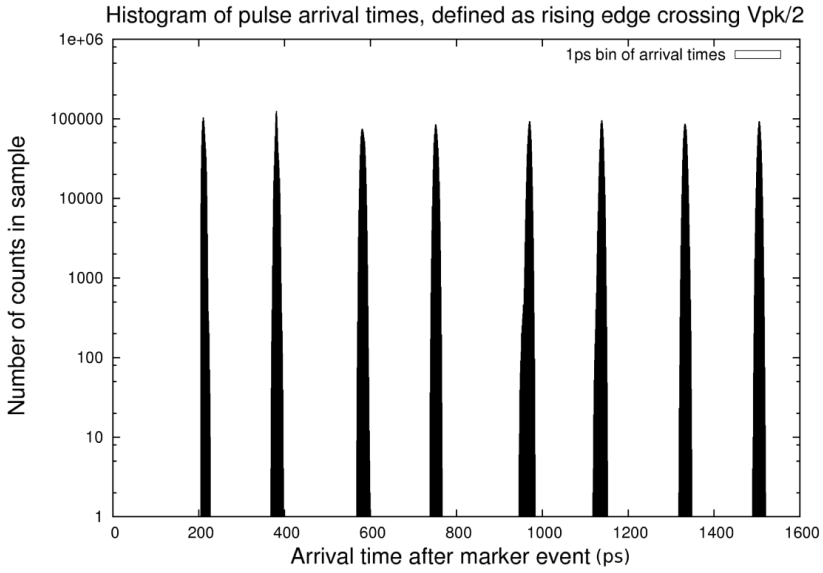


Figure 1.2: From [1] : Log scale pulse arrival time plot for 8 bit data. No counts are seen more than +/-20pSec from the nominal

In-order to understand the timing behavior of pulse based circuits, the most fundamental timing circuit (ring oscillators) was constructed. The measured values of such free running pulse ring oscillators without any kind of voltage controller on chip were far superior to any other reported for such a huge tuning range. Also, the timing stability of such oscillators was seen to be superior to those generally observed by ring oscillators. Measurements done in the frequency domain depicted an anomalous self locking behavior at low frequency cut-offs. This resulted in development of analysis methodology which included the effects of delay variations in ring oscillator timing stability.

1.3 Methodology

In-order to understand such anomalous properties in the circuits, a ground up framework was established from the fundamentals. Dynamics in the asynchronous events in a

ring were reported in [10] but no practical use or application was formulated for them. It was then reported through this work in [11] that such dynamics can be used to improve the phase errors and timing stability properties of oscillators. To further explore the anomalous behaviors in the oscillators, multiple approaches were taken as shown in Figure 1.3. Dynamics were used to predict the behaviors and an empirical relationship was developed. Some points in these relationship were validated using bench measurements and HSPICE simulations. Further, short term timing stability using metrics like Allan deviation were explored due to the inability of current frequency domains analysis to fully represent the problem.

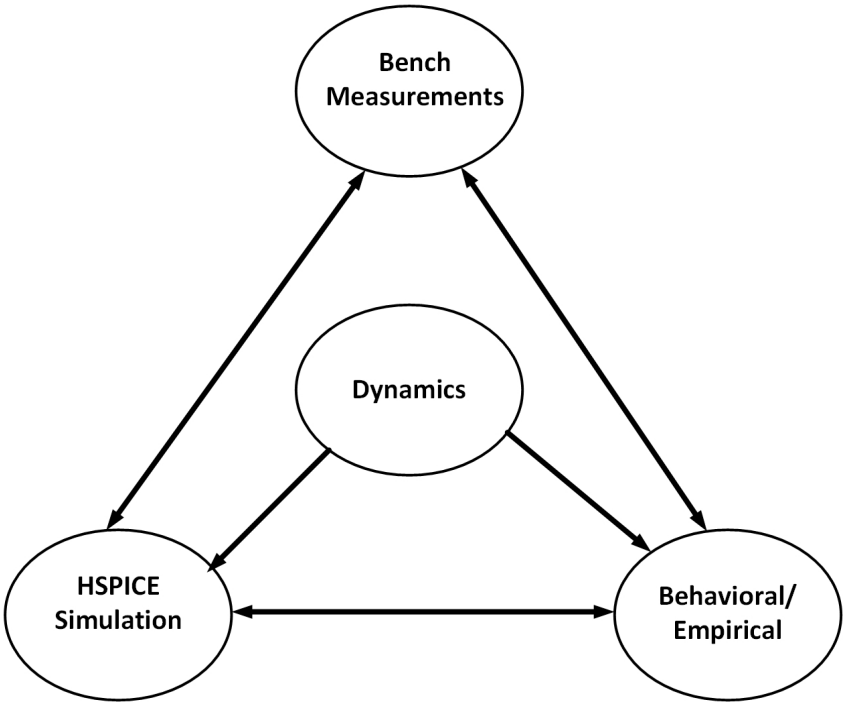


Figure 1.3: Analysis Methodology

1.4 Literature Survey

First, a brief overview of the oscillator timing models and conventional methodologies is presented.

1.4.1 Models for timing analysis of oscillators

Analysis of timing jitter was done in [12] and [13]. Phase noise based on linear time invariant model was analyzed in [14]. Impulse Sensitivity functions(ISF) was proposed as a method to analyze and predict phase noise in CMOS ring oscillators [15]. Effects of phase and amplitude perturbations were combined in the model proposed in [16].

1.4.2 Timing Stability Improvement Methodologies

Phase noise is dependent on the noise to signal ratio [17], which is given by Equation 1.1, where $\frac{N}{S}$ is the noise to signal ratio, ω is oscillator frequency, Q is the quality factor of the resonator used in the circuit implementation, P_{diss} is the oscillator power consumption.

$$\frac{N}{S} = \frac{\omega \kappa T}{Q P_{diss}} \tag{1.1}$$

Circuits primarily analyzed in this work are without resonators (due to large area footprint of resonating topologies). Fundamentally, Equation 1.1 leaves only P_{diss} as the design parameter for an oscillator operating at a given frequency and temperature. Further, if a conventional metric of phase noise per unit power is used as a figure of merritt, than it would seem that there isn't any design improvement possible. But, it is known from abundant literature on ring oscillator design that phase noise improvement is possible for a given power specification. The main concept behind these developments has been the idea to use power in a circuit only where it is needed. To this end, *ISF* and a

time variant model of phase noise was proposed in [15]. Main idea behind the work was that not all noise injected in an oscillator cycle is equally important. So, if higher power is spent in the region of oscillator phase where it is more susceptible to noise to phase error conversion, instantaneous signal to noise ratio will be better, hence a better phase noise for given power. Root mean square of time variant impulse sensitivity function was shown to be an effective measure and indicator of phase noise. So, higher slope transitions in an oscillator would result in better phase noise as it would decrease the root mean square value of ISF. ISF model works under the assumption that amplitude errors do not result in a significant phase error.

[16] showed an analysis which incorporated phase noise resulting from both amplitude and phase errors. Oscillators are generally constructed using saturating and/or limiting amplifiers so that amplitude to phase error is an insignificant number in the overall analysis. Since it is the effective ratio of noise and signal currents at a given node during the timing transition which results in phase error primarily, further power reduction was achieved by lowering the signal swing. This dictates the use of limiting amplifiers in the oscillator. Also, this necessitates that a full swing buffer be added to the oscillator output to connect it to any logic.

Transistor sizing for optimal phase noise at a given power has been analyzed in-depth[14][18]. Increasing the transistor width, increases the current at a node, which improves phase noise. However, this has an upper limitation on it, since it is hard to get high current densities locally (due to interconnect losses and high local losses causing temperature variations). Spatial coupling was presented as means of tackling this issue in [19] and further implemented in a larger system in. Class-C power amplifiers were used with LC tanks in [20] and [21], which effectively reduced the root mean square ISF. Longer time coupling and memory effects were explored in [22] using N-path filtering, but it imposed extra power and area constraints.

Circuit sensitivity and noise are technology dependent. Increasing current to improve phase noise effectively does not improve the phase noise per unit power metric. Also, current cannot be increased indefinitely due to current density constraints. This has limited the design space of ring oscillators. Generally, ring oscillators trail their traveling wave and LC counter parts by a factor of $\approx 20dB$. Since ring oscillators offer huge advantages in terms of area footprint of oscillators, it is worth exploring possibility of new design parameters to further improve phase noise and make them comparable to the ones with resonators, while still maintaining small area footprints. Also, LC oscillators at high frequency in scaled technologies is hard due to inductor Q limitations at high frequencies. In case of flicker noise sources, not many techniques are available to minimize it. Fundamentally, oscillators with small duty cycles are less prone to flicker noise as shown in [23], [24]. This condition works in favour of work discussed here as well. Also, to minimize flicker upconversion the ISF function should have a minimum possible DC component as shown in [15]. This condition goes against the work discussed in this thesis. Copy and cancel techniques are known no minimize flicker. Apart from this, flicker noise region is primarily avoided using some kind of phase locking [25] or delay locking as in case of multiplying DLL [26]. Any phase or delay locking technique has a trade off between VCO flicker and jitter and source flicker setting a condition on loop filter cut off frequency.

1.4.3 Possibilities of Improvement

In general in free running oscillators, it is assumed that any phase error persists indefinitely in time due to their periodic nature. None of the analytical tools and models incorporate the possibility of phase error correction over multiple cycles. Possibility of such a phenomenon has been slightly explored [27] where the phase noise metric was

established using a steady state ISF. All known methodologies effectively work because all you can do is average the white noise. The more you average the better results you get. This has a point of diminishing returns due to all the reasons explained earlier. Further, these techniques work little in the pink noise dominated regions.

Phase locked loops work with the assumption of a good source correcting phase errors in the loop at some very long time scales. The long time scale is necessary to ensure that the negative feedback loop is stable under a given gain and loop latency. Theoretically it is possible that a free running oscillator can be locked to its own median/mean time. This would be noticeably different than the techniques mentioned before since a phase locked loop implements a high pass filter on oscillator noise. But it is not possible to do such an implementation because of two reasons.First, classical inverter and/or operational amplifier based ring oscillators have no mechanism of low latency feedback and high gain error correction. Second, the timescales of these correction need to be relatively high frequency. This is because longer the comparison time, more is the timing uncertainty build up and more noise in the locking mean/median signal itself, defeating the whole purpose of doing it in the first place.

1.5 A New Design Space

Dynamical interaction between different asynchronous events in a ring was observed in [10]. This reported interactions were phase modifications in the timing scale less than ring periods. No reasoning was reported for the existence of such dynamics nor was it shown to improve any particular ring timing characteristic. Gate level timing characteristics were shown to be the cause of these dynamics during the course of this thesis in [11]. Further it was shown that these dynamics can be used to improve the timing uncertainty in pulse ring oscillators.

This thesis aims to show that collective dynamics of gates can be used to improve the timing stability of oscillators. It explores the reasons for such dynamics and ways to reliably modify them. It then proves that existence of such dynamics (under some constraints) is sufficient for increased stability of oscillators. The increased stability resembles that of a phase locked oscillator upto 100's of oscillator cycles.

1.5.1 Why Pulse?

Pulse (specifically those triggered by self resetting pulse gates in [28]) as a medium of communicating timing in ring oscillators offer some inherent advantages due to their rising edge based timing. This was further explored and shown to lower the ISF during the course of this work in [29]. Pulses offer the advantage of having lower flicker noise build up due to their minimal on time of transistors [24]. Further, pulses retain good timing properties with voltage scaling to near threshold limits giving oscillators a huge tuning range just based on supply itself as shown in [29]. The primary focus of this work in on the ease of manipulation of dynamics using pulse gates, which results in programmable dynamics for the use of high gain, low latency negative feedback loops in pulse ring oscillators. In-order for pulses to have reliable dynamics it is essential that pulses maintain shape. The pulse gates used in this work ensure that pulses have largely same shape. This ensures that any dynamics in the gates are independent of the pulse shape.

1.5.2 Visualization Metric

A number of timing stability metrics are available in the literature [30]. Use of standard deviation is only applicable in White Noise case since it does not converge in other cases like Flicker. Due to the low latency feedback from pulse dynamics, use of

frequency domain techniques is problematic in this work. Translation between time and frequency domain causes causality issues to show up due to the finite bandwidth of the translation. This results in incorrect interpretation of the results.

The dynamics explored in [11], when put into a loop result in global timing stability improvement. The collective dynamics from a ring oscillator results in timing stability improvement over multiple cycles. The metric should be able to convey change in stability over different timescales in the oscillator. It should also be able to distinguish different regions of timing stability improvement. Allan deviation proposed in [30] does both these things and hence was used for visualization of different timing characteristics of the researched oscillators.

1.6 Complementary Nature of Work

The ring oscillators designed in this work present a design strategy which is complementary to all the known strategies in the literature. The strategy described aims at improving the stability of oscillators over multiple cycles similar to that of a PLL (without the need of an explicit external reference). All conventional techniques can still be used to minimize the initial timing stability. To prove that conventional techniques are still applicable multiple oscillator architectures were designed and fabricated. Some of them are :

- Traveling Pulse Oscillator: Increased stability of the oscillator was achieved by the use of Transmission line in parallel with the gates.
- Spatial Coupling was tested by the use of cross linking the oscillators.

Other methods such as change in supply to result in change of noise averaging also pointed to the same results.

1.7 Future Research and Application

The timing stability strategy proposed and implemented in this work opens up the possibility of many research applications like:

- Analog to Digital Converter
- Time to Digital Converter
- N-Path Filters

It also opens the possibility of further research in the areas like:

- Multi Timescale Noise Analysis and Mitigation
- Multi Timescale feedback
- Injection locked multi oscillator system

1.8 Thesis Organization

Chapter 2 presents integrated charge as a detectivity metric in CMOS amplifiers and analyzes serial link performance using it. Chapter 3 explains the origination of gate level dynamics and how they can be modified to improve timing stability. Chapter 4 explains timing stability measurement and simulation techniques. Chapter 5 develops a behavioral and empirical model for the system being analyzed. It shows the collective dynamics of pulse gate in a loop is sufficient to create timing stability improvement. Chapter 6 explains pulse ring oscillator design and analyzes it with conventional metrics. Chapter 7 explains the traveling wave implementation of the pulse oscillator. Chapter 8 analyses the results of oscillator presented in chapter 6 and 7 and compares them with the timing stability improvement seen from simulations techniques. Finally, chapter 9

details the new possibilities of research and applications opened up for future work as a direct consequence of this research. It also looks into some open ended questions based on observations made during this research.

1.9 Permissions and Attributions

The contents of chapter 2 was co-authored with Forrest Brewer and was presented at and published in the proceedings of the 2016 GLSVLSI, Boston conference under the title Asynchronous High Speed Serial Links Analysis using Integrated Charge for Event Detection. The contents of chapter 3 were presented and published in the proceedings of the 2017 ICCD, Boston under the title Pulse Ring Oscillator Tuning via Pulse Dynamics. The contents of chapter 6 were presented and published in the proceedings of the 2017 NorCAS, Linkoping under the title Design and Analysis of High Performance Pulse Ring VCO. The contents of chapter 4, 7 and 8 are currently pending review. The materials are used under the terms of the IEEE author re-use policy allowing primary author re-use in subsequent work.

Chapter 2

Integrated Charge for Detection

2.1 Introduction

High speed serial links are commonly used in digital systems to move data between physically separated functional units. Serial links are attractive, because a single bit stream is easy to route and synchronize. High bit-rate links require low-jitter clocks and accurate clock-data recovery. Inevitably, the time base (clock) used to transmit the serial signal and the natural time base of the receiving circuit drift relative to each other. The circuits that compensate for this can be synchronous to, at most, one of the two time domains, giving rise to the use of asynchronous state-machines to handle the transition (phase alligners, FIFOs, bus arbiters, etc). Effectively, asynchronous machines are used in transmission regardless of whether the data is synchronous to a local clock. Thus, signaling methods that are naturally compatible with asynchronous logic become a promising subject of investigation. Asynchronous link design has been the subject of a number of recent studies [31], [32], [33]. Traditional asynchronous protocols are limited in speed due to the need to acknowledge data [32],[34]. In [35] asynchronous protocols share data lines, but performance depends on wire delays. In this work, we target (impolite)

asynchronous links that do not use handshaking such as [28]. This subset of links lacks the feed-back bottle-neck allowing link time-of-flight to be longer than a bit transfer. The critical point of this model is that timing (arrival) of each bit must be unambiguous despite the unknown arrival time and the guarantee of this feature is designed into the system with margins. Signal integrity analysis is thus critical to determining if such a link has sufficient margins to meet the standards of unambiguous reception.

We introduce an integral charge model as a detection and analysis metric. The metric has the advantage that it mimics the behavior of CMOS transistors, which by nature accumulate charge and act when a threshold is reached. This metric is used to examine a variety of link signaling strategies and compare the suitability of the strategies in terms of noise, bandwidth, and practicality on realistic media models such as inexpensive coaxial cable and PCB transmission lines. For a signaling pulse, the critical measure becomes the integral of the pulse shape, rather than its amplitude or duration. Detection of edges, by contrast, is achieved by integrating a voltage level and subsequently integrating a new level leading to both *setup* and *hold* specifications for edge-detection. In that case, the integral is analogous to a slew measurement or RC delay model.

In Section 2.2 an integrated charge ($Q_{\int}$) metric is described. Section 2.3 presents an example application based on the integrated charge ($Q_{\int}$) metric. Section 2.4 defines metrics to analyze integrated charge ($Q_{\int}$) in a transmission media and describes transmission line effects on integrated Charge ($Q_{\int}$). Section 2.5 evaluates how to determine the data transfer rate of a practical link implementation. Section 2.6 presents results of datarate (Gb/s) for two different transmission media simulated over a range of lengths for edge and pulse based encoding.

2.2 Integrated Charge Metric

CMOS circuits, in general, have capacitive, voltage-sensitive, inputs. Digital logic, by design, provides well-defined, stable outputs between transitions. With a well-defined starting voltage, and a capacitive input one can define the amount of charge required to reach a given voltage as $Q_{\int}$, the integrated input charge. When $Q_{\int}$ reaches some value (Q_{crit}) the decision voltage (V_{trig}) is reached on the front-end, and the gate, from an event-driven perspective, is triggered. Timing critical asynchronous machines, such as synchronizers and phase detectors, have made use of integrated charge as early as some of the first CMOS based sawtooth phase detectors[36]. Equation 2.1 formalizes a $Q_{\int}$ metric which models a gate triggering condition.

$$\int g_m \cdot min(0, V_{in}(t) - V_{Imin}) \geq Q_{crit} = V_{trig} \cdot C_{eff} \tag{2.1}$$

This triggering condition signifies the minimum charge (Q_{crit}) to successfully recieve information. V_{Imin} represents the minimum voltage required to start integrating charge at the critical node (the noise rejection threshold). g_m represents the transconductance of the circuit averaged over the decision region. C_{eff} is the effective capacitance at the detection node. The validity of the $Q_{\int}$ measure is dependent on g_m being a valid representation of transconductance over a range of inputs between V_{Imin} and V_{trig}. Note that if the $Q_{\int}$ is below the V_{Imin} it should not affect the critical node at all. If the $Q_{\int}$ above V_{Imin} is less than $V_{DD}C_{crit}$ then the critical node should not be affected and no event must be detected. Lastly, two equal $Q_{\int}$ above V_{Imin} should have similar effects on the event detection.

2.3 Example Application

To demonstrate the use of the $Q_{\int}$ concept we examine a circuit designed for data transmission, using self-resetting logic[28]. A receiver/pulse-shaper circuit from this family is shown in Figure 2.1. The critical values for Equation 2.1 are derived from the behavior of this pulse shaper: $Q_{\int} \geq Q_{crit}$ will cause a pulse on the output, while V_{Imin} is established by the noise suppressing keeper, the 10k resistor, and V_{trig} is set by the decision voltage of the inverter driving the output.

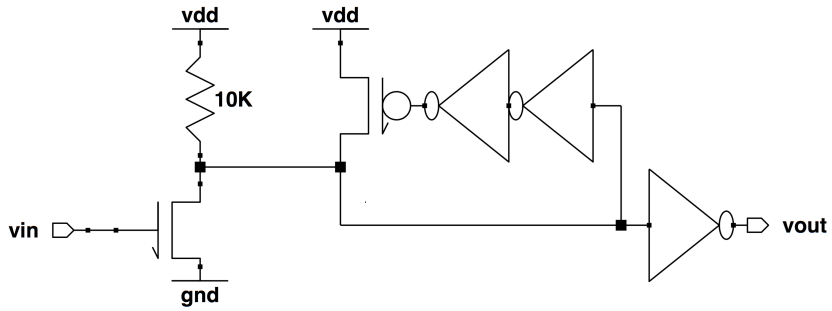


Figure 2.1: Logic circuit for detection of Integrated Charge ($Q_{\int}$) encoded as a pulse.

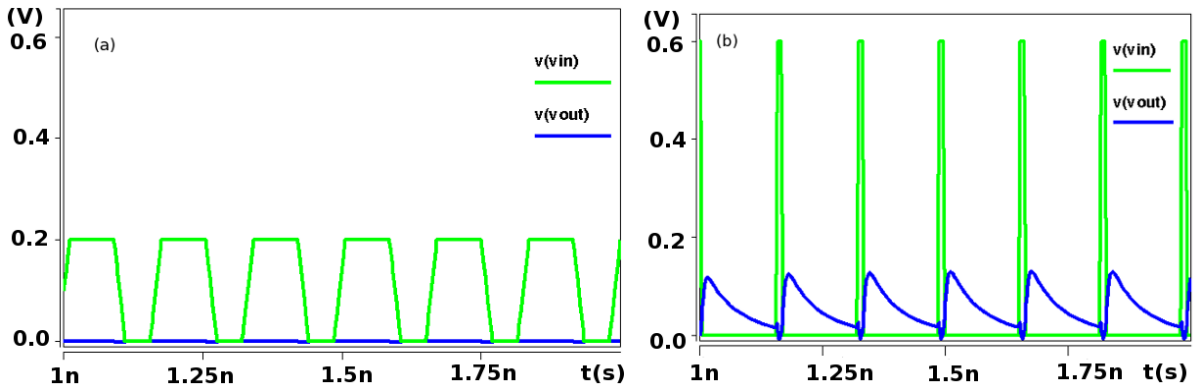


Figure 2.2: (a) Incoming pulse amplitude **below** V_{Imin} at critical node. (b) Incoming pulse amplitude **above** V_{Imin} at the critical node but $Q_{\int}$ is below Q_{crit}

Figure 2.2 shows circuit critical node behavior for two cases where $Q_{\int} < Q_{crit}$. In the first case (Figure 2.2(a)), Pulses don't cross above V_{Imin}, and no charge is accumulated. In the second case, (Figure 2.2(b)) Pulses cross V_{Imin} but V_{trig} is not reached and no pules

result on the output. By contrast, Figure 2.3 demonstrates two cases of $Q_{\int} > Q_{crit}$. Here two pulse trains (dashed lines) at input both result as pulse trains a the output (solid lines). The relative difference in pulse shapes does not alter the one-pulse-in-one-pulse-out function. Thus, this simple model can be used to validate detection in this and similar signaling strategies.

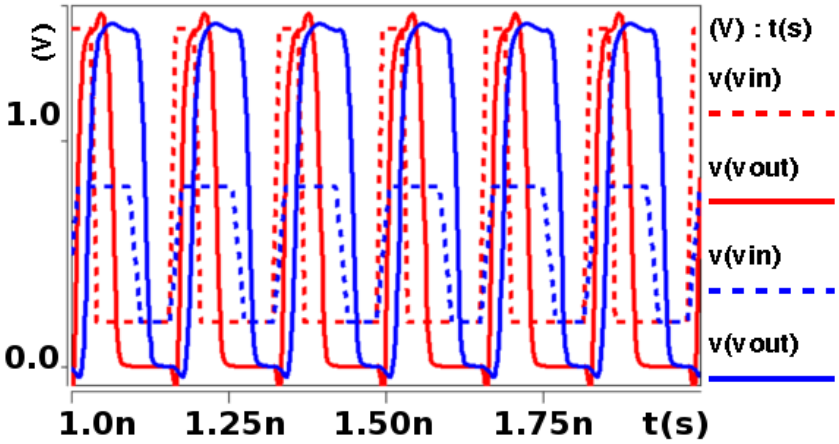


Figure 2.3: Different input pulses (dotted line) with same $Q_{\int}$ result in equivalent output.

2.4 Integrated Charge and Signal Integrity

$Q_{\int}$ has promise as an evaluation tool for signal integrity for asynchronous links, because it can describe the triggering conditions of asynchronous circuits. Classic measures of signal integrity for synchronous links, such as eye diagrams, focus on amplitude and timing uncertainty, while $Q_{\int}$ can better describe circuits where there is a trade-off between the two.

2.4.1 Timing variance & voltage noise

Variance in signal timing can be induced by loss in transmission media or from coupled noise. For example, Figure 2.4 shows strong loss applied to both edge, and pulse encoded signals. A lossy line induces a delay in the signal that is dependent on the previous, incomplete transmission.

To first order, $Q_{\int}$ can be viewed as the area in the signal above the defined threshold V_{Imin}. If this area is above Q_{crit} then the signal is successfully transmitted. $Q_{\int}$ here matches the human intuition that the signals in Figure 2.4 are interpretable if one were to set the levels correctly, even though neither of these curves would have an open eye. Hence $Q_{\int} - Q_{crit}$ serves as a noise margin allowing the selection of both V_{Imin} and Q_{crit}.

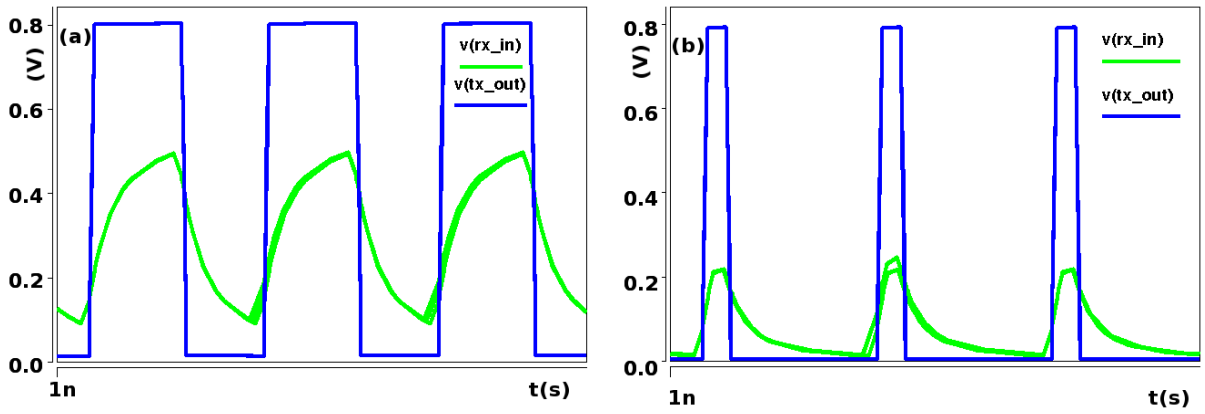


Figure 2.4: Jitter & attenuation for (a) Edge (b) Pulse

2.4.2 Inter Symbol Interference (ISI)

ISI, mainly caused by reflections, is a significant potential source of noise in a link. Such reflections are often due to impedance mismatches in the transmission media. Reflections can cause two effects, either interfere with the detection of an intended signal or inject a detectable unintended signal.

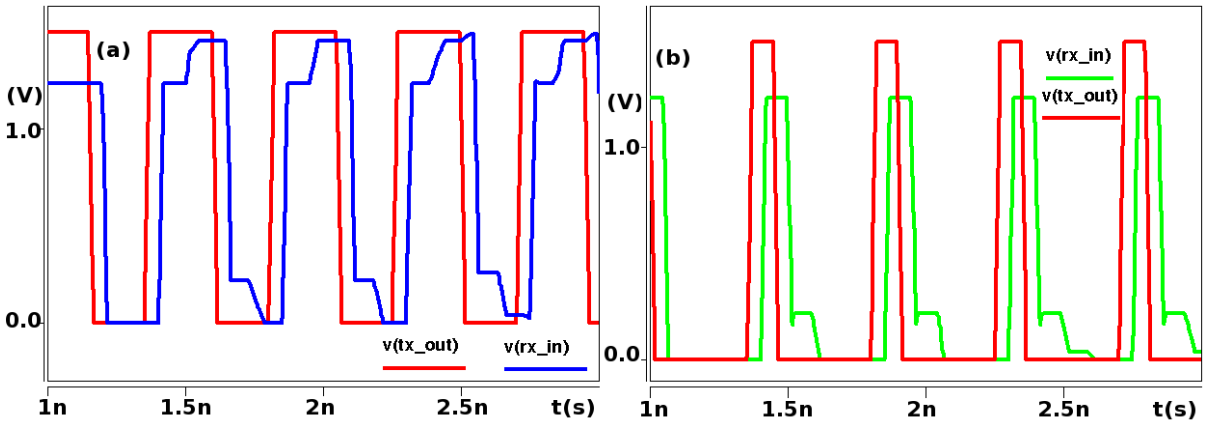


Figure 2.5: (a) Positive edge reflections have potential for double edge detection (b) Positive pulse reflections adding the charge where is does not exist and decreasing noise margin

Figure 2.5 shows the effect of positive reflections, due to under-termination, on both pulse and edge coded links. It can be seen that if the $Q_{\int}$ added because of positive reflection between the encoded information remains below noise margin, the information will be transmitted reliably. In case of negative reflections, if the $Q_{\int}$ remains above the noise margin the signal would be detected and the information will be successfully transmitted. It can be seen that it is advantageous to have positive reflections in the receiver as it adds to the signal, but it needs to be ensured that the noise created because of it remains below the noise margin.

2.4.3 Attenuation, Jitter and Dispersion

Attenuation is the result of losses in the transmission media, which are frequency dependent as higher frequencies are more susceptible to skin-effect, dielectric loss, and radiative loss. Attenuation is given by Equation 2.2 according to [37], where frequency dependent resistance and inductance are given by Equation 2.3 and Equation 2.4. If the information is represented as $Q_{\int}$, the effect of attenuation is decreased in the $Q_{\int}$ value

as the signal passes through the transmission media.

$$atten = 20\ log_{10}[\exp(Re\sqrt{(R + j\omega L)(G + j\omega C)})] \tag{2.2}$$

$$R(f) = \omega\frac{\delta}{2}\frac{\partial L}{\partial n}; \delta = \sqrt{\frac{\rho}{\pi f \mu}} \tag{2.3}$$

$$L(f) = L_{external} + L_{internal} = L_{external} + \frac{\delta}{2}\frac{\partial L}{\partial n} \tag{2.4}$$

Dispersion is a spreading of signal energy in time. Dispersion is given by Equation 2.5 according to [37], where Equation 2.3 and Equation 2.4 are its frequency dependent resistance and inductance. Dispersion leads to phase variance in the transmitted information. Dispersion has a major effect in setting the data rate through the transmission media. The pulse encoding suffers from pulse widening and edge encoding from increase in rise and fall times. Jitter is the phase shift of the symbol resulting in external and internal noise in the system.

$$\beta(f) = Im[\sqrt{(R + j\omega L)(G + j\omega C)}] \tag{2.5}$$

Figure 2.4 shows the effect of attenuation, jitter and dispersion on the $Q_{\int}$ encoded as a pulse and an edge. Channel jitter also shows up as phase variance and can be similarly accounted for. Dispersion and jitter both result in phase variance and have been taken into account collectively as phase variance in this paper for analysis in the later sections. Successful reception requires that the $Q_{\int}$ after the attenuation and phase variance in the media remain above the noise margin.

2.4.4 Baseline Shift

For 2-wire transmission schemes, common mode (both wires changing in the same direction) content in the information sent over the transmission line shifts the reception baseline at the receiver. This results in a shift in the V_{Imin} value at the receiver as compared to that at the transmitter. For example baseline shift at the receiver event detector when constant pulses are sent down a meter of 50 ohms trace in a FR4 PCB can be about 300 mV. The offset is proportional to media length and can be mitigated by differential transmission or by chosing line codes with minimal common mode content.

2.5 Data transfer rate

The maximum data rate of a link can be limited by the transmission media due to frequency dependent loss. Since loss and noise grow with distance, there is a trade off between data rate and link length. Data transmission over longer distances require that the $Q_{\int}$ remains above the noise margin after ISI, attenuation and jitter effects. Additionally, two adjacent symbols need to be kept from colliding due to jitter. A working link needs to maintain sufficient signal strength and temporal separation such that $Q_{\int}$ over the noise threshold represents an achievable Q_{crit} at the receiver.

For RZ pulse encoding, there is a minimum separation between pulses at the transmitter output to allow reliable detection at the end of the transmission line. The attenuation provides with different charge loss at different lengths of transmission media. Thus, the minimum charge needed by the detector to work reliably puts the limit on transmission line lengths. Phase variance allows determination of the minimum separation of pulses for different lengths of transmission media. This result is highly dependent on the jitter in the transmitter. The separation of effects determine the data rate depending on how

many pulses can be accommodated in a given clock cycle. Hence if:

$$Q_{initial} - Q_{loss} \geq Q_{min\ detectable} \tag{2.6}$$

where $Q_{initial}$ is the charge in the minimum sized pulse. The minimum sized pulse generation is technology dependent. Then:

$$data\ rate = \left\lfloor \frac{T_{clock}/2}{T_{min\ pulse}} \right\rfloor \times \frac{2}{T_{clock}} \tag{2.7}$$

Else increase $Q_{initial}$ and calculate date rate according to new $T_{min\ pulse}$.

For edge based encoding, the minimum charge needed at the receiver directly helps in determining the minimum separation between the edges. T_{min} is the value of time it takes to reach the minimum detectable charge at the event detector. The value increases with length as the edge slope decreases with length. It is ensured that transmitter can transmit this minimum separation reliably. Thus, the data rate is determined by how many edges can be accommodated in a single clock cycle. Hence if:

$$T_{min\ edge} \geq T_{min}\ and\ T_{detector\ edge} \geq T_{min} \tag{2.8}$$

where $T_{min\ edge}$ is the minimum possible separation between the edges from the transmitter and $T_{detector\ edge}$ is the separation between the edges at the receiver or detector measured from V_{Imin}. then:

$$data\ rate = \left\lfloor \frac{T_{clock}/2}{T_{min\ edge}} \right\rfloor \times \frac{2}{T_{clock}} \tag{2.9}$$

Else increase $T_{min\ edge}$ and calculate the data rate again. Hence data rate in general is

given by:

$$data\ rate = \left\lfloor \frac{T_{clock}/2}{T_{min\ symbol}} \right\rfloor \times \frac{2}{T_{clock}} \times N_{transition} \tag{2.10}$$

where $T_{min\ symbol}$ is the minimum possible separation between the symbols (edges or pulses) and $N_{transition}$ is the number of valid transitions possible after each transition.

2.6 Results

The minimum detectable charge for the receiver based on circuit topology in Figure 2.1 is shown in Figure 2.6. The plots are done for 75ps pulse width at the transmitter and hence an initial charge of $44.25V.ps$. The minimum detectable charge from

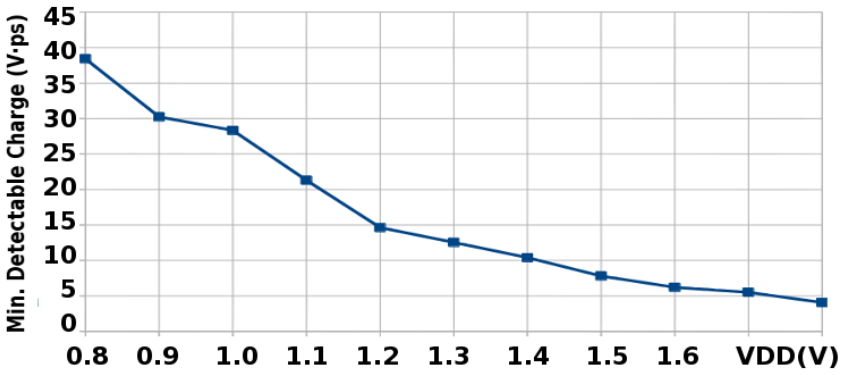


Figure 2.6: Minimum Detectable Charge

Figure 2.6 has the value of 7.8 V.ps for 1.5V VDD. The minimum separation between the 75 ps pulses taking phase variance into account is 185ps. This value is highly dependent on jitter due to transmitter. This results in a 5.12 Gb/s data rate in the RZ encoded pulse link using Equation 2.10. The minimum time difference between the edges to take phase variance in the link and transmitter design constraints into account is 185ps, which is greater than T_{min}. This results in a data rate of 5.12 Gb/s using Equation 2.10 for 2 level edge based encoding. Figure 2.7 shows the increasing loss with length in the edge and pulse based links. This results in data rate as shown in Figure 2.8, which can be seen

to be above 5Gb/s for about 5 feet in FR4 stripline. Data rates remain above 5Gb/s for RG-178 in lengths up to 6 feet.

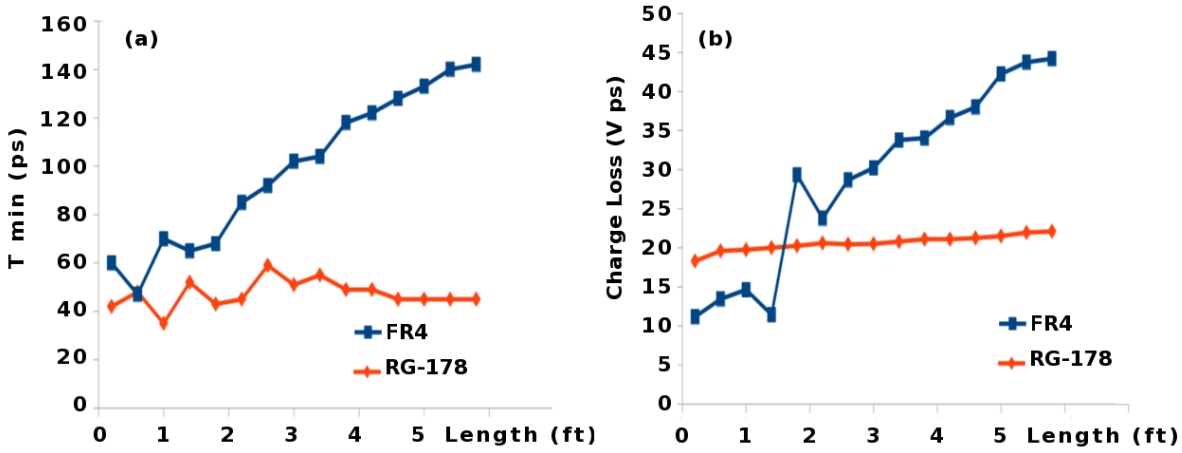


Figure 2.7: Loss vs Length in (a) Edge and (b) Pulse

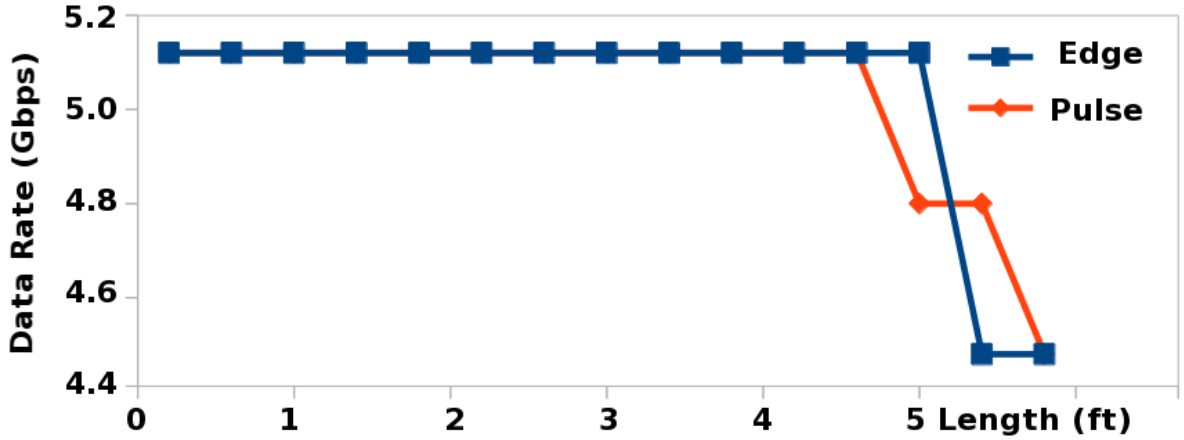


Figure 2.8: Data Rate vs Length

The constraints on minimum separation of edges in two and three level encoding does not change but $N_{transition}$ has a value of two in three level encoding. Hence, data rate of the order of 10.24 Gb/s in the lengths in order of 5 feet in PCB and coaxial cables is achievable with 130nm technology using Equation 2.10. The implementation must be fully differential to alleviate the baseline shift or line coding schemes must be used to

reduce the integral common mode content in all these implementations. $Q_{\int}$ metric used in the presented results has an advantage over conventional eye diagram based metric as the effects mentioned in section 2.4 only become apparent at lengths greater than 5 ft in the analyzed media. Hence a substantially higher data rate is achievable at a given length with the use of $Q_{\int}$ metric.

2.7 Conclusions

A new methodology to alleviate the problems associated with conventional serial link designs was proposed. The proposed $Q_{\int}$ metric can help us make a jitter tolerant link, which can be self timed to get away from time of flight issues in handshaking and not have additional circuitry for synchronization and maintaining signal integrity. The link also has negligible idle state power consumption and can be used with conventional asynchronous techniques alongside the link. The margins for proper utilization of the metric were described and a design was proposed for implementation of a 10+ Gb/s link in 130nm.

Chapter 3

Gate Level Event Dynamics

3.1 Introduction

Chapter 2 described the use of integrated charge at input node of an amplifier as a detectivity metric in asynchronous serial link design. Charge modulation at the input also leads to delay modulation in a amplifiers. This delay modulation is the basis of this work. This chapter focuses on the definitions of the delay modulation. It describes different transistor and gate level modifications to achieve predictable delay modulation in gates. The idea of basic ring oscillators when gates in the ring have delay modulation in then is introduced in this chapter.

3.2 Delay-vs-Separation

Delay-Separation dynamics were observed for asynchronous events interaction in a pipeline [10]. The idea is used in this work to convey the timing information of the current pulse arrival to modify the delay of the subsequent pulse as shown in Figure 3.1. Delay of a pulse through a gate is a function of separation of the pulse from the last

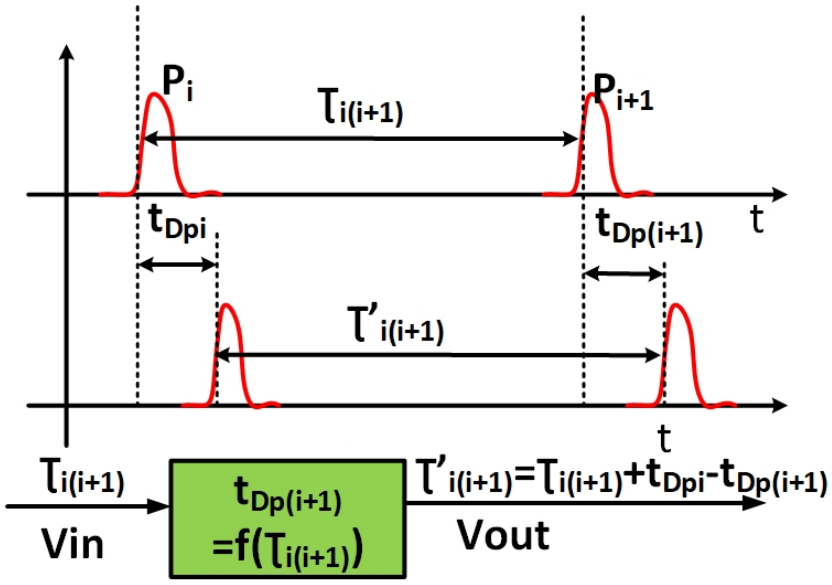


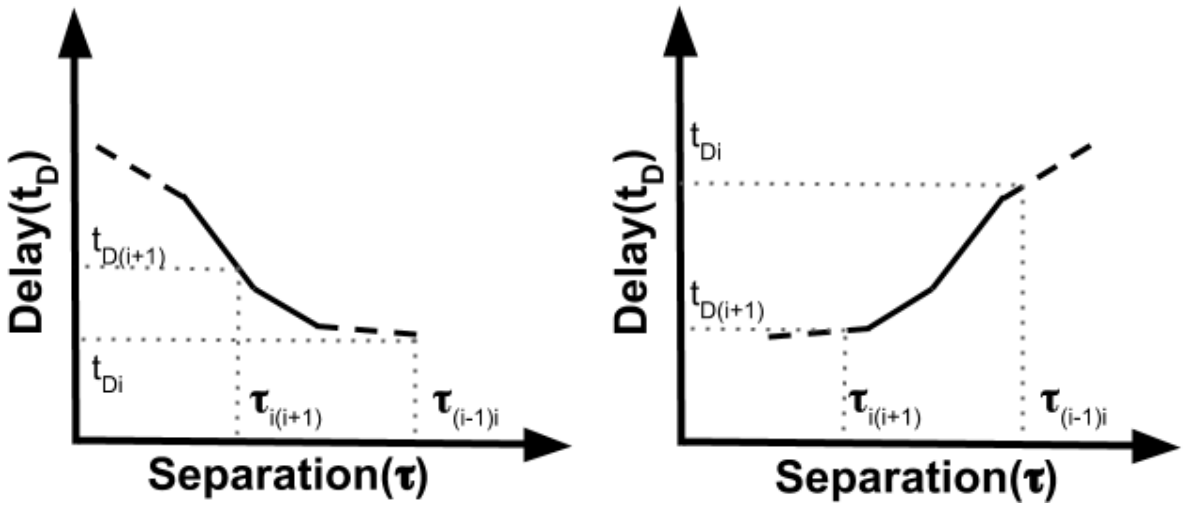
Figure 3.1: Delay-vs-Separation effect

pulse which passed through the gate. This leads to modification of separation between pulses as they pass through a chain of gates. For consecutive pulses Pi and $Pi+1$, the gate delay of the second pulse $t_{Dp(i+1)}$ is dependent on the relative timing of the first pulse $\tau_{i(i+1)}$. Effectively, the gate has a relatively long recovery time in which behavior is correct, but the timing of the second pulse is modified. A *delay-separation curve* indicates the propagation delay for a pulse passing through a gate as a function of timing separation from the previous pulse. The simplest curves are *repulsive* shown in 3.2a or *attractive* shown in 3.2b.

Repulsion will result in the separation between pulses to increase in a long chain of gates until the dynamics changes. *Attraction* will cause the pulse separation to decrease. This is the behavior observed for pulses in conventional CMOS logic leading to the pulse-evaporation phenomena.

- Repulsion: $t_{D(i+1)} > t_{Di}$ Separation between pulse P_i and pulse P_{i+1} **increases** after passing the logic circuit.

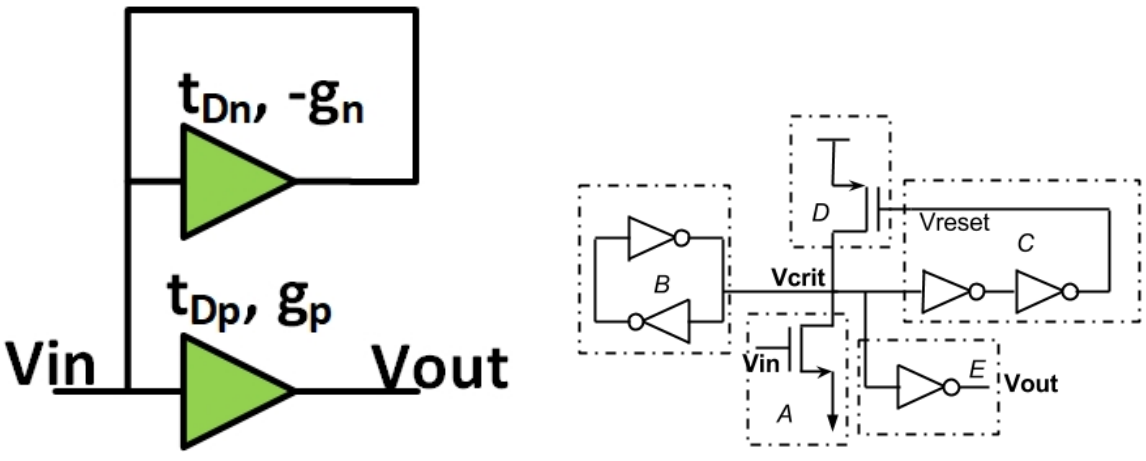
- Attraction: $t_{Di} > t_{D(i+1)}$ Separation between pulse P_i and pulse P_{i+1} **decreases** after passing the logic circuit.



(a) Repulsion (b) Attraction

Figure 3.2: Different delay-vs-separation dynamics

3.3 Pulse-Gates



(a) Cell abstraction (b) Circuit implementation

Figure 3.3: Pulse gate

Pulse-gate circuit implementation has following fundamental components:

- *A:* Vin : Input Logic Pull-down of Vcrit;
- *B:* Threshold Control : Controls the threshold for Vcrit;
- *C:* Reset Loop and Pulse Width : Controls reset behavior;
- *D:* Pull Up : Pulls up Vcrit on Vreset ;
- *E:* Vout : Output Buffer

Pulse gate behavior is easily tuned to create different pulse-to-pulse dynamics, making an effective non-linear delay element. The basic topology of a pulse-gate is shown in 3.3b. At steady state, Vin is low and Vcrit is high. A rising edge at Vin pulls down Vcrit. This in turn pulls up Vout and eventually pulls down Vreset, which then pulls up Vcrit. Vcrit then pulls down Vout and pulls up Vreset, making a pulse and reseting the gate. These gates are triggered by, and re-generate brief electrical pulses. They typically have different delays for short triggering intervals than for long intervals. Operated in the transition between short and long intervals, the gate propagation delay is *dependent* on the oscillator frequency. If the dynamics are repulsive, multi-pulse oscillation solutions with uniform timing are possible.

Abstract version of a pulse gate is shown in 3.3a. It consists of a forward loop delay with a positive gain and a feedback loop with a negative gain. Delay in the negative feedback loop controls the delay of the forward path. If the negative feedback loop has not yet come to steady state, after the occurence of the last pulse, the next pulse sees a modification of the delay.

For the circuit shown in 3.3b, the delay-vs-separation dynamics observed is shown in Figure 3.4. This dynamics can be primarily broken into 3 regions of operation.

1. *Region 1* is when Vcrit is still low after the occurence of the first pulse. A subsequent pulse is rejected in this region.

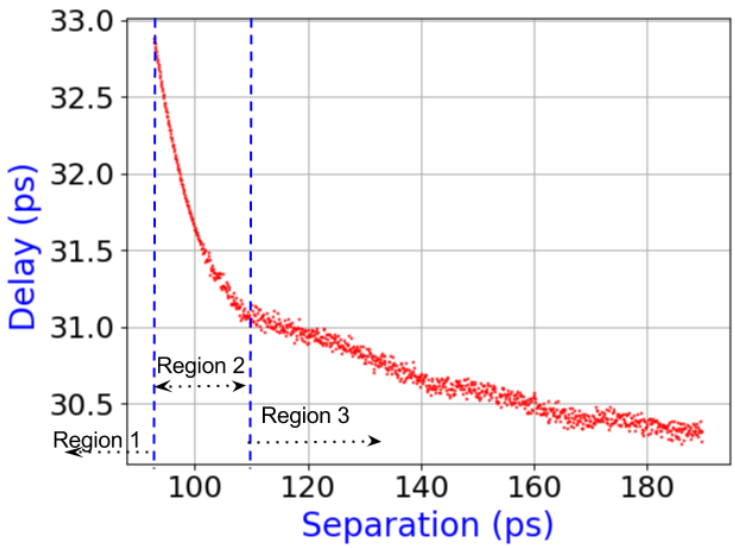


Figure 3.4: Delay-vs-Separation Dynamics for Pulse-Gates

2. *Region 2* is the region of high repulsion slope. It occurs when next rising edge arrives when PMOS has pulled up Vcrit enough that there is a substantial drain-source potential difference across the pull down NMOS. However, there is sufficient voltage swing at Vcrit to cause full swing Vout. On the other hand, both pull-up and pull-down sources are active, delaying the swing of Vcrit. This results in a larger delay as the pulse separation is decreased. This region ends when Vreset goes up.

3. *Region 3* starts after Vreset is pulled up. The lesser delay slope is a function of stored charge in the SRAM hysteresis loop and input transistor network.

In order to model or modify the pulse dynamics, the key behavioral mechanisms need to be understood. These are:

- **Detection**: Detect input pulse rising edge

- **Pulse Generation**: Output a pulse on detection based on current state of the circuit
- **Pulse Width Control**: Maintain output pulse width
- **State Control**: Maintain state to control the next pulse bevavior. It refers to timing control of when pull up and pull down fight at Vcrit in the dynamics plot.

For pulse-gate shown in 3.3b, *Pulse Width Control* and *State Control* are interlinked to each other and hence the freedom to modify the dynamics is limited.

3.3.1 Shape Preservation

The pulse width control feature of the pulse gates ensure that pulses are regenerated each time they pass the pulse gate. This maintains the shape of the pulse. This is a necessary feature of this work. All the dynamics are achieved while maintaining the pulse shapes. The local reset loop (to maintain pulse shape) ensures the independent nature of dynamics from the shape of the pulse.

3.4 Modified Pulse Dynamics

In order to independently adjust the pulse dynamics, pulse-gates were implemented using the updated pulse-gate shown in Figure 3.5. Separate *Pulse Width Control* and *State Control* allow for independent timing tuning of pulse-width and internal gate reset.

Two functionalities which can be achieved are:

- *Separation axis:* Delay in the reset loop shifts the curve along the separation axis as shown in 3.6a

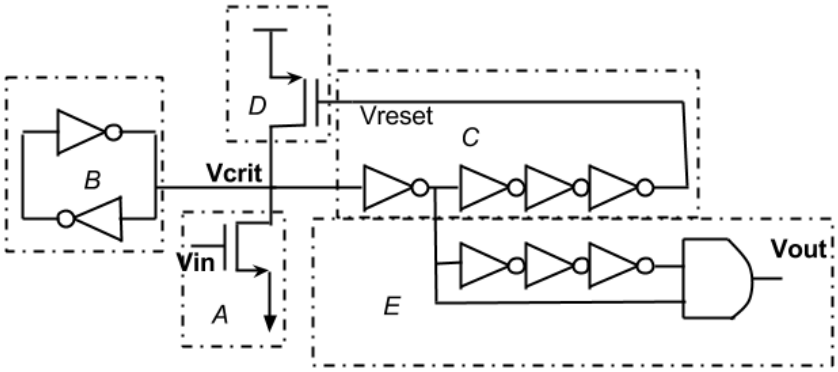
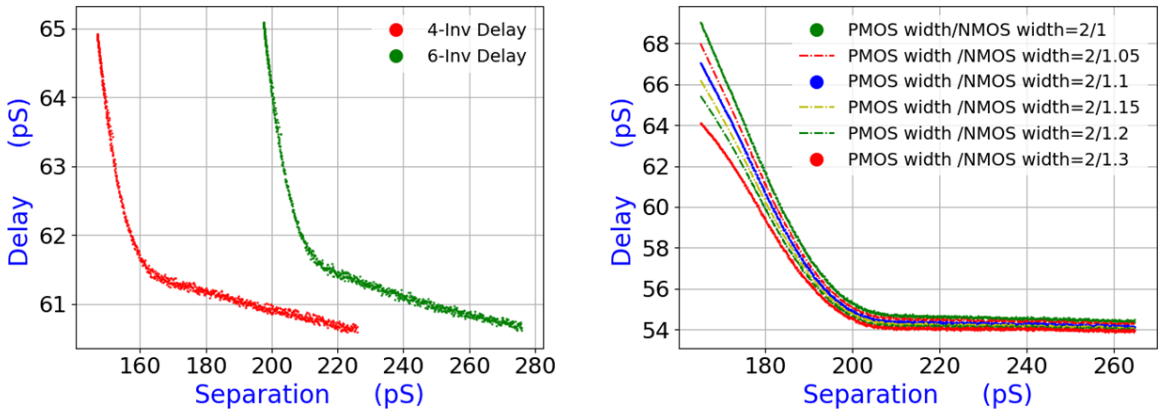


Figure 3.5: Pulse-gate with separate *State Control* : **C** path and *Pulse-Width Control* : **E** path

- *Delay axis:* PMOS to NMOS ratio at the Vcrit node shifts the curve along the delay axis as shown in fig 3.6b. It also controls the slope in *Region 2*.



(a) Separation axis

(b) Delay axis

Figure 3.6: Dynamics along different axis

3.5 Limitations:Second Order Effects on Dynamics

The delay-vs-separation characteristics are dependent on following second order effects which shift the curve as shown in Figure 3.7. The effects arise from change in detectivity point as described in [38] and Chapter 2.

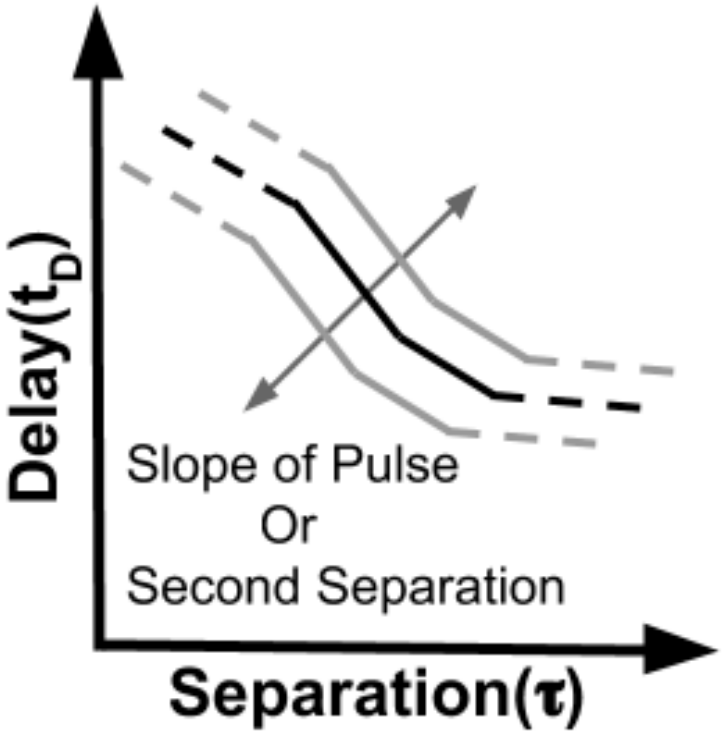


Figure 3.7: Second-Order Effects on Delay-vs-Separation Characteristics

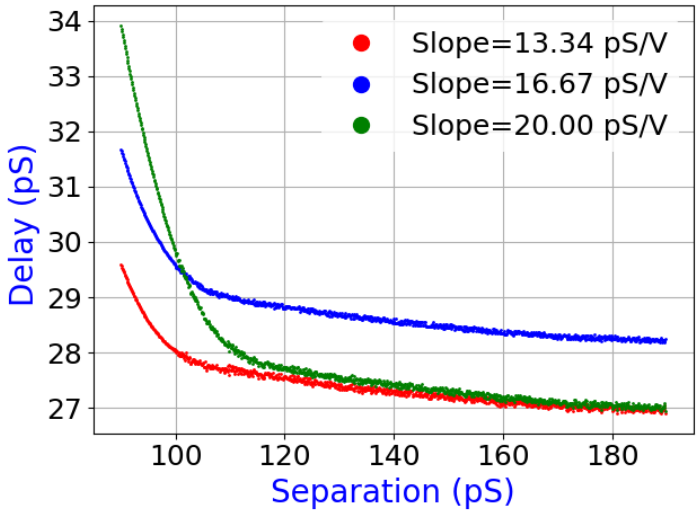


Figure 3.8: Delay-vs-Separation shifting due to change in slope of the rising edge of the pulse

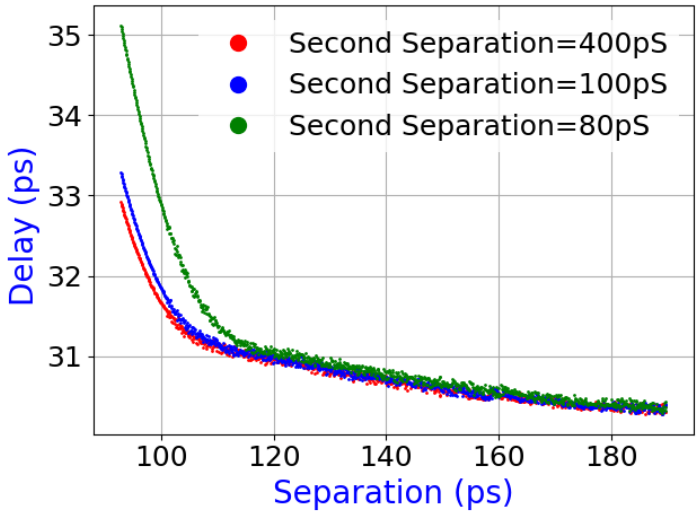


Figure 3.9: Delay-vs-Separation shifting due to change in Next Pulse Separation

3.5.1 Slope effect

All the delay-vs-separation curves described until now assume ideal pulses (all having same slope which does not vary). In the case of non ideal pulses, the slope of the pulse shifts the delay-vs-separation characteristic as shown in Figure 3.8. The pulse changes the rising edge slope under the variation of parameters like temperature.

3.5.2 Next Pulse Separation

Delay-vs-separation characteristic described until now considers the separation of the first and second pulse as the independent variable and delay of the second pulse as the dependent variable. The delay of the second pulse is also dependent on its separation from the next event which shifts the delay-vs-separation characteristics as shown in Figure 3.9. For three pulses P_{i+1}, P_i and $Pi-1$, the delay of pulse P_{i+1} depends on the separation between P_{i+1} and P_i and also between P_i and P_{i-1} (termed as second separation). These effects change the timing behavior of the gates and result in small errors which have not been modeled in this study.

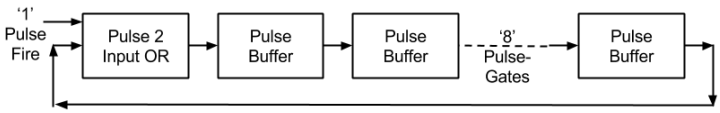


Figure 3.10: Abstract Model of Pulse Oscillator with 'M' Pulses and 'N' Stages

3.6 Pulse Ring Oscillator

3.6.1 Construction

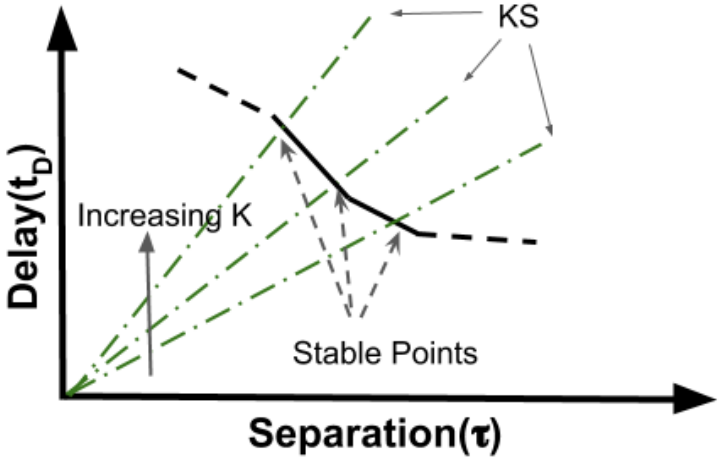


Figure 3.11: Operating stable point of the oscillator

An abstract model for the Pulse Ring Oscillator is shown in Figure 3.10. M pulses are fired into the ring of N pulse gates, each with identical separation curves. The initial separation between the pulses is decided based upon the expected stable operating point of the ring.

It is important to note that in such an oscillator construction, period and duty cycle are not independent of each other. Duty cycle is set by the pulse width, which is a property local to a pulse gate. Period on the other hand is a feature of the whole oscillator construction. It is determined by the interaction between number of pulses, number of stages and delay-vs-separation characteristics as described next.

3.6.2 Stable Point Period

To estimate the stable point of an oscillator built from a uniform ring of pulse-gates supporting multiple pulses, a constant K is defined as *number of pulses (M)* divided by *number of logic stages (N)*, $K = N/M$.

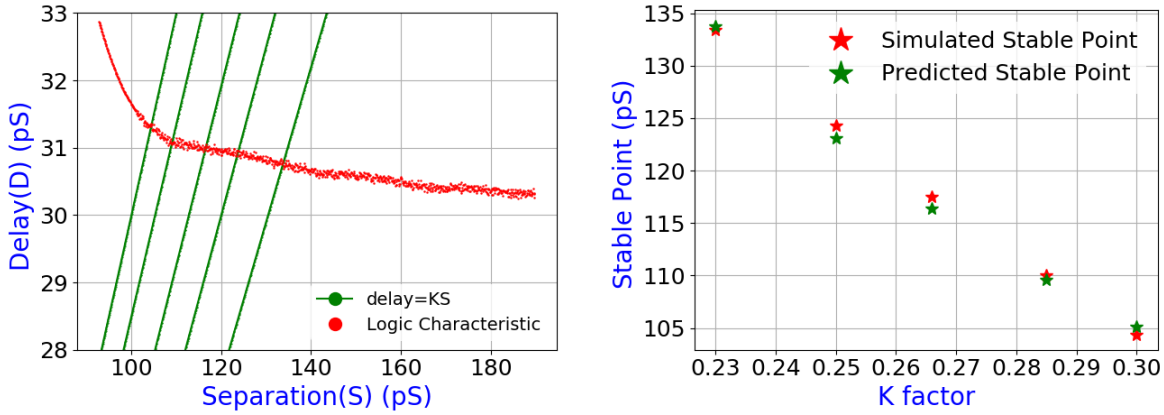
$$t_{Dp} = K\tau \tag{3.1}$$

where t_{Dp} is the gate delay seen by each pulse, τ is the separation between pulses(oscillator period). The stable point is the intersection of the delay-vs-separation plot of the logic gates and delay given by Equation 3.1. For the case of *Repulsion* dynamics, stable point for different K is approximated as shown in Figure 3.11. Repulsion delay-separation results in a stable equilibrium. Any change in separation from the stable point brings the oscillator back to stable point due to the negative slope at this point. Attraction usually results in a non-uniform stream of pulses or pulse loss. This is detailed further in next chapters.

The stable operating point based on intersection of $t_{Dp} = K\tau$ and delay-separation dynamics of Pulse-Gate is shown in 3.12a for different values of K. The projected (from intersection as discussed above) and simulated (HSPICE) stable ring periods are shown in 3.12b.

3.7 Conclusion

In this chapter, the meaning of dynamics of gates was explained. Dynamics were shown to be present in the gates due to delay-vs-separation characteristics of the gates. Pulse gates were shown to be reliable method to create and modify the dynamics as per the requirement. Pulse gates were also shown to preserve pulse shapes while creating



(a) Intersection of $t_{Dp} = K\tau$ and delay-separation (b) Simulated and predicted stable points

Figure 3.12: Operation stable points

dynamics. This shape preservation lets us ignore a lot of second order effects like slope modulation in further analysis. At the end, the concept of a ring oscillator and its operating point was introduced under the condition that the gates have variable delay. This analysis was strictly restricted to a case of no noise. Later chapters explore the effects of noise on such an oscillator.

Chapter 4

Timing Stability : Simulation and Measurement

Timing Circuits like voltage controlled oscillators (VCOs) are typically used in two kind of applications. First being RF/mmWave mixers and second being clocks for digital signal processing and microprocessors. The oscillators are typically phase locked in most of the applications. There is a small fraction of applications in ADC/TDC designs where free running oscillators are used. Improved timing stability provides advantages in both kinds of designs (free running and phase locked) and also both kinds of applications (RF/mmWave and Digital). The methodology to study the stability for various applications differs and needs to be well understood before going into the results of stability. First we describe a basic oscillator model. Then we describe how such a model behaves under conventional oscillator design. Then regions of non-conventional properties in timing stability (explored in this work) are presented. Finally, a methodology to study the such non-conventional properties is explained.

4.1 Oscillator Model

The oscillator analyzed has a basic model of Equation 4.1. The oscillator is assumed to have a nominal frequency of ν_n (units of cycles per second). The nominal angular frequency (in radians per seconds) is given by Equation 4.2. The total phase $\Phi(t)$ can be separated into perfectly cyclic component $\omega_n t$ along with a fluctuating compenent $\phi(t)$ as shown in Equation 4.3.

$$V(t) = V_o \sin(\Phi(t)) \tag{4.1}$$

$$\omega_n = 2\pi\nu_n \tag{4.2}$$

$$\Phi = \omega_n t + \phi(t) = 2\pi\nu_n t + \phi(t) \tag{4.3}$$

4.2 Noise Fundamentals

The instantaneous phase fluctuations $\phi(t)$ in the oscillator model described in section 4.1 can be due to different noise sources operating at different time scales. For a frequency noise given by Equation 4.4, different values of exponent and its phase counterpart are shown in Table 4.1

$$S_y(f) \propto f^{\alpha} \tag{4.4}$$

Table 4.1: Simulated Technology Projections

Noise	Frequency Slope(α)	Phase Slope
White PM(W PM)	2	0
Flicker PM(F PM)	1	-1
White FM(W FM)	0	-2
Flicker PM(F FM)	-1	-3
Random Walk FM(RW FM)	-2	-4
Flicker Walk FM(FW FM)	-3	-5
Random Run FM(RR FM)	-4	-6

4.3 Conventional Oscillators

For the oscillator analyzed in this study, typically the regions of noise associated are White FM and Flicker FM. Other noise regions are typically not analyzed since we run into thermal noise floor and circuit bandwidths in the high frequency sides and very low frequency noises are typically removed using phase locking. For the purpose of simulations only the White FM noise sources are analyzed unless explicitly needed by the application at hand. There are different models for analysis which all relate to each other when the noise source is White FM type. Next we see a quick overview of them in-order to understand the issues which these analysis face.

4.3.1 Jitter

There are typically two kinds of jitters cycle jitter and cycle to cycle jitter described by Equation 4.7 and Equation 4.8 respectively. Cycle jitter is the standard deviation of cycle period (given by Equation 4.6), while cycle to cycle jitter is the root mean square of difference of consecutive periods. Both convey useful information and are conventionally used for power supply noise analysis [39].

$$T_n = \Phi_{n+1} - \Phi_n \tag{4.5}$$

$$\Delta T_n = T_n - \bar{T} \tag{4.6}$$

$$\Delta T_c = \lim_{n\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} \Delta T_n^2} \tag{4.7}$$

$$\Delta T_{cc} = \lim_{n\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} (T_n - T_{n+1})^2} \tag{4.8}$$

Both the metrics do not converge to a value for noise with $\alpha < 0$. Also, even when they converge to a value, they convey very little information of time progression of stability.

4.3.2 Random Walk and absolute phase error

Random walk model suggests that if the noise sources are completely W FM in nature, then the uncertainty in the timing of the of the phase grows linearly with square root of time as given by Equation 4.9.Cycle to cycle jitter is related to the absolute phase error by the slope of the random walk. In that relationship, cycle to cycle jitter is the absolute phase error after 1 cycle.

$$\sigma(\Phi) = k\sqrt{t} \tag{4.9}$$

$$log(\sigma(\Phi)) = log(k) + \frac{1}{2} log(t) \tag{4.10}$$

The slope of the random walk directly relates to the frequency domain phase noise measurement by Equation 4.11, where $L(\Delta\nu)$ is the phase noise at offset frequency of $\Delta\nu$.

$$k = \frac{\Delta\nu}{\nu_n} . 10^{\frac{-L(\Delta\nu)}{20}} \tag{4.11}$$

Random Walk model and its frequency domain counterpart work well when the noise has $\alpha = 0$. For any other noise slope, the model does not faithfully convey the system information.

4.3.3 Simulation

Typically, for non-linear oscillators like ring oscillators with limiting amplifiers, transient noise simulations are suggested (Simulation methods which predict the timing stability by a steady state solution generally do not capture the non-linearities in the circuits). Two forms of transient noise simulations are typically available (Monte Carlo and single Run). Monte Carlo simulations take a very long time to predict the system behavior and do not reveal much about how design decisions affected the system behavior since they reveal an ensemble behavior. Single run transient simulations project single cycle errors using a White FM noise model. Time integrated errors are also calculated based on an ideal clock. In-order to predict and optimize the timing characteristics two design models are prevalent in the literature:

Hajimiri Model : Impulse Sensitivity Function [15]

Impulse Sensitivity Function(ISF) is a Linear Time Variant function of phase change to impulse noise across the oscillator phase as given by Equation 4.12. Due to linear superposition being valid root mean square of the ISF can be used to predict the phase noise and hence timing stability of the oscillator as given by Equation 4.13

$$h_\phi(t,\tau) = \frac{\Gamma(2\pi\nu_o\tau)}{Q_{max}} u(t-\tau) \tag{4.12}$$

$$L(\Delta\nu) = \frac{\Gamma_{rms}^2}{8\pi^2\Delta\nu^2} . \frac{\frac{\bar{i_n^2}}{\delta\nu}}{Q_{max}^2} \tag{4.13}$$

Demir Model : Phase Amplitude Variations [16]

ISF model ignores the amplitude to phase errors in the oscillators. Demir model takes both phase and amplitude errors converting into phase errors and resulting in timing instability. Since most of the non-linear oscillators are made of amplifiers having amplitude limiting mechanism built into them, this effect can be ignored to first order in ring oscillators without much distortion in the result values.

4.3.4 Measurement

As stated earlier, in-order to cater to the two broad application space, RF circuits, where noise power matters and time domain TDC, microprocessor etc., where stability after N cycles matters, following measurements are usually made:

- Cycle to cycle jitter for one cycle. This value can be projected to any number of cycles since conventionally a random walk model described earlier holds true.
- Power Spectral Density: This value gives the noise power at a given frequency offset and is used for RF applications.

Both the values can be translated into one another using methods described before. Also both values can be easily computed using traditional measurement devices like oscilloscope and spectrum analyzers.

4.4 Problems with conventional analysis

Two problems exist when using the conventional analysis.

- *Models to visualize* the timing stability assume that there is no phase error correction going on in the oscillator over time (non external phase locked case). This

leads to the assumption that a cycle to cycle jitter can be projected using White FM random walk. If there is any phase error correction going on over time, then the model fails to represent the system dynamics.

- *Models to design and optimize* the oscillators assume that phase error does not correct over time. Hence there is no leeway in them to account for a phase error correction term.

4.5 Allan Deviation

Allan deviation is a tool to measure the time domain stability and has been researched quite in depth. The tool has mainly been applied to analysis of noise in the long timescales typically ranging from 1 seconds and greater. The representation given by the allan deviation provides a good method to analyze the phase error correction happening in the oscillators in the short times of nano-seconds. Allan variance is given by Equation 4.17 where $\bar{y}(t,\tau)$ is average fractional frequency given by Equation 4.15.

$$y(t) = \frac{\nu(t) - \nu_n}{\nu_n} = \frac{\nu(t)}{\nu_n} - 1 \tag{4.14}$$

$$\bar{y}(t,\tau) = \frac{\Phi(t+\tau) - \Phi(t)}{\tau} \tag{4.15}$$

$$\bar{y_i} = \frac{\Phi_{i+1} - \Phi_i}{\tau} \tag{4.16}$$

$$\sigma^2(\tau) = \frac{1}{2} < (\bar{y}_{n+1} - \bar{y}_n)^2 >= \frac{1}{2\tau^2} < (\Phi_{n+2} - 2\Phi_{n+1} + \Phi_n)^2 > \tag{4.17}$$

$$\sigma_y = \sqrt{\sigma_y^2(\tau)} \tag{4.18}$$

4.5.1 Modified Allan Deviation

The Allan variance has a drawback in that it is unable to separate the white phase modulation (WPM) from the flicker phase modulation (FPM). Looking at their response to Power-law noise it is clearly seen that WPM and FPM have almost the same response to τ, but WPM is linearly sensitive to the system bandwidth whereas FPM is only weakly dependent on it. Thus, by varying the system bandwidth the WPM and FPM noise forms may be separated. However, it is impractical to alter the hardware of the measurement system. By post-processing the sample-series and implementing a software bandwidth a modified Allan variance measure can be given capable of resolving the noise forms.

Modified Allan variance is given by Equation 4.19. By averaging the Allan variance, it introduces a bandwidth limitation on the output values. So, it is able to distinguish between WPM and FPM like noise sources. In computation, the bandwidth limitation is imposed by post processing the phase data using Modified Allan variance given by Equation 4.20. In practice, a loop unrolled version of modified Allan variance is used.

$$mod\ \sigma_y^2(\tau) = \frac{1}{2\tau^2} < [\frac{1}{n}\sum_{i=o}^{n-1} \Phi_{i+2n} - 2\Phi_{i+n} + \Phi_i]^2 > \tag{4.19}$$

$$mod\ \sigma^2(\tau = m\tau_0) = \frac{1}{2(m\tau_0)^2(N-3m+1)} \sum_{j=1}^{N-3m+1} \{ \sum_{i=j}^{j+m-1} \Phi_{i+2m} - 2\Phi_{i+m} + \Phi_i \}^2 \tag{4.20}$$

4.5.2 Frequency Filtering

Modified Allan variance was used as the measure in this study. Since the phase error correction takes the form of a high pass filter which looks similar to WPM and FPM regions and it is essential to distinguish them. Different high pass noise filtering slopes can be distinguished using the slope of Modified Allan variance. As shown in Figure 4.1, Modified Allan variance has a slope of -3/2 for White PM (which resembles a high pass characteristics of 20dB/decade in frequency noise). FPM has a slope of -1 which resembles a high pass characteristics of 10db/decade in frequency noise. Any slope intermediary to the two has a high pass filter frequency roll of which is in between 10dB/decade and 20db/decade.

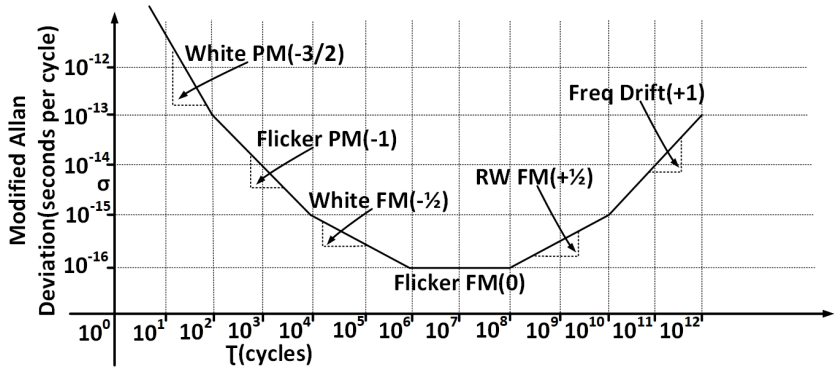


Figure 4.1: Modified Allan Deviation

If there is no discontinuity in the phase stability characteristics, then integration of frequency stability can be used as a measure to project the phase stability of the oscillators as shown in Figure 4.2. It can be seen that White FM has phase stability deterioration by a slope of 1/2 in log-log plot which is the same as predicted by the random walk model in Equation 4.10. Flicker FM noise deteriorates the phase stability by a slope of 1 in log-log plot. Any behavior, which filters the noise results in an improvement in phase stability over time.

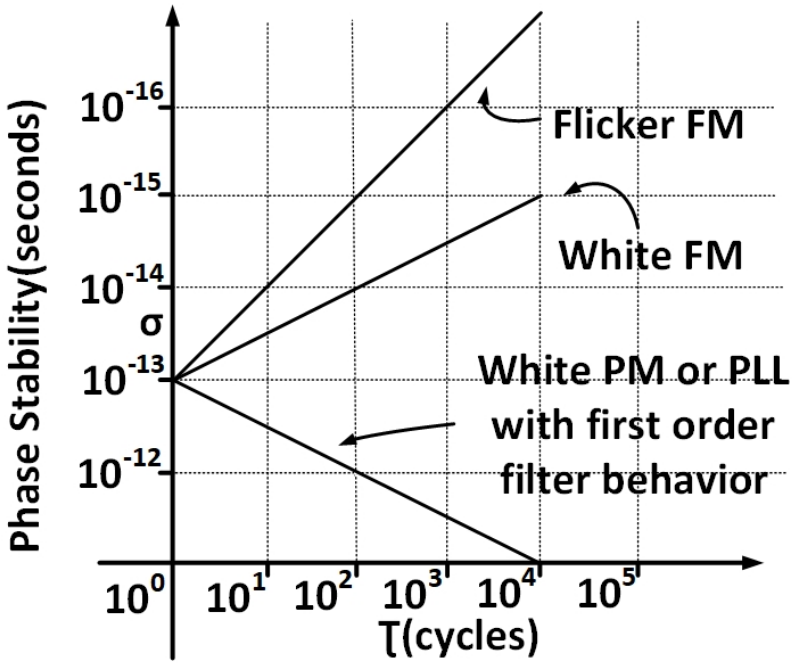


Figure 4.2: Phase Stability from Allan Deviation

4.5.3 PLL or PLL like Stability Improvement

The initial high (more negative) slope in the frequency stability plot is a result of frequency noise filtering characteristics. The systems described in this work have high initial slope in their frequency stability plot. This stability plot resembles a high gain (for a given bandwidth) phase locked loop(PLL) as shown in Figure 4.3. The interesting feature is the existence of PLL like behavior without any external reference. The reasons for this PLL like behavior are explained later. Here, Modified Allan variance is shown to be a viable method to visualize such a behavior.

4.5.4 Region of Interest

Three characteristics from modified Allan deviation plot need to be considered for stability analysis of oscillators with PLL like self stabilization/locking.

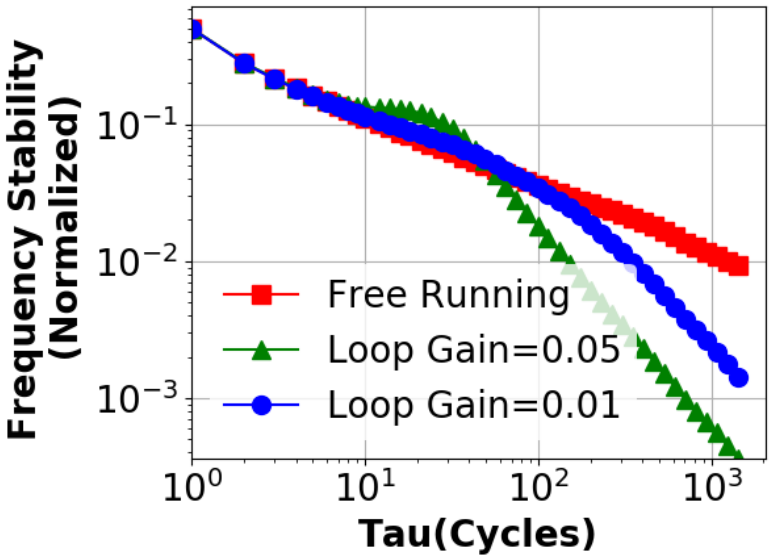


Figure 4.3: Phase Locked Loop Frequency Stability improvement

Self Locking Slope

The magnitude of the initial slope directly relates to how much stability improvement happens over consecutive cycles. This is shown by β_{self} in Figure 4.4.

Self Locking Cycles

The number of cycles over which the oscillator maintains the initial high slope of self locking is effectively the time to which oscillator stability improves. This is shown by τ_{self} in Figure 4.4.

Initial Jitter

Initial single cycle jitter is the value from which the high initial slope starts to improve the stability. If the initial value is bad, them the effect of improvement using self locking is reduced. This value is same as cycle to cycle jitter for 1 cycle.

Figure of Merit

Optimal improvement in stability is achieved when there is minimum initial jitter and there is high initial slope β_{self} magnitude for large number of cycles τ_{self}. For this purpose a figure of merit (FOM) is defined as given by Equation 4.21. It is equivalent to a ratio of integrated phase error over single cycle phase error.

$$FOM = \frac{|\tau_{self} . \tau_{self}|}{\Delta T_{cc}} \tag{4.21}$$

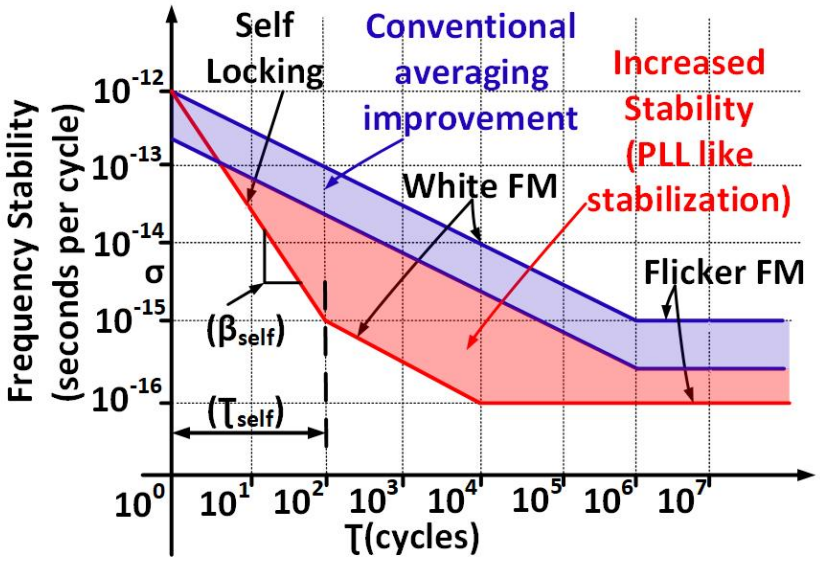


Figure 4.4: Improvement over conventional methods

4.5.5 Simulation

HSPICE transient noise simulations were used to estimate and analyze the oscillator. A long single run of simulation was performed. Computation algorithm was then run on the data. Only the values which were less than 1 percent error were taken for analysis. Since the noise filtering behavior in the system is observed in very small timescales ($\approx$

10s of cycle), simulation projections for only ≈ 100s of cycle were computed. 1000ns runs are easily done in simulations. This provides valid data for ≈ 1000 cycle for the frequency range analyzed in this work. This in turn results in less than 1 percent computation error for ≈ 100 cycles. This easily lets us project errors in ≈ 10 cycles were the filtering is observed.

4.5.6 Measurements

Infinium V-series scope was used for Direct Digital Sampling and data was then post processed in a computer. The scope has an inbuilt oscillator with jitter specification of less than 300fS. Effective Number of Bits (ENOB) of the oscillator is only about 6 at the measurement frequencies (5GHz). ENOB matters less in the measurement as the input signal can be large swing and the outputs are interpolated while the computation is done.

Possible Improvements in Measurement

The measurements are only limited to the jitter specifications of the oscillator (if the care is taken to probe them very closely, otherwise also the jitter build up in the buffering path and output pads). So, future research improvements will be bounded by this oscillator jitter specification. In-order to get around this, on chip autocorrelation circuitry needs to be made. This will let us probe the oscillator stability in the order of 10s of femtoseconds.

4.6 Conclusion

Different timing stability metrics were reviewed. Modified Allan Deviation was shown to be a viable metric for analysis of the oscillator behavior in this work. Figure of Merit for

self stabilized oscillators discussed in this work was proposed. Methodology for simulation and measurement of Modified Allan Deviation with regards to this work was discussed.

Chapter 5

Behavioral Analysis

The design space presented by the system is very complex and non-linear with many interacting parameters. This necessitated the development of a behavioral tool which can predict to first order the effects of different design parameters on the timing stability. The tool aims to show that delay-vs-separation dynamics in each gate (presented in the previous chapters) are sufficient to result in timing stability improvement. The timing stability improvement observed has the same trend and approximate magnitude as that of simulations done from HSPICE. This chapter explains the development of the behavioral tool. It then presents an empirical relationship between different design parameters and their effect on timing stability improvement.

5.1 System Level Model

As discussed in previous chapters, pulse gates amplifiers have a dynamics associated with them. This dynamics when used in a loop results in a system level picture as shown in Figure 5.1. Notice that, three major design parameters show up due to this design picture, namely, number of pulses(M), slope of delay modulation function η and

number of pulse gates per pulse (N/M). Note that in actual circuit implementations these parameters may be dependent on each other. In this analysis these have been treated orthogonal to each other to get a sense of design space for the designer as shown in Figure 5.2.

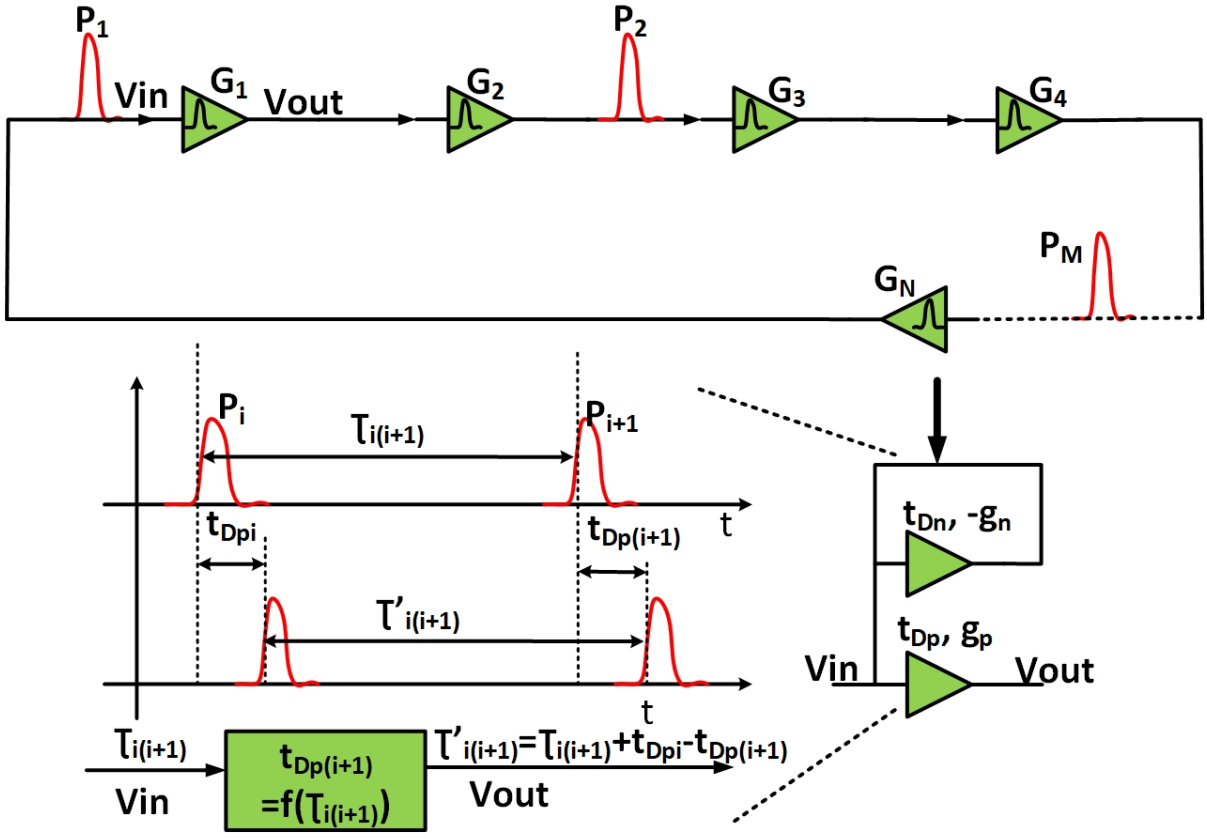


Figure 5.1: System Level Model of Pulse Oscillators

5.2 Noise Model

In-order to simulate the global effects of local dynamics when put into a loop, appropriate discrete time noise models were needed. While white noise is stationary and can easily be modeled in almost all the simulators, any other noise of $\alpha <= 2$ are non

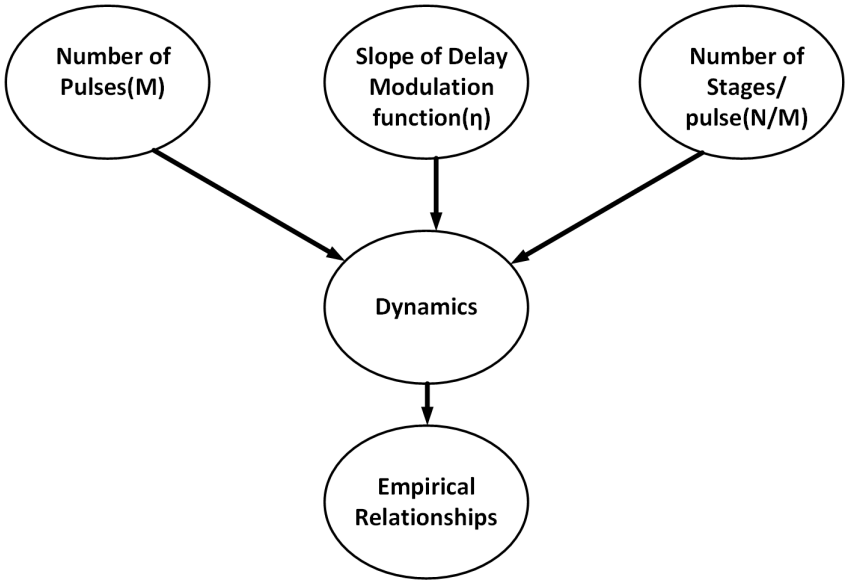


Figure 5.2: Behavioral Model and Empirical Relationships

stationary. So, discrete time noise models developed in [40] were used. The work uses autocorrelation of different noise models to give a correct frequency domain representation of noise (based on the time series generated by it). It does it by assuming the autocorrelation functions to be symmetric about origin and then approximating them as deviations from Brownian motion. The work is highly cited and accepted as a form of discrete time model for noise sources and hence was selected to be enough to validate the concepts in this work.

5.2.1 Noise Simulation

Figure 5.3 shows the Allan deviation of different noise models obtained from behavioral simulator and the use of discrete time noise models from [40]. It shows that the White FM and Flicker FM noise sources needed as part of this work are correctly modeled using the noise models and Allan deviation representation of the noise models is correct and matches those described in the previous chapters.

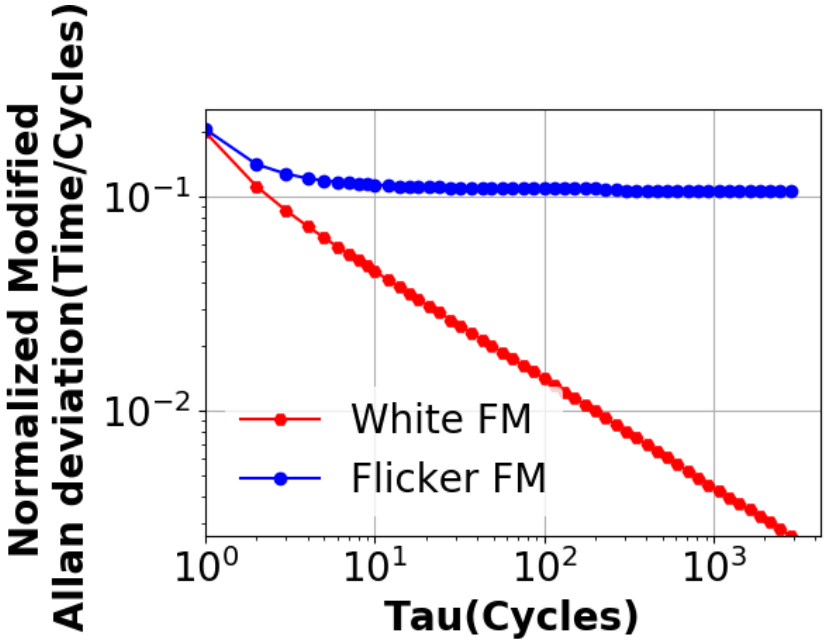


Figure 5.3: White FM and Flicker FM Modified Allan Deviation (Normalized to Noise of 0.1 magnitude)

5.3 Oscillator Model

We care about phase stability in this work. Phase is the sum of oscillator periods as given by Equation 5.1. In pulse oscillators, for the case of 1 Pulse period is the sum of forward delays for all the stages (N) as given by Equation 5.2. For the case of M pulse, each pulse passes through N delays stages. The time taken to traverse the loop by each pulse is the sum of delays of each stage encountered by that specific pulse. Phase equation for a such a case is presented after going through a 2 pulse 2 stages example next. In such an oscillator, phase error after some number of cycles (K) is given by the difference of actual phase and mean phase as given by Equation 5.3.

$$\Phi = \sum_{n=1}^{\infty} T_n \tag{5.1}$$

$$T_n = \sum_{n=1}^{N} t_{Dp} \tag{5.2}$$

$$\Phi_{err} = \Phi - \sum_{n=1}^{K} T_{mean} \tag{5.3}$$

5.4 Example

In-order to visualize the effect of gate dynamics on oscillator timing uncertainty, a simple abstraction of the oscillator is chosen as shown in 5.4a. Following assumptions are made in the example:

- Two pulses are traveling around a loop of two pulse gates
- The system has two states:
    1. P_1 at the input of gate G_1 and P_2 at the input of G_2
    2. P_2 at the input of gate G_1 and P_1 at the input of G_2

For the simulation case, it is assumed that the pulses are in steady state with no noise to begin with. Two cases are considered:

$$t_{Dp} = 0.5 \times \tau + 50 \tag{5.4}$$

$$t_{Dp} = -0.5 \times \tau + 150 \tag{5.5}$$

$$t_{Dp} = \frac{N}{M}\tau = \frac{2}{2}\tau = \tau \tag{5.6}$$

- Attraction as shown in 5.5a. The oscillator operates at the intersection of Equation 5.4 and Equation 5.6.
- Repulsion as shown in 5.5b. The oscillator operates at the intersection of Equation 5.5 and Equation 5.6.

Both cases are setup such that at steady state with no noise oscillators have a period of 100 units, hence a pulse to pulse separation of 100 units for both pulses. Both gates have a nominal delay of 100 units under such a condition as pointed out by the intersection points.

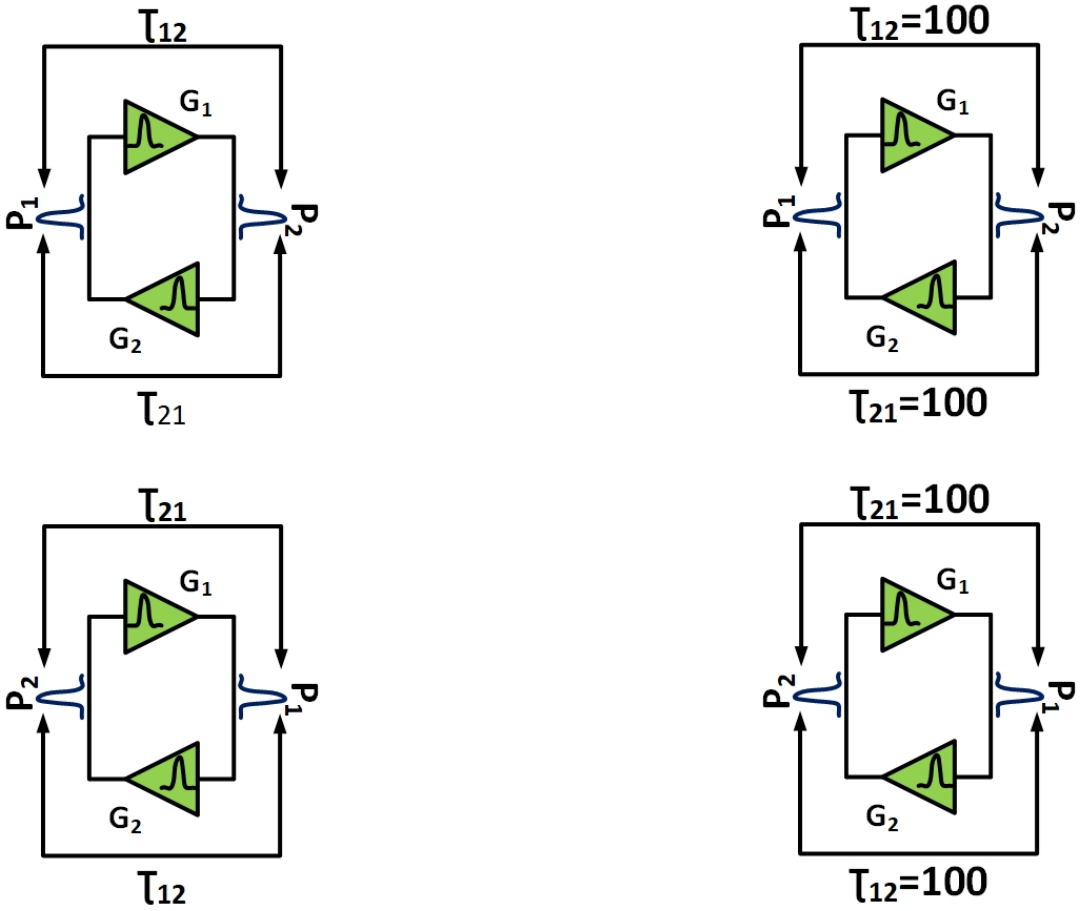
5.4.1 State Equations

The example oscillator has two state described before based on the position of the pulses with respect to the gates. In state 1, the oscillator follows the Equation 5.7 and Equation 5.8 for pulses P_1 and P_2 respectively. In state 2, the oscillator follows the Equation 5.9 and Equation 5.10 for pulses P_2 and P_1 respectively. In these equations:

1. New separation between the pulses is computed by adding the change in delay. Change in delay is the difference of delay of current pulse (computed of the current separation) and delay of the last pulse.
2. Gate delay is updated to that of the pulse which passed through the gate.
3. Separation of the pulse is updated to the new value computed.

$$\tau'_{12} = \tau_{12} + f(\tau_{12}) - t_{dp1}; t_{dp1} = f(\tau_{12}); \tau_{12} = \tau'_{12} \tag{5.7}$$

$$\tau'_{21} = \tau_{21} + f(\tau_{21}) - t_{dp2}; t_{dp2} = f(\tau_{21}); \tau_{21} = \tau'_{21} \tag{5.8}$$



(a) Simple oscillator abstraction

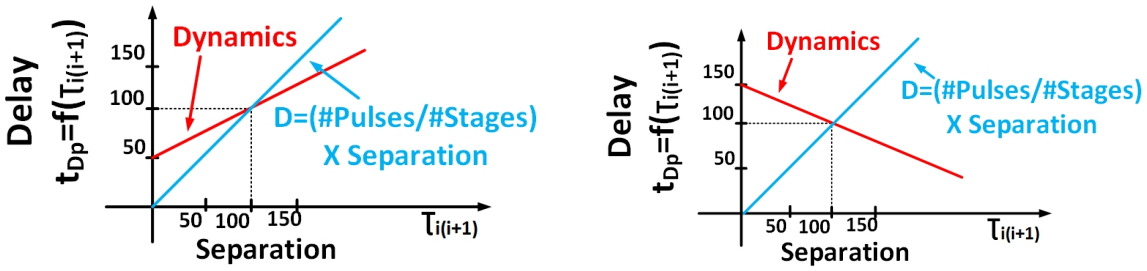
(b) Simulation case

Figure 5.4: Two state oscillator example

$$\tau'_{21} = \tau_{21} + f(\tau_{21}) - t_{dp1}; t_{dp1} = f(\tau_{21}); \tau_{21} = \tau'_{21} \tag{5.9}$$

$$\tau'_{12} = \tau_{12} + f(\tau_{12}) - t_{dp2}; t_{dp2} = f(\tau_{12}); \tau_{12} = \tau'_{12} \tag{5.10}$$

It is claimed that, under such a condition, period of the oscillator is the separation between pulses. Any reference point can be chosen (say $inputofG_1 = outputofG_2$). Then, each time a pulse arrives at this reference point, its separation is the period of



(a) Attractive dynamics (b) Repulsive dynamics

Figure 5.5: Stable operating point

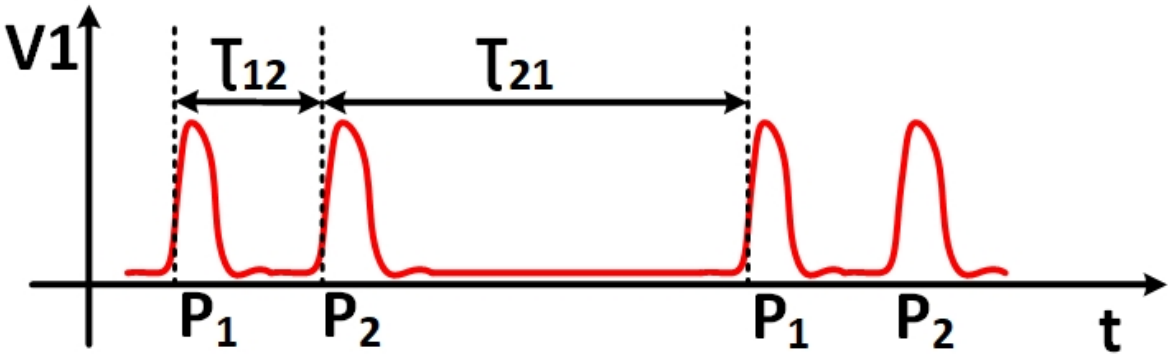


Figure 5.6: Period and Pulse separation are equivalent in case of 2 pulse case

the oscillator. It is easy to visualize this by thinking about a case of two crowded pulses traversing an oscillator loop as shown in Figure 5.6. In such a condition the period marked at node V1 (usually computed as the time between rising edges) would be alternating be high and low. This is the same as separation between the two pulses as claimed in this work.

5.4.2 Impulse Noise

For the ease of visualization of the two possible dynamics(Attraction and Repulsion), an impulse noise case is considered. In-order to make the visualization easier, a symmetric case is considered, i.e. a change of separation of P_1 to 101 from 100 and a change of

separation of P_2 to 99 from 100.

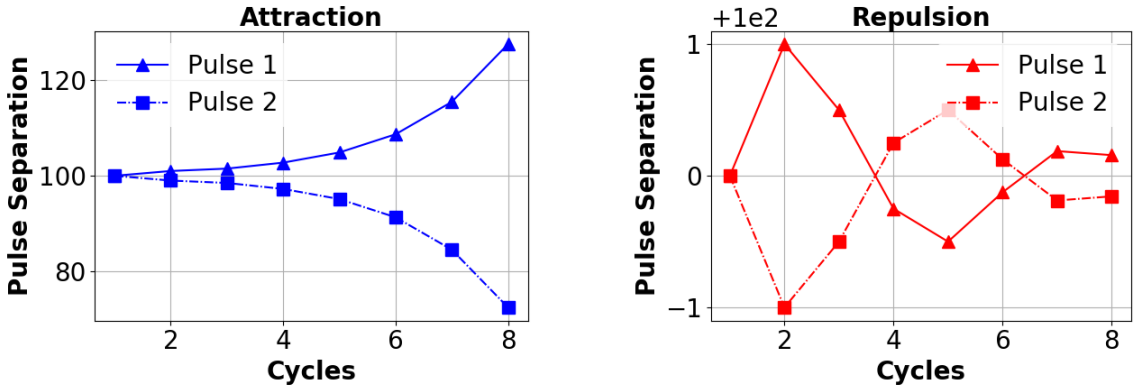
Attraction

Separation of the two pulses from the other one in case of attractive dynamics under the influence of impulse noise is shown in 5.7a. It can be seen that pulses just diverge from the nominal separation. It is due to the fact that a pulse with smaller separation (than nominal) has a smaller delay (than nominal) and pulse with larger separation (than nominal)has a larger delay (than nominal). Phase error can be seen to be diverging. This behavior in an actual circuit implementation cannot persist indefinitely. This leads to eventual pulse evaporation. Conventional amplifiers (inverters or differential amplifiers) have either constant or attractive dynamics (originating from amplitude limitation). Therefore, even if we start a inverter based ring oscillator into a mode where there are mode than one edge traveling around the loop, it eventually reverts back to a single edge mode.

Repulsion

Separation of the two pulses from the other one in case of repulsive dynamics under the influence of impulse noise is shown in 5.7b. It can be seen that pulses converge back to their nominal separation. It is due to the fact that a pulse with smaller separation (than nominal) has a larger delay (than nominal) and pulse with larger separation (than nominal)has a smaller delay (than nominal). Phase error can be seen to be converging. The converging value is less than 1 (which would have resulted from a conventional constant delay case).

Attractive dynamics results in unstable systems. Repulsive dynamics result in oscillators with phase error smaller than a constant delay case for an impulse noise. Further analysis in this work has only been done with repulsive dynamics due to their stable



(a) Attraction (b) Repulsion

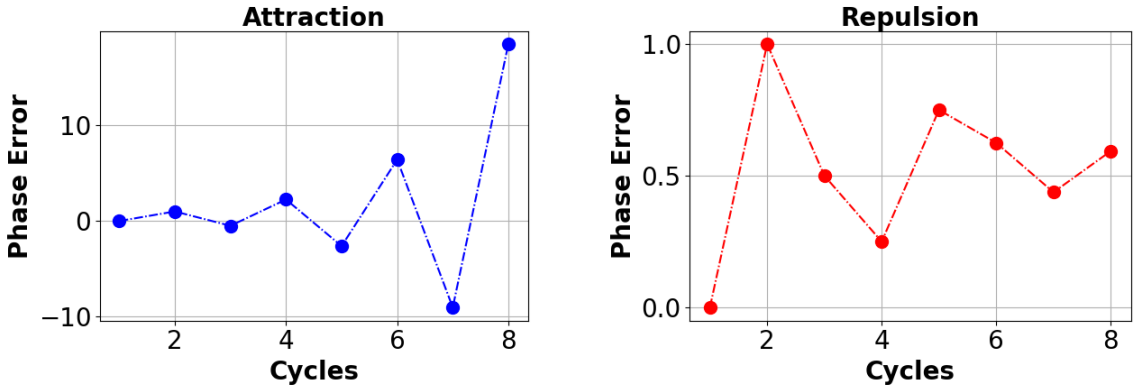
Figure 5.7: Phase Error under impulse noise of magnitude=1

behavior. Next, a case with actual oscillator with noise at all gates needs to be analyzed. This analysis needs to be done for different noise types and for different system design parameters.

5.5 Behavioral Tool

Figure 5.9 describes the basic setup of the behavioral tool. The basic tool construction is as following :

- Pulses are assumed to be traversing a loop of pulse gates as shown in Figure 5.1. Timing is computed at input of the pulse gates.
- Black Box interpretation of gates is assumed. Each black box only computes the timing of the output pulse based on the timing of the pulse at its input and the separation of the input pulse from the last pulse at the gate.
- Every Pulse has a separation from the pulse in front associated with it. Every gate in the Loop has a delay(of the last pulse which passes through it) associated with



(a) Attraction (b) Repulsion

Figure 5.8: Pulse Separation under impulse noise of magnitude=1

it.

- All gates have a noise source associated with them. This noise source can be either White FM or Flicker FM
- For ease of simulation number of gates per pulse is kept a natural number.

The simulator has a the following flow (Figure 5.10):

1. Since each pulse is assumed to be at input of some gate, compute the delay of all the pulses based on the delay-separation model of each gate. The only value necessary to compute this delay is separation from the pulse in front. This value is always associated with the pulse.
2. Separation of all the pulses are updated by adding the change in delay of the pulse.(Change in delay is the difference of current delay minus the last pulse delay associated with the gate.)
3. Noise associated with each gate is added on the values of separation of each pulse.

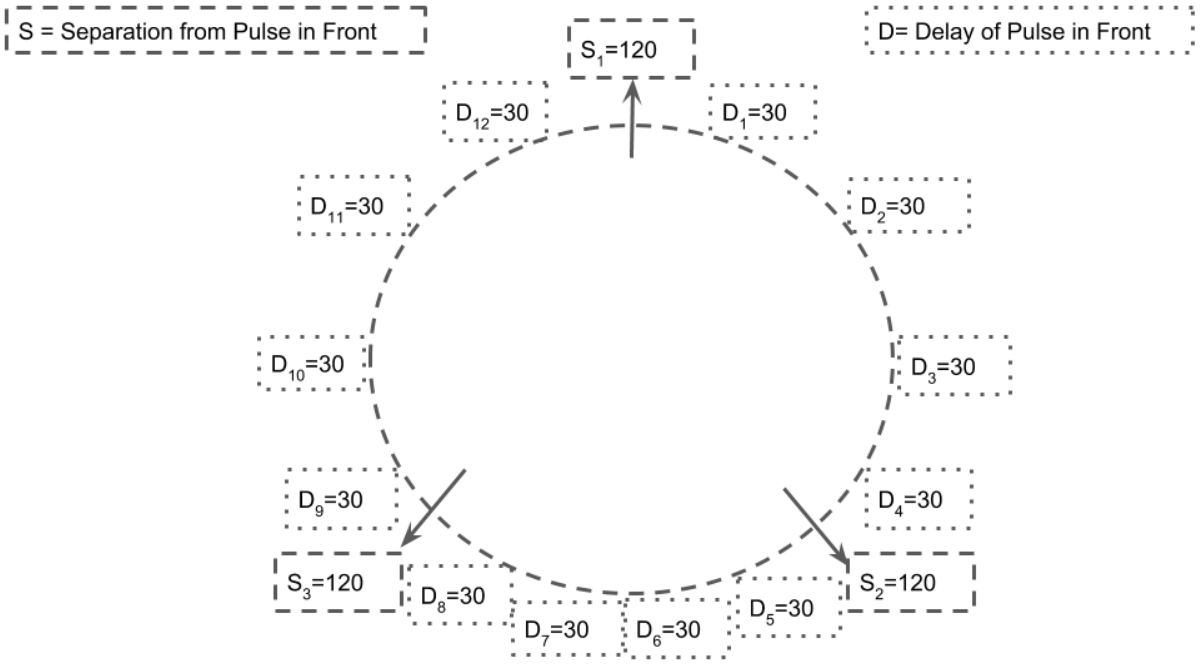


Figure 5.9: Behavioral Tool Setup

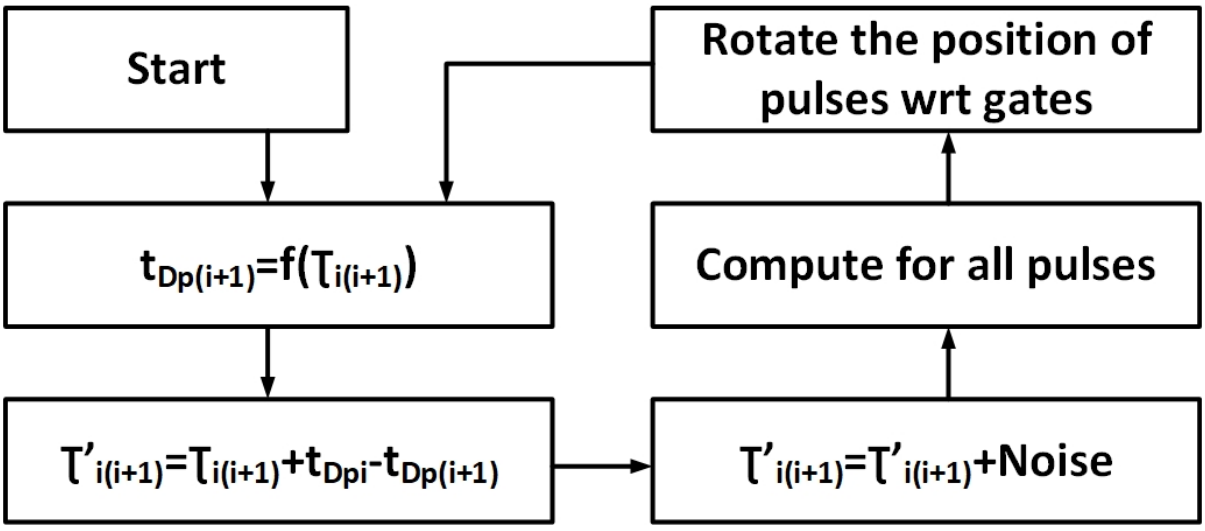


Figure 5.10: Behavioral Tool Flow

4. Delay associated with each gate is updated as the value of the last pulse which passed through the gate.

5. Position of the pulses with respect to the gates is update.

6. Steps 1 to 5 are repeated for number of cycles being analyzed.

Discrete noise series generated by using algorithm described in [40] are used in the behavioral tool to simulated oscillator noise simulation. The flow followed to account for the oscillator noise addition is shown in Figure 5.10. Noise is added to the separation values every time a new separation value is computed by passing through a gate. The nature of this noise can be different and different noise have different behavioral characteristics at the output as analyzed in the next section.

5.6 Results

Effects of White FM and Flicker FM noise was analyzed for different system characteristics (M, η, and N/M).

5.6.1 White FM

White FM noise has a slope of -1/2 in log-log modified Allan deviation plot. Different design parameters have different effects on the slope for different timescales as shown next.

Slope of delay modulation η

Effect of increase in the slope of delay modulation function η on the timing stability for a White FM noise source is seen in Figure 5.11. The results are compared for a case with 4 pulses and 4 stages per pulse case. The base case with constant delay is only

stable for 1 pulse has been shown as a reference point. It can be seen that with increase in η, both the self locking slope β_{self} and self locking cycles τ_{self} increases. It can also be observed that timing stability for shorter timescales becomes worst for higher η but eventually is better for longer timescales.

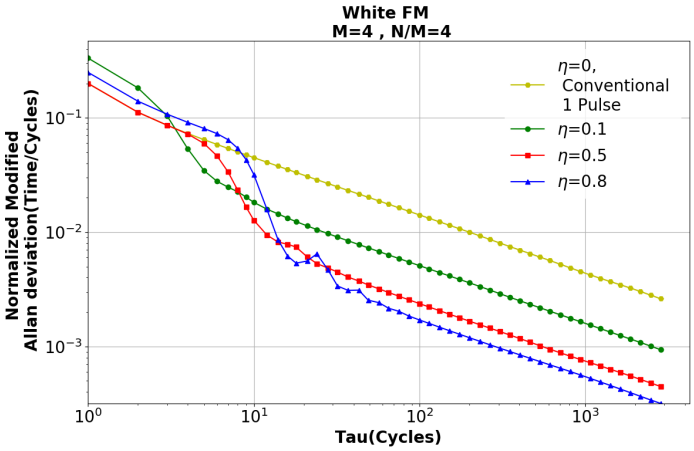


Figure 5.11: Modified Allan Deviation as a measure of timing stability for different delay modulation function slopes

Number of Pulses(M)

Effect of increase in number of pulses(M) on the timing stability for a White FM noise source is seen in Figure 5.12. The results are compared for a case of 4 stages per pulse and a delay modulation function with a slope of 0.2. It can be seen that both β_{self} and τ_{self} increase with the increase in number of pulses. It can also be observed that timing stability for shorter timescales becomes worst for higher M but eventually is better for longer timescales.

Number of stages per pulse (N/M)

Figure 5.13 shows the effect of change in number of stages per pulse (for White FM noise, 2 Pulses and η=0.2) on the timing stability.

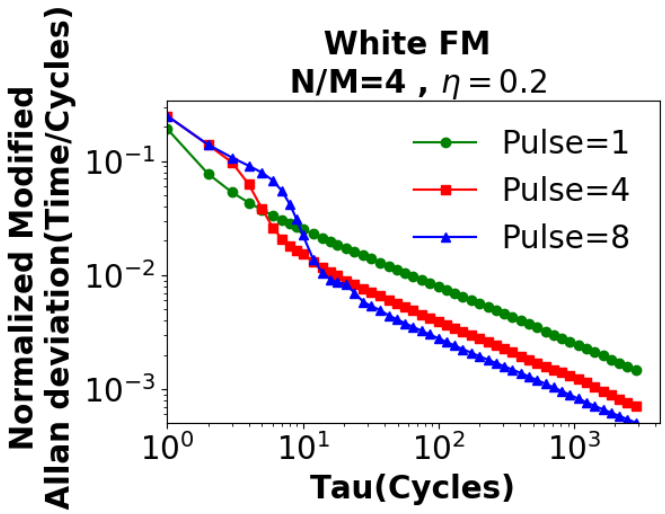


Figure 5.12: Modified Allan Deviation as a measure of timing stability for different number of pulses

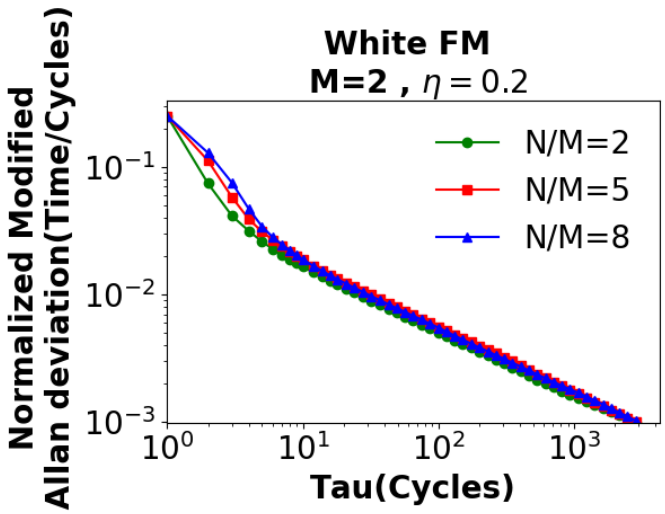


Figure 5.13: Modified Allan Deviation as a measure of timing stability for different number of stages per pulse

5.6.2 Flicker FM

Flicker FM noise has a slope of 0 in log-log Modified Allan deviation plot. Different design parameters have different effects on the slope for different timescales as shown next.

Slope of delay modulation η

Effect of increase in the slope of delay modulation function η on the timing stability for a Flicker FM noise source is seen in Figure 5.14. The results are compared for a case with 4 pulses and 4 stages per pulse case. The base case with constant delay is only stable for 1 pulse has been shown as a reference point. It can be seen that with increase in η, both the self locking slope β_{self} and self locking cycles τ_{self} increases. It can also be observed that timing stability for shorter timescales becomes worst for higher η but eventually is better for longer timescales.

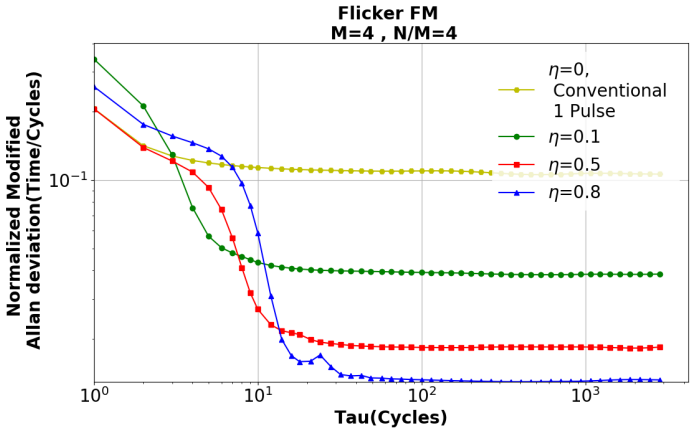


Figure 5.14: Modified Allan Deviation as a measure of timing stability for different delay modulation function slopes

Number of Pulses(M)

Effect of increase in number of pulses(M) on the timing stability for a Flicker FM noise source is seen in Figure 5.15. The results are compared for a case of 4 stages per pulse and a delay modulation function with a slope of 0.2. It can be seen that both β_{self} and τ_{self} increase with the increase in number of pulses. It can also be observed that timing stability for shorter timescales becomes worst for higher M but eventually is better for longer timescales.

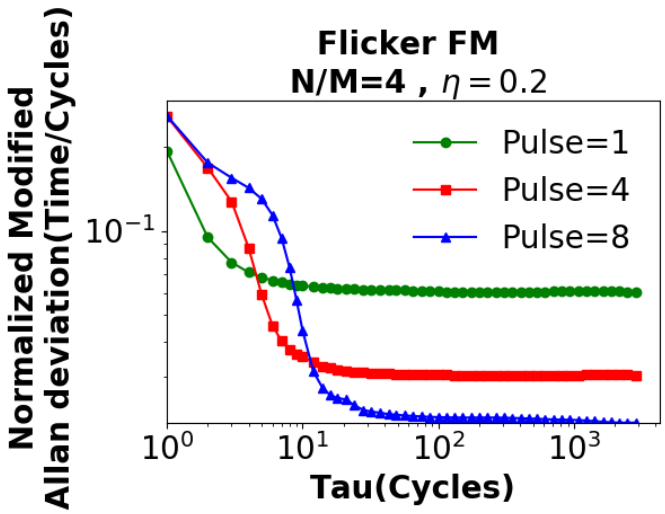


Figure 5.15: Modified Allan Deviation as a measure of timing stability for different number of pulses

Number of stages per pulse (N/M)

Figure 5.16 shows the effect of change in number of stages per pulse (for Flicker FM noise, 2 Pulses and η=0.2) on the timing stability.

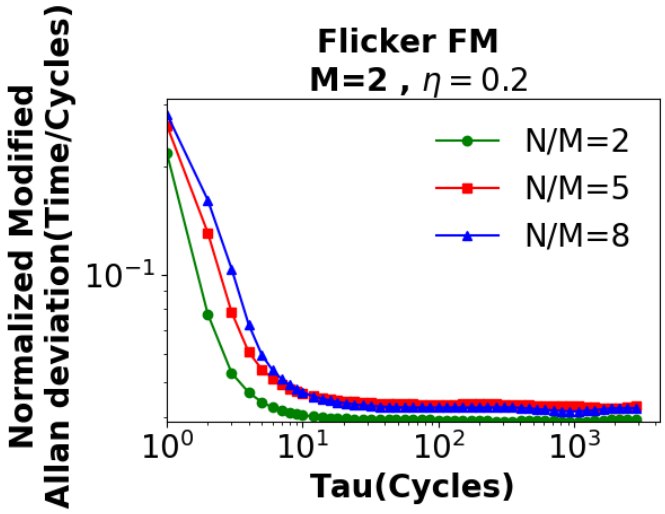


Figure 5.16: Modified Allan Deviation as a measure of timing stability for different number of stages per pulse

5.7 Conclusion

Presence of dynamics in gates was shown to have an impact on the timing stability behavior of ring oscillators. The impact results in improvement in timing stability when the dynamics are repulsive (negative slope delay-vs-separation). Behavioral tool to study the impact of dynamics was developed. Effects of different design parameters on the timing stability improvement was visualized. The optimal design point using a Figure of Merit is computed in later chapters after looking into different architectures and designs of pulse oscillators.

Chapter 6

Ring Oscillator: Conventional Design and Analysis

6.1 Introduction

Distribution of high frequency, low jitter, timing signals over long distances consumes substantial power, motivating small localized synchronizing oscillators that maintain the system global coherence. Ring oscillators are used universally for the purpose of local oscillators due to their small footprint. Ring oscillators made of inverter chains have been shown to have substantially larger phase noise than a LC oscillator at the same power budget due the the larger inherent Q of the LC resonator[18]. Unfortunately, this improvement comes at a substantial cost in layout area and potential for EMI interference. This chapter introduces a shape-preserving pulse regeneration buffer based oscillator to achieve a large phase noise performance improvement in a footprint and power level equal to that of a conventional ring oscillator. CMOS pulse-gates have long been used in high performance digital circuits such as the Intel Pentium 4 and more recently in low power, high-speed serial links [41] because of their high timing repeatability. Pulse-gate

triggering is sensitive only to the rising edge integrated charge (not the pulse amplitude or width once the trigger threshold is reached)[38]. Further, the output pulse width is largely insensitive to the input width. These properties act to reduce the root mean square value of Impulse Sensitivity Function [15], resulting in substantial phase noise improvement over inverter and linear amplifier based delay elements when used as an oscillator. Further, the signals are buffered (double inversion) [42] leading to improved high-frequency supply noise rejection. Pulse-gates do have an asymmetric ISF and thus exhibit slightly higher flicker phase noise sensitivity.

6.1.1 Applicability

The design and analysis of pulse ring oscillator in this chapter is applicable under the assumption of constant delay. The effects of delay modulation explained in previous chapters is not explored in this chapter. The chapter aims to explain the benefits and design intricacies of a ring oscillator when constructed out of a pulse gate. The results arising from delay modulation in gates are presented in a later chapter.

6.2 Concepts

6.2.1 Impulse Sensitivity Function Shaping

The Impulse Sensitivity Function(ISF) [15], Γ, is widely used for estimating the phase noise characteristics of an oscillator. ISF measures the effect of injecting noise in the form of a small current impulse on a given internal circuit node, on the phase change in the oscillator.

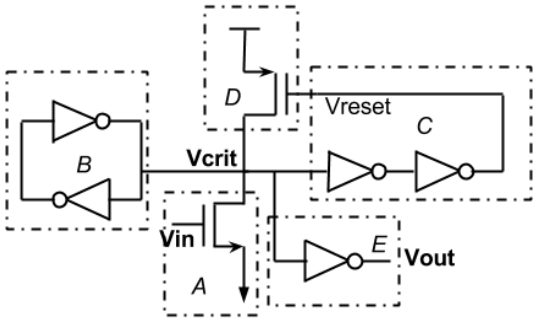


Figure 6.1: Pulse Gate Circuit

Rising Edge based Timing

[15] showed that root mean square value of the ISF, Γ_{rms}, determines the magnitude of phase noise $L\{\Delta\omega\}$ at a frequency offset $\Delta\omega$. The DC component of ISF, Γ_{dc}, determines the shift of the flicker noise corner frequency $\omega_{\frac{1}{f}}$ to higher frequency $\omega_{\frac{1}{f^3}}$ in phase noise characteristics. Exact equations are given by Equation 6.1 and Equation 6.2, where q_{max} is the maximum charge at the node where ISF was measured and $\frac{\overline{i_n^2}}{\Delta f}$ denoted the total noise current.

$$L\{\Delta\omega\} = \frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\frac{\overline{i_n^2}}{\Delta f}}{2\Delta\omega^2} \tag{6.1}$$

$$\omega_{\frac{1}{f^3}} = \omega_{\frac{1}{f}} \cdot \frac{\Gamma_{dc}^2}{\Gamma_{rms}^2} \tag{6.2}$$

To achieve the best oscillator phase noise performance, both Γ_{rms} and Γ_{dc} must be small. Conventional amplifiers used in oscillator designs are sensitive to both rising and falling edges of the signal. For symmetric rising and falling drive Γ_{dc} is almost negligible. However, this symmetry is achieved at the cost of a substantial increase in Γ_{rms}, since the oscillator is sensitive to noise across a larger part of the cycle. The Pulse-gate amplifier shown in Figure 6.1, is sensitive only during the rising edge of its

input. Indeed, the amplifier is designed to trigger before the input voltage reaches it maximum amplitude reducing sensitivity to input pulse amplitude. This greatly reduces Γ_{rms} but its inherent asymmetry increases Γ_{dc}. In practice, this problem can be easily compensated by phase locking the oscillator to a stable low-frequency source using PLL techniques. This eliminates the flicker noise shift in the phase noise plot. Effectively, the technique maximizes the rising-edge slew rate independently of the total phase lag, and makes the phase delay insensitive to all other effects.

6.2.2 Common Mode Noise Rejection

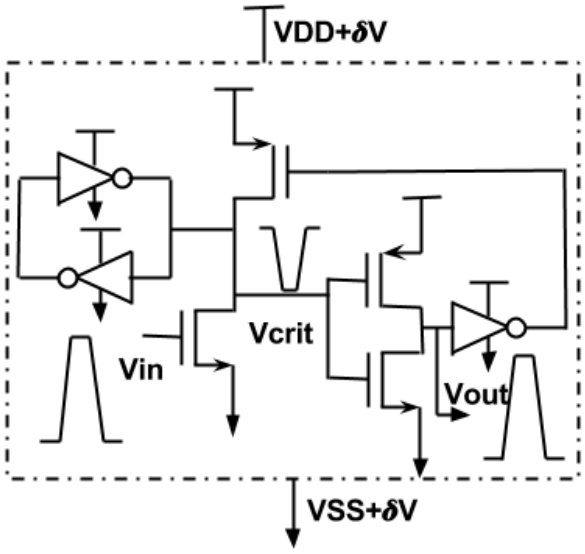


Figure 6.2: Common mode power noise

Chen et.al.[42] showed that single stage amplifiers (like inverters) are more adversely affected by common mode supply noise (VDD and VSS) than by differential mode supply noise. In large-swing buffers, saturation current (inversely proportional to delay) is determined by gate-source voltage and drain-source voltage. Common mode noise shifts VDD and VSS for the amplifier shown in Figure 6.2 by a voltage, δV. The two threshold effects oppose each other in buffers, mitigating the delay (and thus phase)

modulation. This same effect is present in Figure 6.2 and compensates for drain-source voltage as well.

6.2.3 Improvement over Inverter based Ring Oscillator

In an oscillator made of inverters, any phase change in either rising or falling edges accumulates in the loop and creates a phase error. In a pulse ring oscillator only the rising edge phase error accumulates (The simulated falling edge triggered by V_{reset} node has a ISF function a factor of 10 smaller than the rising edge).

If a pulse ring oscillator is constructed out of N pulse-gates, in all of the N gates, every rising at V_{in}, creates a falling edge at V_{crit} which creates a rising edge at V_{out} (which is V_{in} of next gate). Hence there are N noise sources at V_{in} and N at V_{crit} . Note that a pulse ring oscillator can operate with both even or odd number of pulse gates. Also in both cases, rising edge sees $2N$ noise sources.

A ring oscillator made of inverters needs to have an odd number of gates. For it to have a comparable frequency of operation to that of pulse ring oscillator, the number of inverters needs to be either $2N-1$ or $2N+1$. This implies that every rising and falling edge passes $2N(+/-)1$ stages. Thus total nodes where noise can get added is two times $2N(+/-)1$.

Thus phase noise of Pulse ring oscillator is smaller than inverter ring oscillator by a factor of 2 (for large N) :

$$PN_{Improvement} = 20log(\frac{2N(+/-)1}{N}) \approx 6dB \tag{6.3}$$

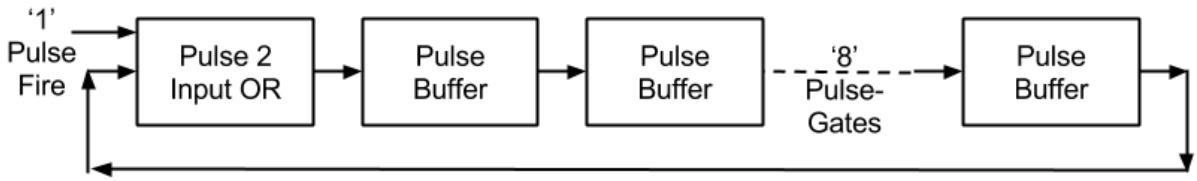


Figure 6.3: Pulse ring oscillator with a ring of '8' Gates

6.3 Oscillator Design

Pulse gates have the circuit design shown in Figure 6.1. The gates are connected as shown in Figure 6.3 making a simple ring oscillator. An 'OR' pulse-gate has 2 pull down NMOS instead of a single one and the extra input is used to start the pulse in the ring.

6.3.1 ISF Based Design Analysis

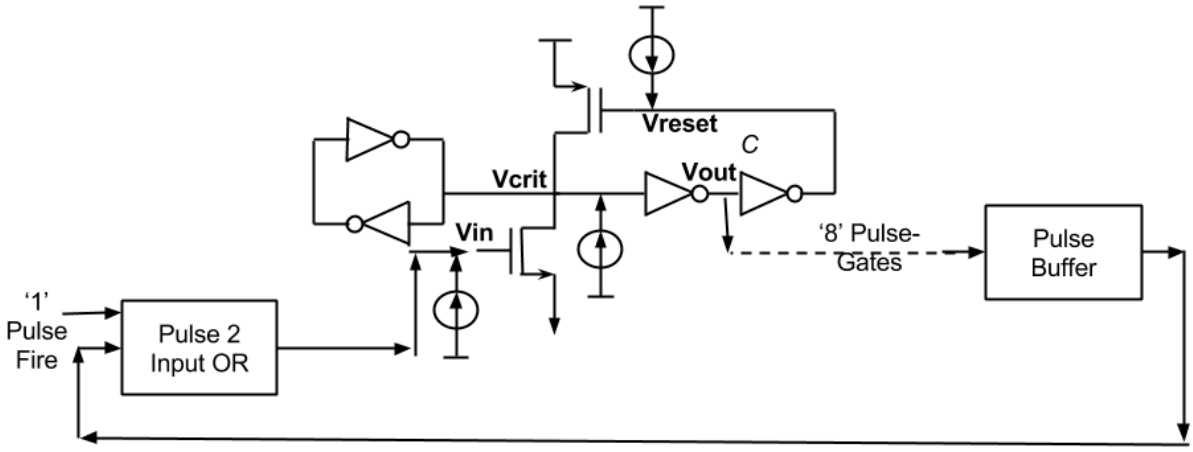


Figure 6.4: ISF measurements by current impulse injection at three possible nodes: V_{in}, V_{out} V_{reset}

A current impulse was injected into different nodes in the pulse gate as shown in Figure 6.4. ISF predicts the phase noise under the assumption that phase change to the injected noise impulse is linear and amplitude variations do not result in substantial phase shift. Since the design is based on a saturating amplifier, the second assumption

is true.

Linearity to current impulse

Linearity of the phase change to the current impulse charge can be seen in Figure 6.5. For further ISF analysis, charge value of 2.8fC was chosen as it lies in the linear region.

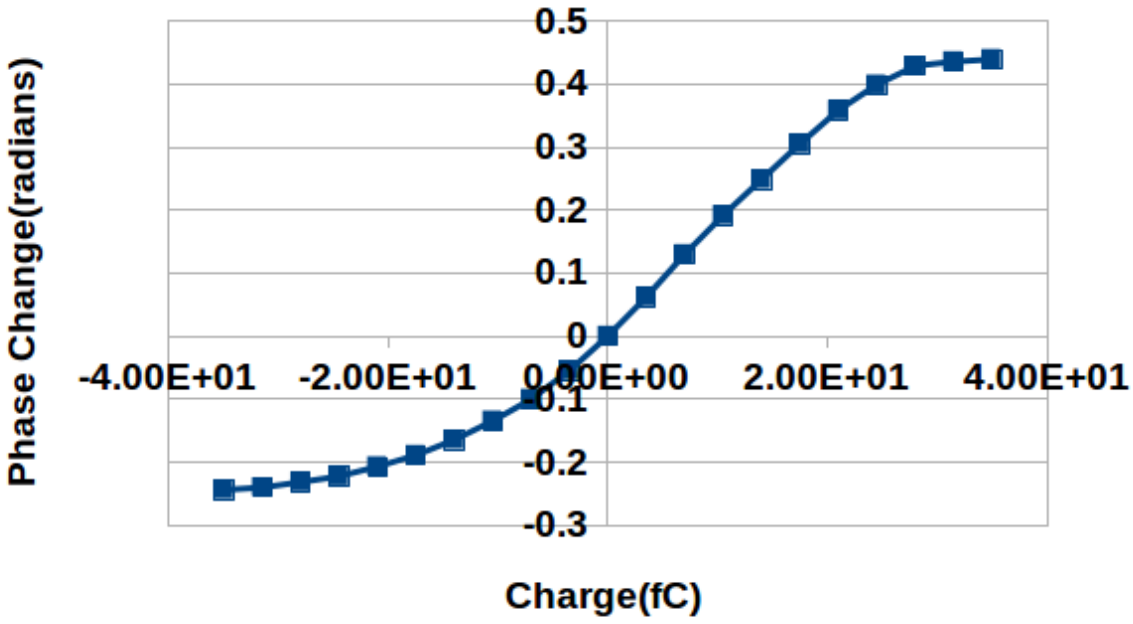


Figure 6.5: Response of ISF to charge injection between $+/-10fC$

Nodes With Impulse Sensitivity

V_{reset} results in a phase change which is approximately 10 times smaller than the phase change seen at V_{in} (which is V_{out} of the previous stage) and V_{crit} for a given impulse charge. Hence, only V_{in} and V_{crit} were used for further ISF analysis.

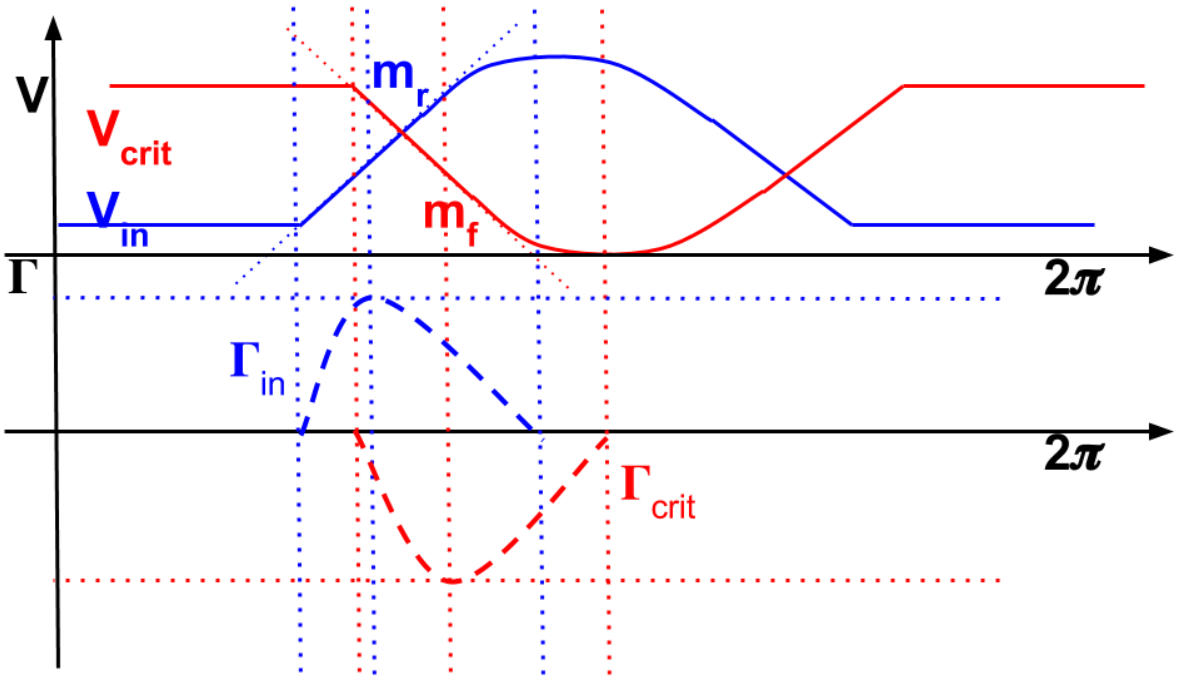


Figure 6.6: Abstract model of ISF at nodes V_{in} and V_{crit}

Shape of the ISF

- @V_{in} : Phase change due to current impulse at V_{in},Γ_{in}, occurs only during the rising edge of the signal. The peak of ISF lies in the middle of the rising edge and its position is dependent on the slope of V_{in}, m_r.

- @V_{crit} : Phase change due to current impulse at V_{crit},Γ_{crit}, is shifted in phase by the delay of V_{in} to V_{crit}. Γ_{crit} has opposite sign compared to that of Γ_{in} and the two overlap in phase as shown in Figure 6.6 and Figure 6.7. Time to peak of Γ_{crit} is again inversely proportional to slope of V_{crit}, m_f.

Noise Current

Since the ring oscillators are non-linear amplifiers with vastly different values of current bias, corresponding noise current is very far from constant. ISF Noise current is

assumed to be constant, hence an appropriate average noise current needs to be picked. To obtain a bound, the noise current was chosen at the biasing level corresponding to the operating point of the peak ISF value.

Design Phase Noise Projection using ISF

Based on the analysis described above $\Gamma_{rms(in)}$ was 0.015 radians and corresponding $\frac{\overline{i_n^2}}{\Delta f}$ was $2 \times 10^{-23} A^2/Hz$. $\Gamma_{rms(crit)}$ was 0.013 radians and corresponding $\frac{\overline{i_n^2}}{\Delta f}$ was $3.2 \times 10^{-23} A^2/Hz$. Separate computation of phase noise at 1MHz offset using Equation 6.1 was done. The values were multiplied by a factor of 8 due to total of 8 buffers being present in the oscillator loop. This computes to a phase noise value of -98.5 dBc/Hz at 1MHz offset for a 2.5GHz oscillator operating of a 1.2V supply.

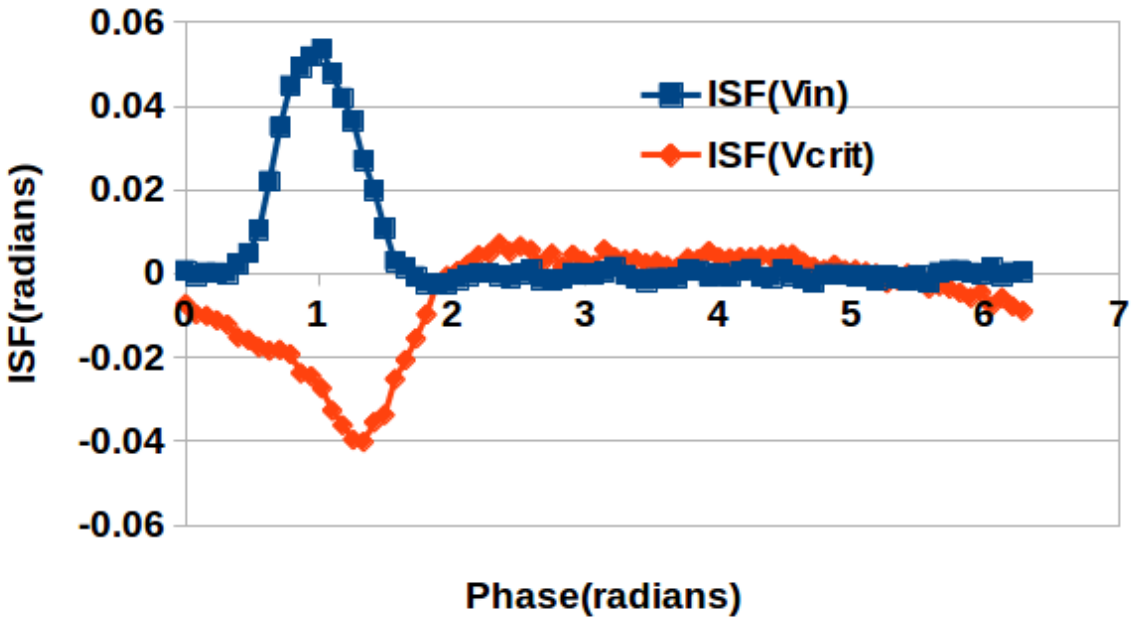


Figure 6.7: Simulated ISF at nodes V_{in} and V_{crit} post layout extraction

6.3.2 Common Mode Rejection

Figure 6.8 shows that the effect of common mode noise is smaller than differential mode noise which is in contrast to inversion type amplifiers as explained in subsection 6.2.2. The effect can be optimized using consecutive stage NMOS to PMOS ratio (but it has opposite effects on positive and negative δV). This work presents the phase noise optimized design, so the idea was to show that the buffers have very good common mode supply rejection.

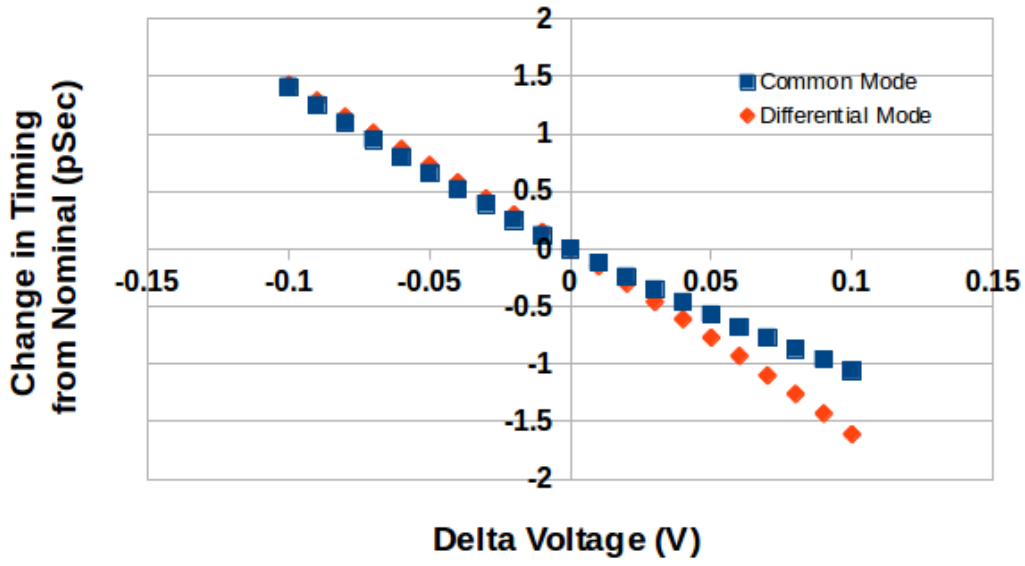


Figure 6.8: Common mode-vs-differential timing change

Table 6.1: Comparison of the simulated and fabricated pulse ring oscillators

Design	Phase Noise @1MHz	Freq
Pulse-Ring Oscillator Simulated	-98.5dBc/Hz	2.5GHz
Pulse-Ring Oscillator Fabricated	-97.46dBc/Hz	1.889GHz

6.4 Results

The oscillator was fabricated in 130nm CMOS technology. The layout is shown in Figure 6.9. A ring of 8 gates is started with an external pulse. The oscillator frequency shows a linear behavior with supply as control voltage as shown in Figure 6.10.

Table 6.2: Fabricated ring oscillator performance comparison

Ref	Technology	Phase Noise	Power	Measurement Frequency
This Work	130nm	-97.46dBc/Hz @1MHz	2.94mW	1.889GHz
[43]	350nm	-126dBc/Hz @10MHz	7.48mW	866.521MHz
[44]	350nm	-116dBc/Hz @10MHz	42.9mW	–
[45]	180nm	-105dBC/Hz @1MHz	–	1.81GHz
[46]	180nm	-106.1dBc/Hz @0.6MHz	65.5mW	900MHz
[47]	180nm	-89.79dBc/Hz @0.6MHz	16mW	850MHz
[48]	130nm	-91.5dBc/Hz @1MHz	0.44mW	–
[49]	90nm	-90 dBC/Hz @0.6MHz	16.8mW	1.74GHz

Table 6.3: Fabricated ring oscillator performance comparison

Ref	Tuning Range	FOM_1	FOM_2	Status
This Work	0.513-2.64GHz	158.29dB	175.33dB	Tested
[43]	0.381-1.15GHz	156.0dB	170.9dB	Simulated
[44]	0.92-0.925GHz	138.9dB	110.0dB	Tested
[45]	1.1-1.86GHz	–	166.9dB	Tested
[46]	0.73-1.43GHz	151.5dB	169.3dB	Tested
[47]	0.394-1.14GHz	140.8dB	158.4dB	Simulated
[48]	0.4-0.433GHz	147.1dB	121.9dB	Tested
[49]	1.57-3.57GHz	147.0dB	161.4dB	Simulated

The measured phase noise performance for the oscillator at 1.2V supply voltage and 1.889GHz frequency of operation is shown in 6.11a and 6.11a. The measurement tool calculates the carrier power and computes the phase noise with respect to a carrier frequency at an offset using an internal frequency tracking. Phase noise across the frequency range is shown in Figure 6.12. Phase noise is better than -93dBc/Hz @1MHz across the operating range of 513MHz to 2.64GHz. It deteriorates below 0.65V control voltage in

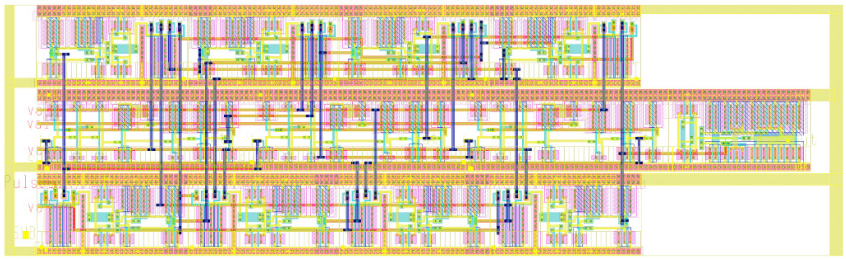


Figure 6.9: Layout of fabricated oscillator and control circuitry (60umX20um)

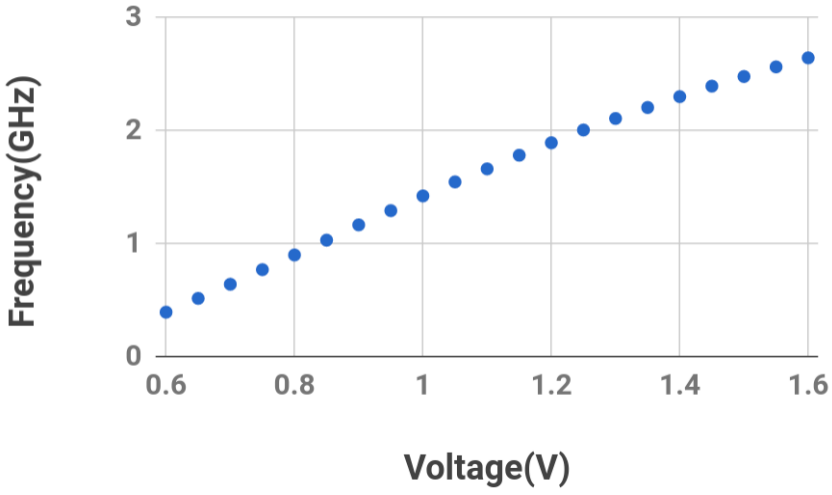
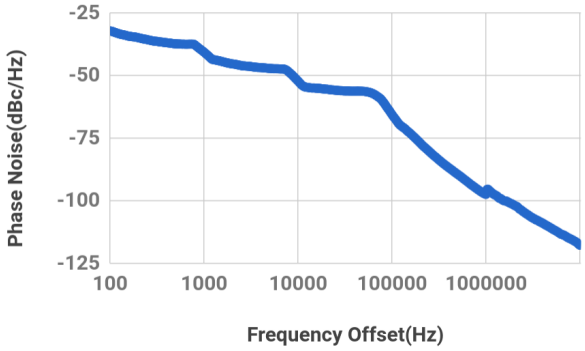
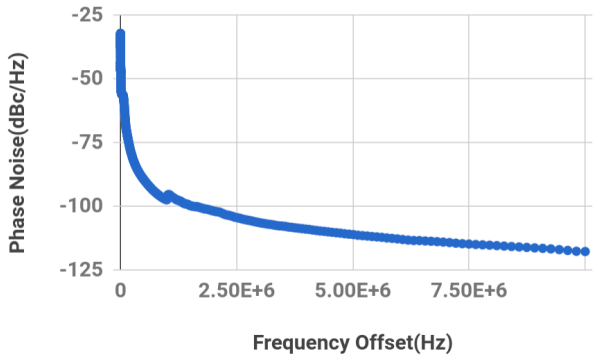


Figure 6.10: Control voltage-vs-operating frequency: linear behavior

the current design largely due to corruption of the input triggering condition.



(a) Log scale



(b) Normal scale

Figure 6.11: Measured phase noise@1MHz for freq.=1.889GHz at 1.2V supply

Two common figures of merit have been used for oscillator comparison with the other (free-running) ring oscillators. FOM_1 compares the phase noise and power consumption of the oscillators and is defined in Equation 7.1 (Δf refers to the phase noise measurement offset, f_o refers to the measurement frequency and P_o refers to the DC power consumption). FOM_2 (defined in Equation 6.5, where f_{max} and f_{min} refer to the maximum and minimum frequency in the tuning range respectively) accounts for tuning range along with phase noise. It can be seen in Table 7.2 that this work outperforms all the tested and simulated related VCOs in both figures of merit.

$$FOM_1 = 20log(\frac{f_o}{\Delta f}) - PN - 10log(\frac{P_o}{1mW}) \tag{6.4}$$

$$FOM_2 = 20log(\frac{f_o}{\Delta f}) - PN + 20log(\frac{f_{max} - f_{min}}{f_{min}}) \tag{6.5}$$

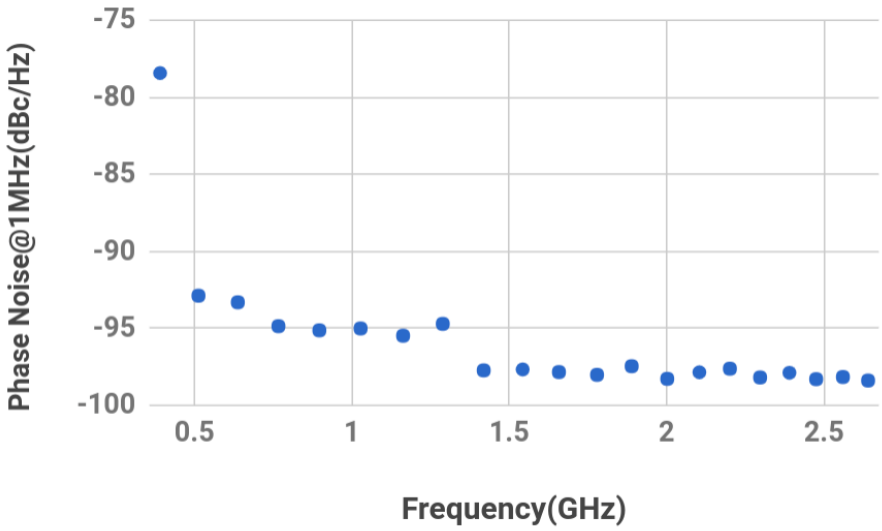


Figure 6.12: Phase noise@1MHz-vs-operating frequency

Chapter 7

Traveling Pulse Wave Oscillator

7.1 Introduction

High precision, low phase noise, multi phase voltage controlled oscillators are needed in many RF applications ranging from radio links to ADCs[50]. Particularly, low jitter and low skew timing distribution is required for mixer first receiver architectures and N-Path filters[51][52]. A key design feature needed in such circuits is the requirement of full swing and less than 25 percent duty cycle, non-overlapping clock drivers.

Transmission line stabilized clocking distribution offers a viable method to produce low skew, multi-phase VCOs. Transmission line systems such as salphasic distribution[53], distributed transmission line amplification[54], and adiabatic LC resonant clocks [55] provide sinusoidal or semi-sinusoidal clocks, making fast edges viable using additional buffering, adding to both extra, power, skew and jitter. Fast edge, low jitter and skew distribution is possible using rotary traveling wave architectures which have been well studied and analyzed[56][57]. Such architectures are limited by the signal swing and have difficulty providing non-overlapping clock phases. Full swing, non-overlapping distribution would require additional signal conditioning and buffering, which adds to power,

jitter and skew. Further, any such timing distribution at high frequencies required for low duty cycle and fast edges is subject to crosstalk and coupling issues. This limits the use of such on chip oscillators in high frequency designs of mixer first receivers and similar circuits.

Previous studies on pulsed wave oscillators using linear transmission line elements has demonstrated good phase noise properties[58]. The oscillators from the study are implemented using off-chip, low-loss elements. By contrast, a different implementation [59] demonstrates preliminary results for the first pulse-based on-chip traveling wave oscillator. The oscillator uses distributed amplifiers to counter the comparatively high loss in on chip elements. Specially designed pulse regenerating amplifiers were used to both create a unidirectional traveling wave and to maintain the low duty-cycle pulse shape.

An oscillator using non-linear, full-swing, limiting amplifier stages achieves optimal phase noise performance, when the slope of the edges is maximum. In conventional rotary traveling wave oscillators slope is increased with an increase in total amplifier drive thereby improving the phase noise[57]. A conclusion usually drawn from such studies is that more energy in the oscillator, better the phase noise. This is not necessarily true for all cases; if the traveling wave operates at maximal slope by design, then any further energy addition is a waste and does not lead to phase noise improvement. In this work, two designs are investigated, with a special focus on slope preservation to validate this argument.

The pulsed driver style investigated later in this paper offers multiple design parameters which cater to the different design needs. Stable multi-pulse (overtone) behavior is possible which enables a unique architectural feature: the same phase available at multiple points on the oscillator. Pulse width, and hence duty cycle, is a design parameter which can be adjusted according to application independent of many other oscillator

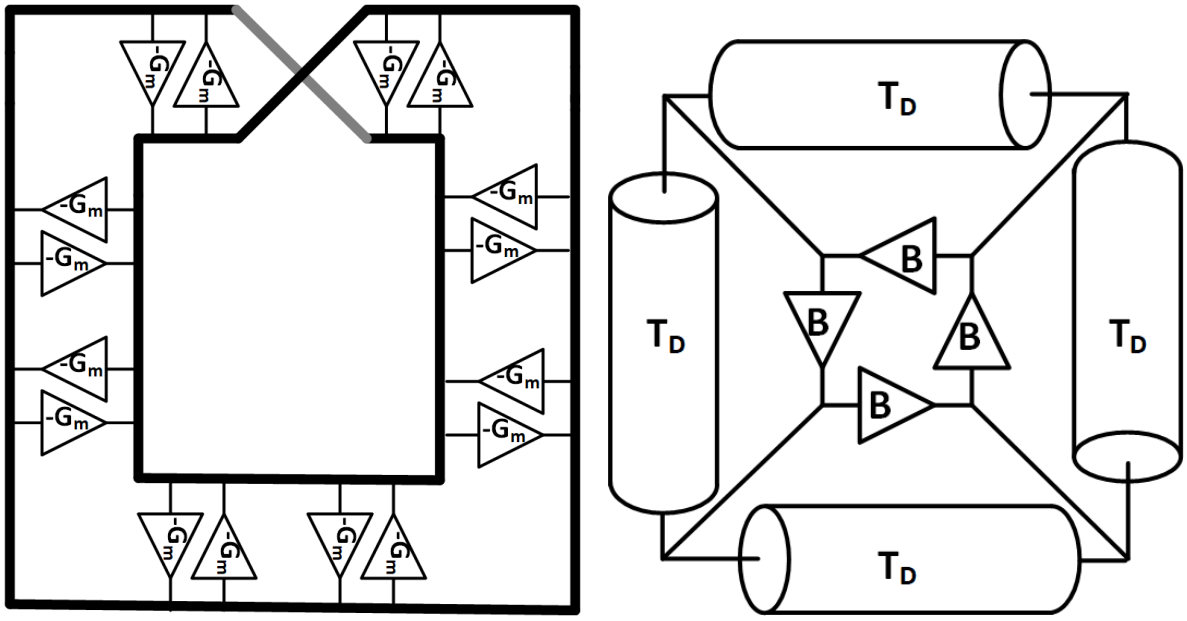
parameters. These properties make these oscillators an ideal candidate to be used in applications requiring timing distribution, or non-overlapping clocks. Further, they offer a viable alternative for these technologies to scale in frequency with smaller design nodes.

In this chapter, architecture parameters and constraints are explained. A viable method to setup and start the oscillator is explained. Two implemented designs in GFUS 130nm are compared to show a $2dB$ figure of merit(FOM) while maintaining the same high slope traveling wave. Lowest power CMOS implementation of rotary traveling wave oscillator was achieved using specialized startup and amplification techniques which start and maintain high wave slope. At last, some projections based on simulations are made for technology scaled versions of this oscillator topology and its applications.

7.2 Oscillator Architecture

Conventional traveling wave oscillators have differential amplifiers along a transmission line loop. The amplifiers are always connected to diagonally opposite ends of a transmission line. It is not possible to get a non overlapping clock output taps from the propagating wave in the loop. Also, no two locations along the loop have the same phase. A large number of amplifiers are required to get a high slope traveling wave (to minimize noise) [57] which translates to high power consumption in the oscillator.

In-order to create a pulse traveling wave, pulse regenerating amplifiers were designed (discussed in section 7.3). Consider a section of a transmission line as shown in Figure 7.2. A pulse input at the input V_1 of a pulse regenerative amplifier(B) and transmission line goes through the transmission line and comes out V_{1T} after some loss and a time delay T_D. The amplifier generates an output pulse V_{1B} after a time delay of T_B with a smaller amplitude just enough to compensate for the loss in the corresponding transmission line segment. The relative time delay of T_D and T_B produce an output waveform at V_2 that



(a) Conventional traveling wave (b) Pulse traveling wave

Figure 7.1: Traveling wave oscillators

is the superposition of the two waves at V_{1B} and V_{1T}. The slope of the rising edge of the output waveform is dependent on the relative phase lag of the amplifier and transmission line segments.

A pulse traveling wave oscillator consists of one or more copies of the above pulse regenerator in a loop meeting the phasing constraints for regeneration as shown in 7.1b. Any wave traveling in the reverse direction does not get amplified due to the large non-amplifying reset phase of the amplifier discussed in section 7.3. This pulse oscillator architecture allows a large number of other design alternatives to meet specific challenges. Interleaving the pulse amplifiers is possible as shown in 7.3c. Better distributed amplification is possible with interleaving the amplifiers as the constraint between amplifier delay and transmission line delay can be relaxed while smaller segments of transmission line can be buffered. The transmission line length can be multiplied and the same frequency oscillator can be constructed having multiple pulses chase each other. This results in a oscillator clock distribution in which identical clock phases can be distributed using

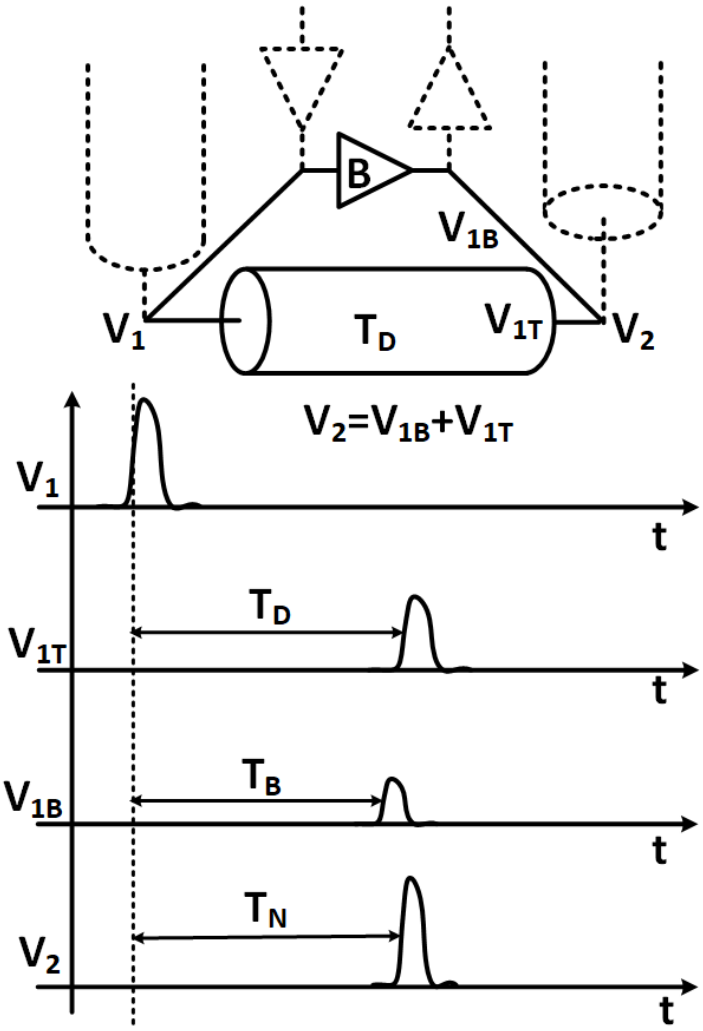


Figure 7.2: Traveling pulse Wave along a distributed transmission line

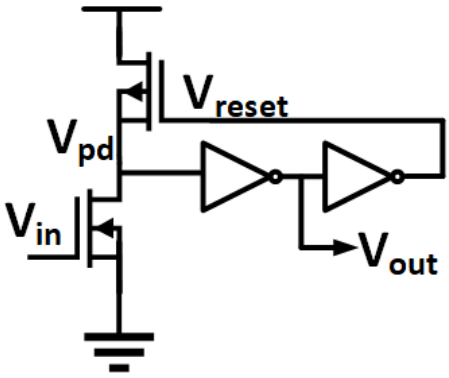
transmission line stabilized timing without the extra timing jitter and skew of timing distribution networks. Multi-pulse stability and even timing distribution due to interaction between them was discussed in [11] and is utilized in traveling wave topology here.

7.3 Pulse Amplifier

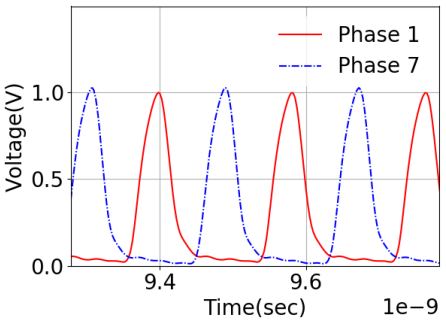
The non-linear pulse amplifiers are shown in 7.3a. The amplifier is a self-reseting pulse generator based on a pulse-gate CMOS design[28]. V_{pd} is pulled down on the rising edge of the signal at V_{in}. This pulls up V_{out} and pulls down V_{reset}, causing the PMOS to pull up V_{pd}, which causes V_{out} to pull down. The generated pulse at V_{out} is relatively insensitive to the input pulse shape or amplitude if the input pull-down transistor has large transconductance. This triggers the gate and the pulse shape is set by the internal reset loop as long as the input pulse does not persist longer than the reset time. After the pulse output, but before the reset has concluded, the input is insensitive to further pulses and the output is low impedance to ground, suppressing the reverse wave in the TM-line. After a suitable delay, V_{reset} returns to its steady state awaiting the next incoming pulse.

7.3.1 Startup Constraints

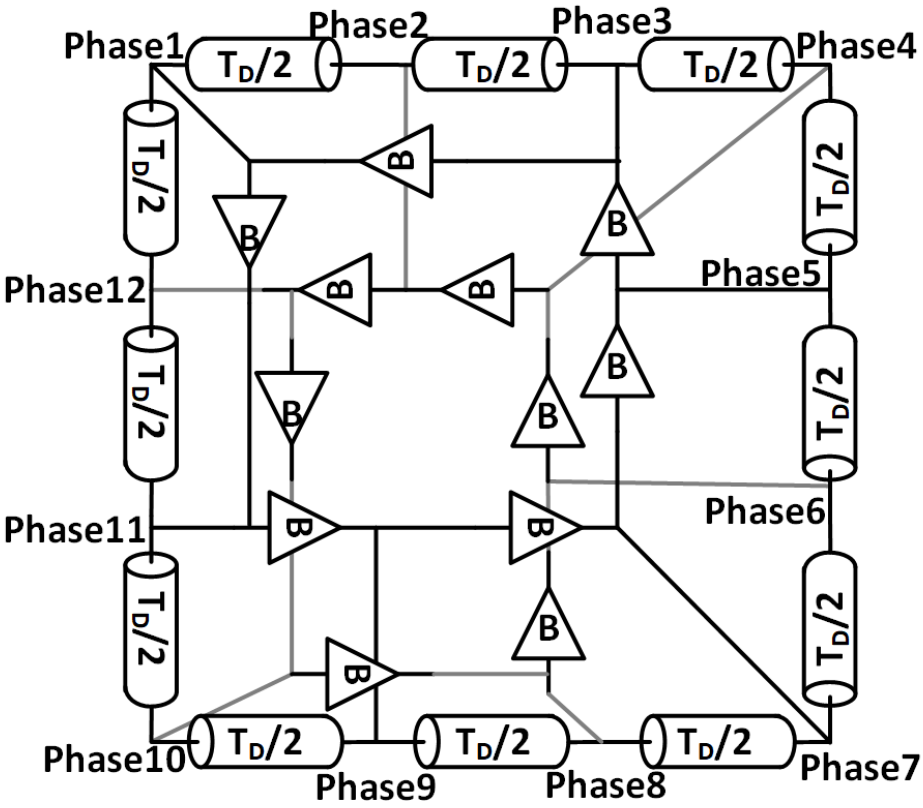
At startup, all the inputs and outputs of the pulse amplifiers are low-impedance and there is no energy stored in the transmission line. In-order to build up sustained oscillations in the traveling pulse mode, initial pulses of low amplitude (such as those created by a single regenerative stage acting alone) must trigger further regeneration until the amplitude is sufficient for stable operation. Unfortunately, the pulse amplifier shown in 7.3a rejects such small pulses as noise. The output impedance of the amplifier is set much higher than the transmission line, in fact just sufficient to compensate the transmission line loss. Two techniques are used to guarantee startup: 1. TM-line bias is



(a) Pulse gate amplifier



(b) Simulated non-overlapping clock outputs(phases 1 and 7 of a 12 phase output taps)



(c) Buffer interleaved traveling pulse oscillator

Figure 7.3: Pulse traveling wave oscillator

adjusted to provide small signal gain. 2. A "starter" oscillator based on a simple ring oscillator of pulse gates fires trigger pulses into suitable high-impedance inputs of the

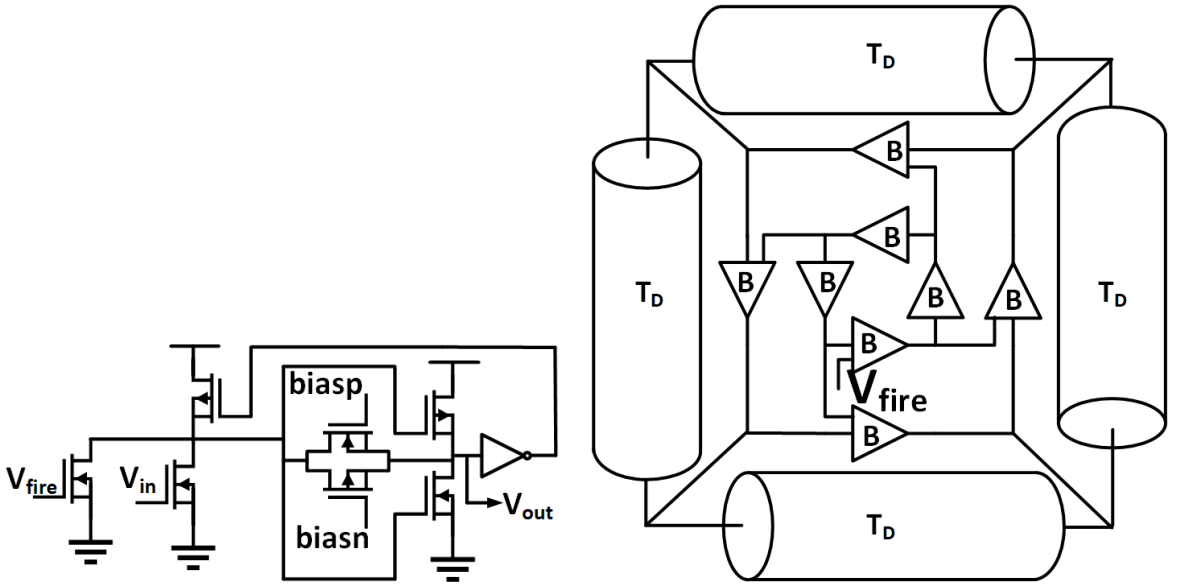
pulse regenerators.

Resistive Feedback Mode

The pulse amplifier in 7.3a is modified with the addition of a transmission gate from input to output as shown in 7.4a. This creates two modes of operation for the amplifier. During startup, the transmission gate connects the input and output of the inverter in the output stage. This forces the inverter into self-biased amplification mode and charges the TM-line to that potential. In that mode, small disturbances are amplified so that start-up pulses rapidly grow to an amplitude that no longer needs the self-biasing mode. Once the oscillations are correctly setup, the amplifier is set back to the pulse amplifier mode which rejects small noise impulses by turning the transmission gate off. This lowers the power usage as well as rejects several types of noise coupling.

Secondary Startup Oscillator

A secondary "starter" oscillator is setup with oscillation frequency equal to or slightly faster than the traveling wave oscillator. This secondary oscillator is constructed of only pulse amplifiers without a transmission line. It is started up by a single pulse injection into any of its (high-impedance) gates. The outputs of the secondary oscillator are put into the V_{fire} inputs of the traveling wave oscillator with correctly matching phases as shown in 7.4b. Once the traveling wave oscillator boots up, the secondary oscillator is stopped.



(a) Resistive feedback pulse amplifier

(b) Startup oscillator inside the pulse traveling wave oscillator

Figure 7.4: Startup circuit

7.4 Design Constraints

7.4.1 Period

In-order to get the highest slope of the rising edge amplifier delay and transmission delay are ideally matched. Under this design constraint, period of the oscillator is largely dependent on the total transmission line length. Bigger the length, larger the oscillation period.

The next two design parameters are determined based on transient noise simulations on a fully parasitic extracted design. The oscillator analyzed is a 12 tap cross-interleaved version as shown in 7.3c. Since the designed oscillator is highly non-linear in response to noise characteristics and superposition is not a valid argument for different noise sources, usual techniques like Impulse Sensitivity Function[15] cannot be directly applied. Two metrics are used and consensus of the two based on the current design constraints is used

to finalize the design. Phase stability for one cycle of the oscillator and phase stability integrated upto 40 cycles (determined by maximum possible run time possible under design constraints) are compared. High wave slope is maintained by the amplifier. The effects of buffered segment lengths and power, while maintaining high slope are analyzed next.

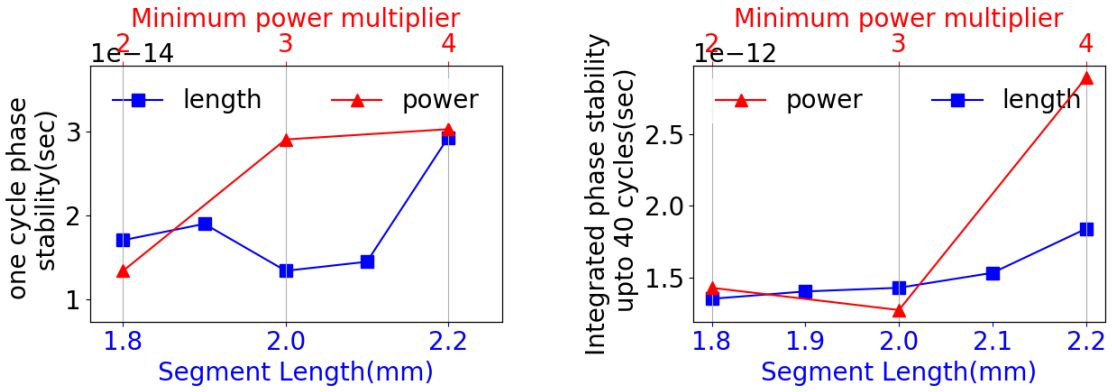
7.4.2 Buffered Segment Lengths

To determine the maximum segment length across which an amplifier is to be connected, minimum sized buffers were constructed which reliably maintain the oscillations. Then single segment length was varied. Analysis was done per cycle basis to not let the effect of frequency affect it. It can be seen in 7.5a that minimum single cycle phase stability is seen for a length of 2mm per segment. Integrated phase stability 7.5b can be seen to grow exponentially with segment length. As a compromise between the two parameters, 2mm was chosen as the segment length to connect the amplifier across. In actual design, the amplifiers delays are larger than 2mm transmission line segment delay. So, interleaving (as shown in 7.3c) between amplifiers needs to be done to buffer correct transmission line segment lengths.

7.4.3 Power

In the simulated design, 2 minimum sized buffers were needed to reliably maintain oscillations. This simulation is done for 24mm length transmission line divided into 12 segments to buffer every 2mm segment determined in the last section. As can be seen from 7.5a, single cycle phase stability is highest at minimum operational power. Integrated phase stability 7.5b is nearly constant for multiplier of 2 and 3 but goes considerably worse for multiplier of 4. This can be accounted due to the fact that high

wave slope is maintained as a design constraint and not achieved due to power added by buffers. Hence too much power added by buffers trades off with transmission line stored energy. Due to the minimum power design constraint, multiplier of 2 was chosen in the final design.



(a) Single cycle

(b) Integrated upto 40 cycles

Figure 7.5: (Smaller value of phase stability is better)Phase stability

In practice, different stability constraints can be optimized for against the low power feature of the oscillator. For this design the above two features were chosen due to simulation constraints.

7.5 Results

Two designs were fabricated in GFUS 130nm technology. First was a $2.9GHz$ oscillator with a $44mm$ transmission line length, $0.66mm^2$ area and 16 phase output. Second was $5.4GHz$ oscillator with a $24mm$ transmission line length (abstract model shown in 7.3c), $0.41mm^2$ area and 12 phase output. Figure 7.6 shows the die micrograph of the second oscillator. The designs were measured using Keysight PXA signal analyzer $N9030B$ $3Hz - 26.5GHz$.

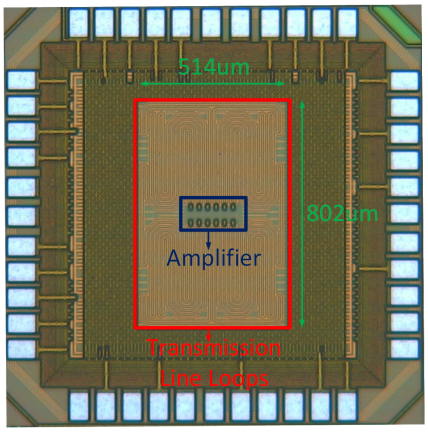


Figure 7.6: Die photo of the $5.4GHz$ oscillator

$$FOM = 20log(\frac{f_o}{\Delta f}) - PN - 10log(\frac{P_o}{1mW}) \tag{7.1}$$

Figure 7.8 shows the phase noise of the two oscillators at 10MHz offset across the operational frequency range. Table 7.2 shows the measurement comparison with other traveling wave oscillators. Linear voltage controlled frequency response was achieved in the two designs as shown in 7.7a . Further, fine voltage control operation was implemented in the higher frequency version with linear control as shown in 7.7b. FOM defined as Equation 7.1 (where f_o is the measurement frequency, Δf is the offset frequency, PN is the phase noise and P_o is the power) was used to compare the two designed oscillators. The higher frequency oscillator had an improvement of about 2dB in average FOM across the tuning range due to the specialized startup circuit designed to achieve lower power in it. Table 7.3 shows the projected scaling (based of simulations) of the proposed architecture to smaller scale technologies. The limitations in frequency and pulse width are set by the rise time of buffers in the technology.

Table 7.1: Comparison with Rotary Wave Oscillators

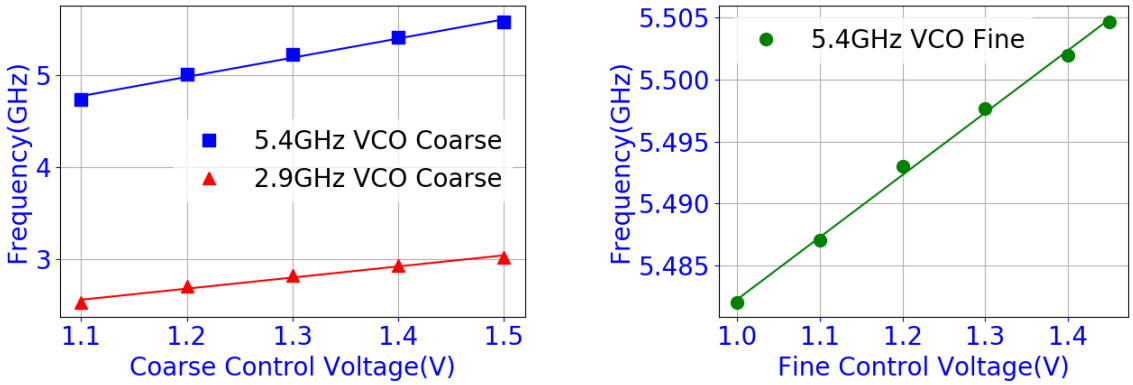
Ref	Technology	Phase Noise	Measurement Frequency
This Work	CMOS 130nm	-131.75dBc/Hz@10MHz	2.93 GHz
This Work	CMOS 130nm	-126.2dBc/Hz@10MHz	5.41 GHz
[60]	CMOS 130nm	-105dBc/Hz@1MHz	12 GHz
[57]	CMOS 110nm	-140.8dBc/Hz@3MHz	3.05 GHz
[61]	CMOS 90nm	-96.65dBc/Hz@1MHz	11 GHz
[62]	SiGe BiCMOS 120nm	-112dBc/Hz@10MHz	45 GHz

Table 7.2: Comparison with Rotary Wave Oscillators

Ref	Power	Tuning Range
This Work	34.75mW-68.7mW	2.53-3.02 GHz
This Work	18.59mW-34.58mW	4.73-5.57 GHz
[60] 30mW	11-12.2 GHz	
[57]	52.8mW	3.05-3.65 GHz
[61]	70mW	10.41-11.37 GHz
[62]	14mW	43.5-46.5GHz

Table 7.3: Simulated Technology Projections

Technology	Pulse Width	Max Frequency
GF130nm	45pSec	6GHz
GF45nm	15pSec	28GHz
GF22FDXSOI	14pSec	30GHz



(a) Coarse voltage control (b) Fine voltage control

Figure 7.7: Linear voltage controlled frequency change

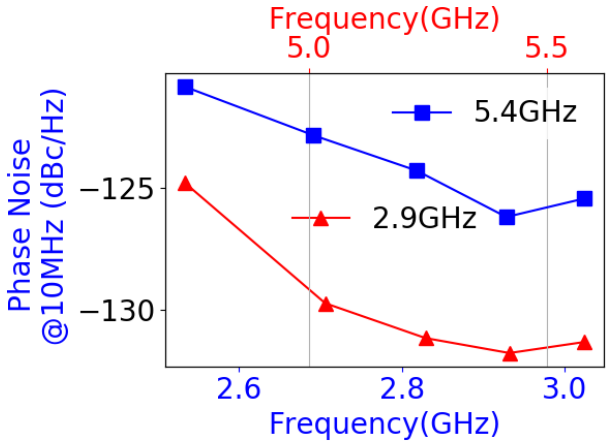


Figure 7.8: Phase noise measurement across VCO operational frequency

Chapter 8

Pulse Oscillators with Dynamics

Different pulse ring oscillator architectures and designs were explained in last two chapters. Effects of dynamics were not taken into account in the analysis and measurements presented in those chapters. This chapters aims to exclusively observe the effects of dynamics on the timing stability. Results from fabricated oscillator measurements in GF 130nm, HSPICE simulations and behavioral tool are compared to show that gate dynamics results in timing stability improvement. All the results are analyzed in per cycle, so as to not reflect the affect of frequency. Frequency scaling would results in timing stability change as predicted by the conventional models [17]. Further, figure of merit across the possible design space were visualized using the behavioral tool.

Fabricated oscillators were shown to have timing stability improvement for about 10 times longer than their simulated counter parts. Better characteristics in fabricated oscillators is accounted to different nature of noise in actual devices. Due to multi timescale nature of noise, different timescales can have different timing stability improvement. The overall effect being a stability improvement for longer duration. This points to a limitation of our noise simulation methodologies and the type of noise models currently available.

8.1 Fabricated Oscillators

Four different oscillators were fabricated and tested for timing stability improvement due to collective pulse dynamics. The fabricated oscillators and their measurements are described next.

8.1.1 Different Oscillators

Four different oscillators fabricated and tested were:

- Figure 8.1 : Oscillator 1 : It has 1 pulse running around in 8 gates. It operates at a smaller slope of delay modulation function η than the rest of the tested oscillators. Noise at smaller number of cycles due to η being small will be considerably reduced. Adding to that it should have higher noise at smaller number of cycles due to higher number of stages per pulse. The overall timing stability behavior is the combination of these two effects.

- Figure 8.2 : Oscillator 2 : It has 2 pulses running around in 8 gates. It operates at a higher slope of delay modulation function η than Oscillator 1. Noise at smaller number of cycles due to η being larger than oscillator 1 will be considerably higher. Adding to that it should have smaller noise at smaller number of cycles due to less number of stages per pulse. The overall timing stability behavior is the combination of these two effects.

- Figure 8.3 : Oscillator 3 : It has the same structure as Oscillator 2 but has additional paths. Since in a no noise case, output from every 4 gates would be identical in Oscillator 2, so the output has been forwarded to interleave the oscillator. It is same as spatially coupling a oscillator.

- Figure 8.4 : Oscillator 4 : It is a traveling pulse oscillator. It has increased timing stability due to transmission line stabilization of a pulse gate.

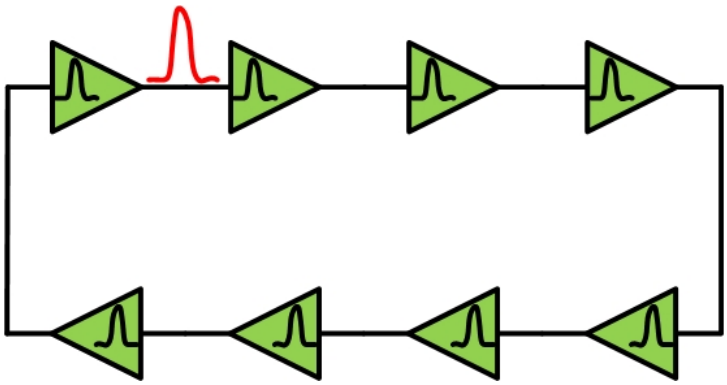


Figure 8.1: Oscillator 1 :Pulse Ring Oscillator with 1 Pulse in 8 pulse gates

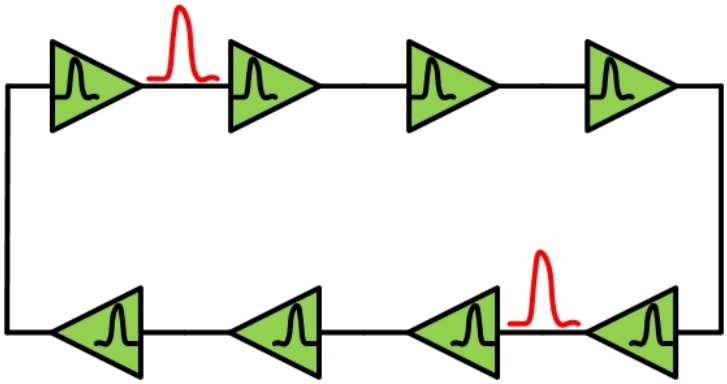


Figure 8.2: Oscillator 2 :Pulse Ring Oscillator with 2 Pulse in 8 pulse gates

8.1.2 Measurements

Following observations were made from the measurements:

- In Figure 8.5 initial timing stability of Oscillator 1 is better than Oscillator 2. But after a few cycles, Oscillator 2 is more stable than Oscillator 1. This is due to higher η in oscillator 1 which leads to poor stability in smaller cycles but higher stability in larger number of cycles.

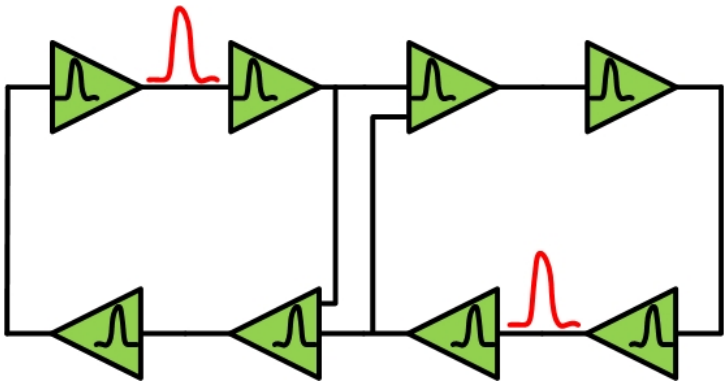


Figure 8.3: Oscillator 3 :Pulse Ring Oscillator with 1 Pulse in 4 pulse gates interleaved

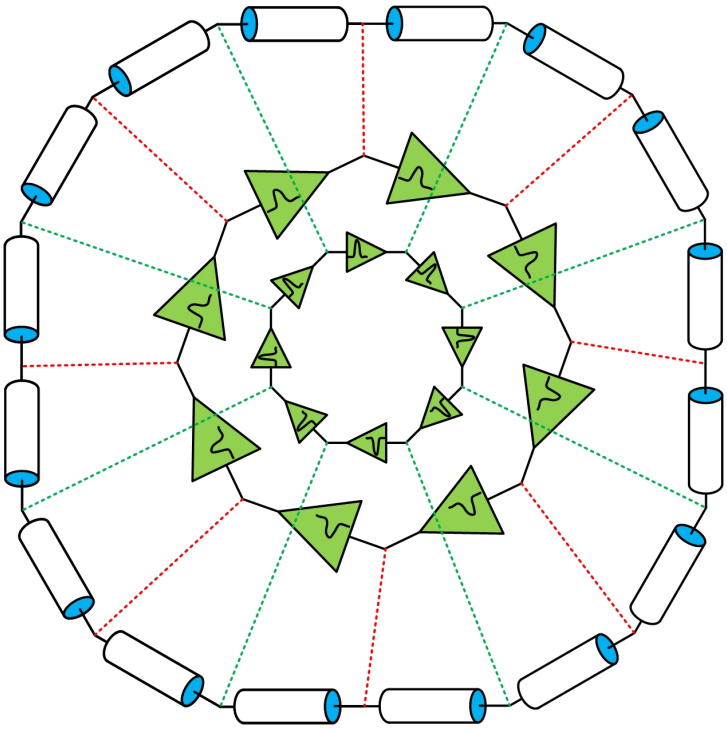


Figure 8.4: Oscillator 4 :Interleaved Pulse Traveling Wave Oscillator with 1 Pulse in 6 Gates

- In Figure 8.5 and Figure 8.6 timing stability of Oscillator 3 can be seen to be better than Oscillator 1, since interleaving in 2 pulse case results in better noise averaging and improves the timing stability.

- Figure 8.5 and Figure 8.6 show that timing stability improvement of Oscillator 4 is better than Oscillator 1,2 and 3. This is due to increased stability and longer memory of wave oscillator resulting from the transmission line Q. The increased stability also lasts larger number of cycles.

- In Figure 8.7 and Figure 8.8, both Oscillator 1 and Oscillator 4 can be seen to improve in timing stability with increase in supply. This is due to better current noise averaging resulting in timing stability improvement which shifts in parallel.

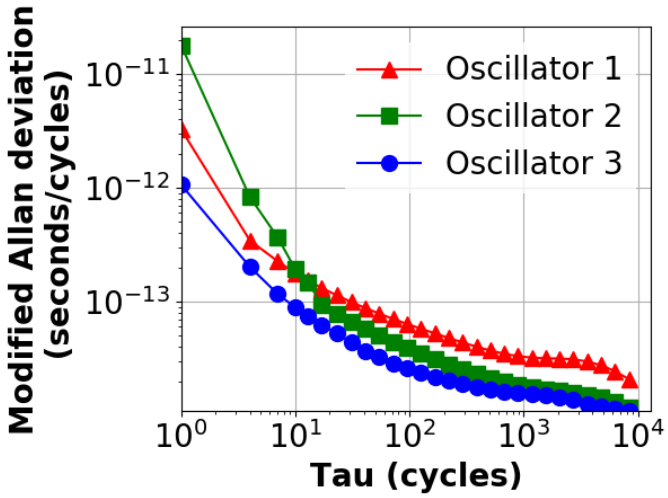


Figure 8.5: Timing stability of different oscillators at Supply=0.7V

8.1.3 Complementary Nature of Work

It has been claimed that the design methodology discussed in this work is orthogonal to all the conventional design methodologies. The claim was verified by following

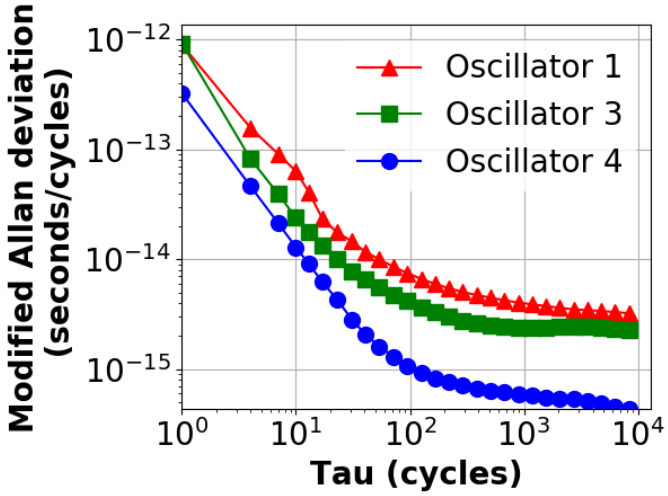


Figure 8.6: Timing stability of different oscillators at Supply=1.5V

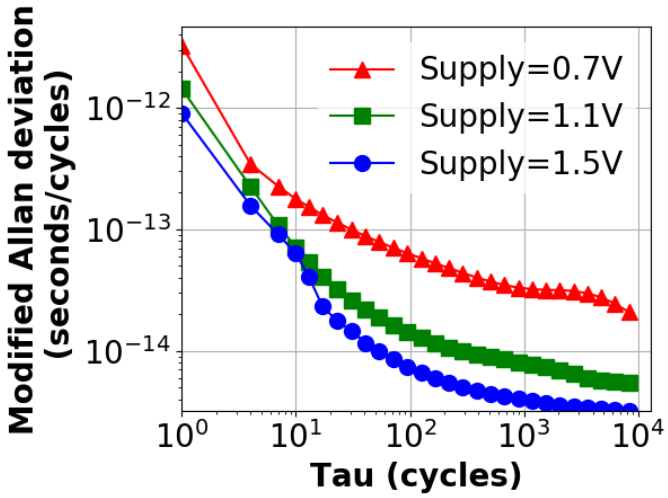


Figure 8.7: Timing Stability variation with Supply for Oscillator 1

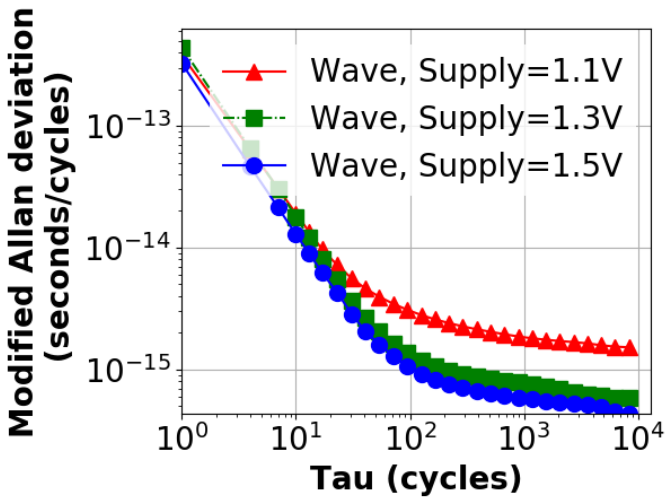


Figure 8.8: Timing Stability variation with Supply for Oscillator 4

observations:

- Parallel shift in timing stability measurements was seen with change in supply voltage. Increase in supply results in increase of current which in turn results in better timing stability resulting from better averaging.
- Interleaving the 2 pulse oscillator also results in better averaging and thereby shifting the timing stability plots in parallel.
- Pulse traveling wave oscillator again results in further improvement of noise averaging due to transmission line Q.

8.2 Simulation

Increase in stability over multiple cycles can be observed in HSPICE simulations similar to that observed in the bench measurements. HSPICE simulations were done for White FM noise source in GF 130nm process.

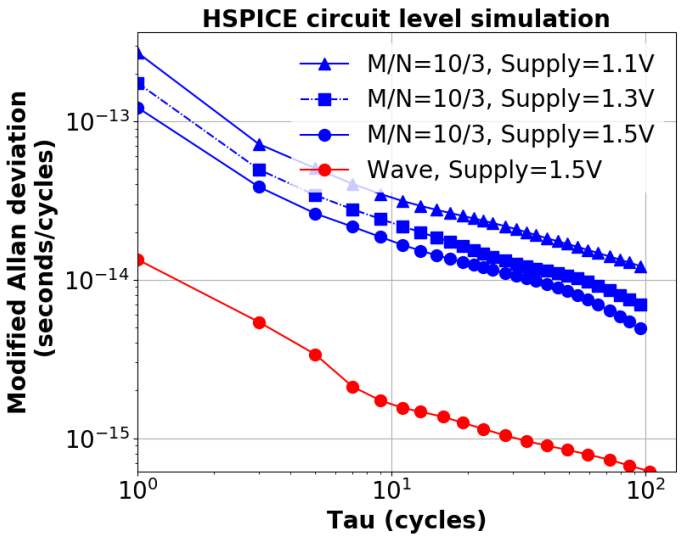


Figure 8.9: HSPICE simulated timing stability of Pulse ring and Wave Oscillator

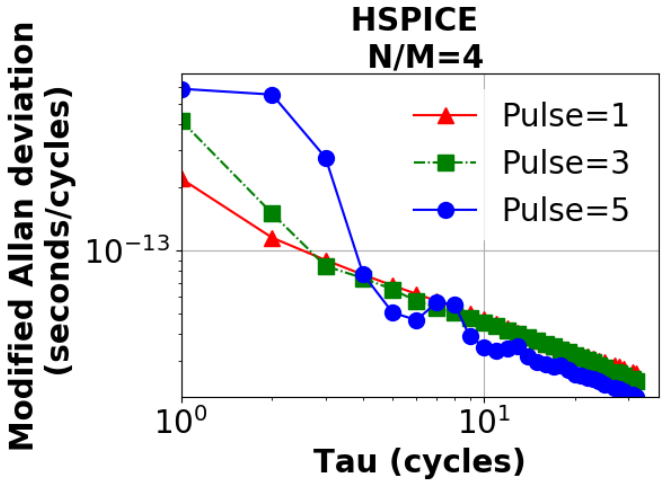


Figure 8.10: Variation of Timing Stability with number of pulses

Following similarities can be drawn between bench measurements and HSPICE simulations:

- Wave oscillator is more stable than pulse ring oscillator as shown in Figure 8.9.
- Increase in supply increases the timing stability and shift the plots in parallel as shown in Figure 8.9.
- Timing stability improves in larger timescales for more number of pulses (keep the stages per pulse and η fixed) shown in Figure 8.10.
- Higher η case of 3 pulses in 10 stages is more stable than a 3 pulses in 12 stages oscillator as shown in Figure 8.9 and Figure 8.10.

8.3 Behavioral Tool

Figure 8.11 shows the effect of increase in number of pulses for fixed 4 stages per pulse and $\eta = 0.2$. The result predicted from the behavioral tool is similar to that from the HSPICE simulations. Next timing stability improvement is evaluated by sweeping the design space using the behavioral tool.

8.3.1 Figure of Merit

Figure of merit defined earlier is evaluated to give an idea to the designer for optimal region of design. First phase stability improvement is evaluated by direct multiplication of average β_{self} (self locking slope) and τ_{self}. It is observed that the stability for single cycles changes with change in design parameters. Next, figure of merit is evaluated by dividing the phase stability improvement by single cycle jitter.

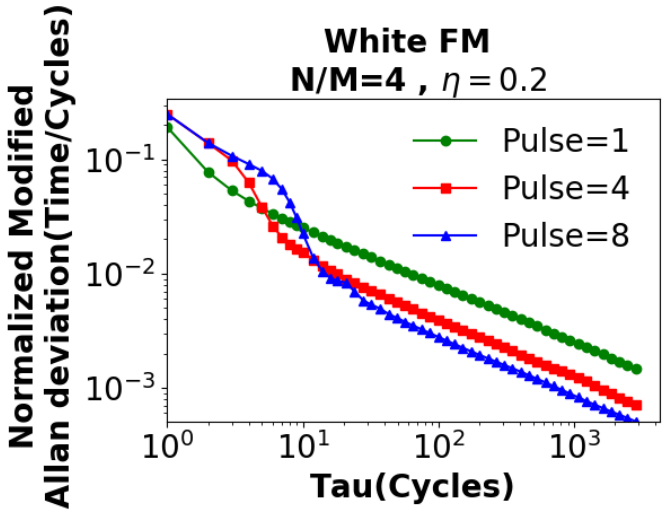


Figure 8.11: Modified Allan Deviation as a measure of timing stability for different number of pulses

For the case of Flicker FM noise, Figure 8.12 shows the average phase stability improvement. It can be seen that the phase stability improves with increase in number of pulses and η. Figure of merit, shown in Figure 8.13, also shows similar improvement with both number of pulses and η.

8.3.2 Multi-Timescale Noise

Noise in CMOS circuits constitutes of different processes operating in different timescales. Conventional simulation techniques have either White FM noise which has equal noise magnitude across the whole frequency spectrum. Any other noise source like flicker FM is constructed by filtering the White FM using an appropriate filter. This creates a noise spectrum which has correct characteristics in the frequency domain but lack the notion of individual processes which constitute the noise in different timescales. A small study was done to analyze the reason behind timing stability improvement in bench measurement for larger number of cycles. It is posited that if noise processes have different timescales, then it is possible to improve timing stability separately in all those timescales. This

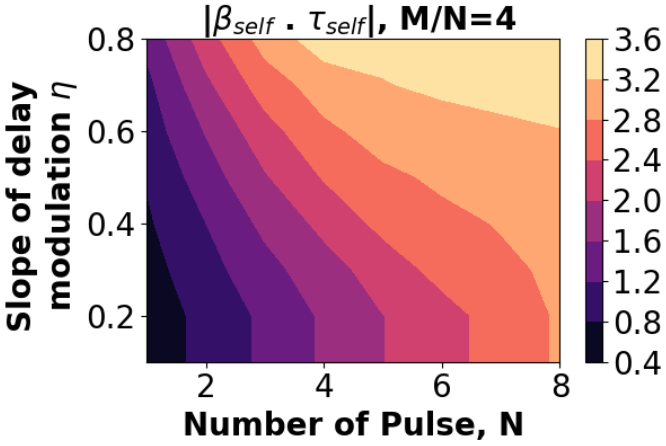


Figure 8.12: Variation of phase stability improvement with number of pulses (M) and slope of delay modulation function η

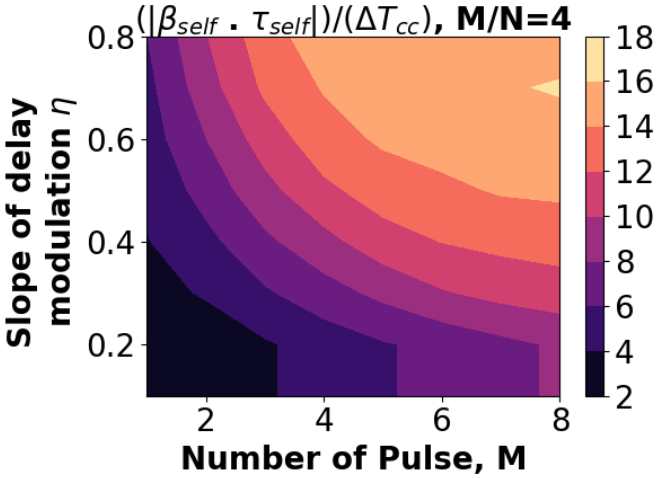


Figure 8.13: Variation of ratio of phase stability improvement and cycle to cycle jitter with number of pulses (M) and slope of delay modulation function η

would result in better timing stability in bench measurements. It would also mean that current simulations techniques for noise in simulators like HSPICE are not sufficient to account for oscillators with dynamics.

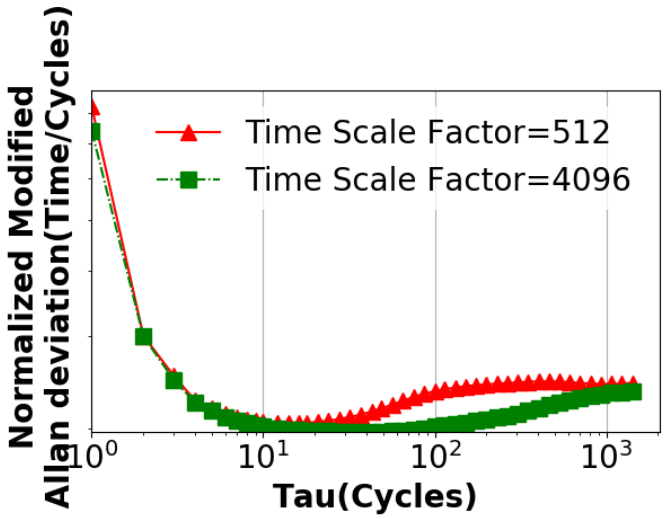


Figure 8.14: Effect of multi-timescale noise on timing stability of oscillators

Timing stability was evaluated for two flicker noise sources having different magnitudes and different timescales of operation. Longer timescale had smaller noise magnitude (typical noise behavior in CMOS). Figure 8.14 shows the effect of change in time scales for the smaller magnitude (factor of 10 smaller) noise. Following observations are important:

- High initial improvement in timing stability as observed in this work can still be seen for both timescales.
- An extra dip in timing stability improvement can observed. This extra dip is not observed when the Flicker FM noise source has a single timescale (all other plots from behavioral and HSPICE in this work).
- The duration for the extra improvement in timing stability is in the order of the

time scale factor for the two simulations.

The example shows that for dynamical oscillators, multi-timescale noise models need to be developed for accurate simulations of timing characteristics. This also provides a reason for stability improvement lasting longer in bench measurements.

8.4 Conclusion

The effects of collective dynamics of pulse gates on the timing stability were validated by comparison between bench measurements, HSPICE simulations and behavioral simulations. Predictions from behavioral simulator (having just local gate dynamics) is sufficient to get timing stability improvement similar to that from HSPICE simulations. Bench measurements have stability improvement for longer durations than that predicted by simulations(both HSPICE and behavioral). Inadequate modeling to noise models in time domain has been shown to be a possible cause for such a mismatch.

Chapter 9

Conclusion and Future Research and Applications

9.1 Research Discussion

The thesis presented a new design space of voltage controlled oscillators. Following are the highlights of the thesis and the conclusion drawn from them:

- Pulse Gates were shown to be a reliable method to generate dynamical interaction between consecutive events happening in a gate. The dynamics generated are due to charge interaction and not amplitude changes. Different dynamics using different pulse gate topology changes were discussed.

- Pulse gates offer a good alternative to conventional amplifiers due to their single sided ISF and high common mode supply rejection. ISF based analysis was done to predict the timing stability characteristics of oscillators. The numbers were shown to have a good correspondence with measured values on bench. Mutiple pulse oscillators were fabricated in multiple technologies.

- Local dynamics when put into a loop result in global timing stability improvement. Behavioral simulator was constructed to show that just the delay-vs-separation local dynamics of gates is sufficient to result in global timing stability improvement. This stability improvement resembles that of a phase locked oscillator with a high gain.

- Timing stability improvement is dependent upon number of pulses, strength of interaction in pulses and number of gates per pulse.

- The proposed methodology opens up a new design space in ring oscillator design which has the capability of pushing the ring oscillator boundaries to near LC oscillator limits. Since LC oscillators in fine scale CMOS have their own issues, this methodology has the ability to revolutionize the ring oscillator design

- Multiphase timing distribution is possible due to the existence of more than a single pulse in the loop

- Transmission line stabilized pulse traveling wave oscillators provide opportunity to have iso-phase timing distribution with high timing stability. They show similar PLL like frequency stability improvement. Designs were fabricated in multiple technologies in multiple frequency ranges.

- Current noise simulation methodologies do not account for multi timescale nature of noise and hence do not do justice to dynamical oscillators in simulations. This results in bench measurements being superior to simulations.

9.2 Possibilities of Research

Due to the novel nature of research, there exist a multitude of new questions which need to be analyzed. Some such topics are discussed next as possible directions of future

research.

9.2.1 Self Locking Cycles Improvement

The proposed oscillator design methodology improves the timing stability of oscillator for some initial cycles. Currently the pulse ring oscillator has improved stability for less than ≈ 100 cycles and pulse wave oscillator has improved stability for few 100s of cycles. This number directly corresponds to how well the oscillator can create its own time reference. For external locking it is dependent on the purity of external time reference.

Conventional averaging methodologies can be used to improve this timing reference. The timing information in the designed oscillators are conveyed using negative feedback loop in the pulse gates. The reason current methodology works is because the timing uncertainty build up in the negative feedback is lower than the overall system. This lets the negative feedback corrects for the timing uncertainty in the bigger loop on account of its better timing. N sample averaging can be used to maintain high timing coherence in the negative feedback loop.

9.2.2 Phase Locking using Delay Modulation

Slope of the delay modulation function (delay-vs-separation dynamics) determines the period of the loop. If same number of pulses, stages per pulse and pulse width is maintained, then the oscillator period can be modified by modification of slope delay modulation function. This gives a small tuning range in the oscillator. The benefit of using this at a control mechanism to change the oscillator period is that it provides an inherent first order filter. Hence, it provides with the opportunity of easily phase locked oscillators using an external reference.

9.2.3 Phase and Frequency Stability Modeling Consensus

This work analyzed the oscillators by measurement of frequency stability and projected the phase stability from it. Doing this, inherently assumes that phase stability in oscillators is a continuous function, hence its derivative is well defined. Analyzing the derivative, therefore lets us analyze the phase itself.

It is to be noted that the oscillators described in this work have a negative feedback with loop delay in the order of loop frequency. Such systems are borderline acausal and phase stability may not be a continuous function of time in such systems.

In such a case the described frequency stability analysis only does half the analysis needed to fully describe the systems. The problem is phase stability is not a well defined function under different noise sources. An in-depth analysis is needed for phase stability in the systems at hand. Then a model which uses both phase stability and its derivative frequency stability can used for complete system description.

9.2.4 Multi Timescale Noise Analysis and Mitigation

It was noted in the measurements that number of cycles over which higher frequency stability improvement was seen, was considerably higher in fabricated oscillators as compared to HSPICE simulations or behavioral model. This can be described by the fact that noise in real systems is due to multi-timescale noise sources. In different timescale it has different frequency behavior, but inherently the behavior is created due to sources in different timescales and having different magnitude interacting with each other. The noise models usually do not take this multi timescale noise behavior into account. The proposed oscillator designs are sensitive to noise in different timescales differently. Although there is interaction between phase errors in different timescales, but the effect of different timescales can still persist semi-independently. This is because all the information in the

described oscillators in contained in time.

9.2.5 Multi Timescale feedback

The oscillators currently designed and analyzed have feedback local to the gates. This local feedback when interacted in a global loop is resulting in timing stability improvement. It is possible to create topologies where in addition to the local feedback, there is feedback in multiple timescales. This feedback should still be interacted globally. The problem arises due to the fact that it is hard to create feedback after a longer duration. This is because the uncertainty build up matches the oscillator uncertainty and no effective improvement can be achieved.

9.2.6 Injection locked multi oscillator system

Current design methodology deteriorates the initial cycle to cycle jitter at the cost of eventual timing stability improvement after some cycles. Design techniques to construct an oscillator with low cycle to cycle to jitter are well known. To get the most out of the design methodology, a highly stabilized conventional low cycle to cycle jitter oscillator should be injection locked to a pulse oscillator with multiple pulses interaction with high η. The output of such an oscillator will be stable in both short and long timescales. Due to the gated oscillator like front end of the pulse ring oscillators, it is also easy to injection lock these oscillators by themselves. If further locking from an external reference is done on the pulse oscillator. It will create a highly stabilized system in a very long timescale.

9.3 Possibilities of Applications

The oscillators designed in this work have self stabilization characteristic in long time scales. Such oscillators can be used in variety of circuits which either do not need a phase locked oscillator or can get away without one if the oscillator was stable enough.

9.3.1 Local Timing with Global Consensus

High frequency timing distribution on chip over long distances is costly (high buffering power to maintain traveling edge) and inefficient (due to jitter build up). The usual method to solve this problem is two fold, one divide the chip into different clock domains with each having its own phase locking synchronization. Second is to have a global synchronization phase locked loop which supplies timing information using heavily buffered timing distribution. The oscillators described in this work have the potential of creating a timing network which in self timed, and where minimal high frequency information travels long distance. The idea is to have an oscillator tree like distribution where each local oscillator maintain self stabilization long enough for operations local to the domain to get processed correctly. The oscillators higher in the tree stabilize the oscillators lower down the tree. The whole tree acts like a single timing network due to back pressure stabilization of the oscillators.

9.3.2 Analog to Digital Converter

The use of explored oscillators in ADCs is two fold:

- ADCs require an extensive timing distribution (like in Successive Approximation Register (SAR) ADC). This timing distribution is often the bottleneck in ADC design performance. Extensive tuning of such ADCs post fabrication is necessary

to make them perform upto the specifications. The timing distribution described earlier will directly benefit such an ADC timing distribution. The self stabilization of the whole distribution will reduce the need post fabrication tuning.

- Use of VCOs as front end integrators in sigma delta ADCs is a known technique. These ADC are often limited by the timing stability of the VCO. Since this VCO is a free running one, and the methods explored in this work improve the timing stability of a free running VCO, the oscillators offer a good alternative to the already existing ones to improve the ADC performance.

9.3.3 Time to Digital Converter

Time to digital converters are used in many applications like LIDARS, pixel detectors etc. One particular design architecture of TDCs involve comparing multiple timing loops. The oscillators proposed in this work offer direct advantage to such a design architecture due to following reasons:

- Oscillator startup is a defined event and can be used to reliably predict the timing.
- The oscillators have better timing stability and thus can offer better long term time measurements

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