Modeling of the SiO_2/SiC Interface Trapped Charge as a Function of the Surface Potential in 4H-SiC Vertical-DMOSFET

Gian Domenico Licciardo, *Member, IEEE*, Luigi Di Benedetto, *Member*, *IEEE* and Salvatore Bellone, *Member, IEEE*

***Abstract*— A new analytical description of the trapped charge distribution at the semiconductor-insulator interface of 4H-SiC Vertical-DMOSFET has been derived as a function of the surface potential into the channel. The model enables one to accurately calculate the *I-V* characteristics of the device in both sub- and above-threshold operation, namely when the channel works from weak accumulation to strong inversion. The accuracy of the model has been verified by comparisons with numerical simulations that evidence the effect of trap densities in the range [0-10^{14}] $cm^{-2}eV^{-1}$, and with experimental measurement of a 1.7kV commercial device.**

***Index Terms*— Silicon Carbide, power MOSFET, Analytical model, oxide defects.**

I. Introduction

Vertical DMOSFET, VDMOS from now on, is one of the most attractive device in 4H-SiC, since it combines the advantages of a voltage controlled device to good figure-of-merits for high and medium power applications [1,2], where silicon carbide exhibits very good physical and electrical properties [3,4]. However, the operation of the device is strongly influenced by the quality of the gate oxide, which remains a major concern despite of the recent improvements of the silicon carbide processing technology [5-7]. The relevant density of defect distribution into the oxide and at the semiconductor interface, indeed, significantly modifies the charge distribution into the channel and the accumulation region (see Fig. 1), so as to heavily modify both the above and sub-threshold *I-V* characteristics of the device [5-9].

Because of the lack of physical models to quantitatively predict the variations of the Forward Bias-Safe Operating Area (FB-SOA) of 4H-SiC VDMOS induced by the oxide defects, in [5] the authors presented a compact model of the oxide/semiconductor interface trapped charge, based on an approximated capacitor divider. However, the main approximation, related to the energy dependence of the interface traps and surface potential, limits its employment to the strong inversion operation and, hence, prevent it for analyses that include also the sub-threshold behavior.

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In this brief, a new analytical expression is proposed to describe the energy dependence of the interface-trapped charge distribution and its variations as a function of the surface potential and the gate voltage, from weak accumulation to strong inversion of the channel. This distribution, in conjunction with the variation induced on the flat-band voltage from the fixed charges into the oxide, allows one to accurately describe the forward behavior of 4H-SiC VDMOS in sub-threshold and above-threshold operations. Comparisons with numerical simulations and experimental measurements of a commercial device verifies the proposed model.

II. Analytical Model

A. Interface Trapped Charge

The inset of Fig. 1 shows the simplified 2D structure of the half-device used for model and simulations, together with the physical and geometrical symbols involved in the following equations. According to the results in [10, 11], the Density-of-States (DoS) induced by traps at the insulator-semiconductor interface, D_{it}, has been modeled as a function of the energy trap, E_t, by the superposition of four distributions, symmetrically placed with respect to the mid-gap, as shown in the inset of Fig. 2: $D_{it}\left(E_t\right)=D_{it,TA}\left(E_t\right)+D_{it,TD}\left(E_t\right)+D_{it,MA}+D_{it,MD}$. The term $D_{it,TA}\left(E_t\right)=D_{it,T0}e^{\frac{Et-E_C}{WTA}}$ ($D_{it,TD}\left(E_t\right)=D_{it,T0}e^{-\frac{Et-E_V}{WTD}}$) describes the band tails of acceptors (donors) distributed in the upper (lower) half-gap, while $D_{it,MA(D)}$ describes the deep level DoS distribution, assumed constant near the mid-gap [10]. However, since the Fermi level moves in the upper half of the band-gap when the device is forward biased, even in weak inversion, the ionized donor trap density results several orders of magnitude lower than that of the acceptor traps. Therefore its contribution can be neglected and the total DoS of traps reduces to $D_{it}\left(E_t\right)\approx D_{it,TA}\left(E_t\right)+D_{it,MA}$. The related trapped charge density, $Q_{a,it}$, can be calculated as a function of the surface potential in the channel, ψ_S, by means of the Fermi-Dirac distribution of probability as:

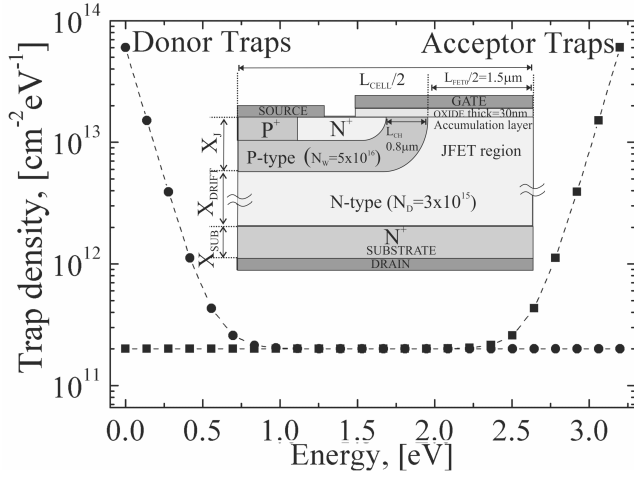

Fig. 1. Acceptor and donor traps distribution into the bandgap, imposed in the model and simulator. The inset shows the scheme of the half VDMOS employed.

$$Q_{a,it}\left(\psi_S,T\right)=-q\int_{E_i}^{E_C} D_{it}\left(E_t\right)\left(1+\frac{n_i}{n_S\left(\psi_S,T\right)}e^{\frac{Et-Ei}{k_BT}}\right)^{-1} dE_t \quad (1)$$

where $n_S\left(\psi_S\right)=n_i^2 N_W^{-1} e^{\frac{\psi_S}{Vt}}$ is the electron density at the oxide interface, E_i is the intrinsic Fermi level, assumed as the neutral energy value for the imposed symmetry of DoS and k_B is the Boltzmann constant. By substituting E_i with the lower limit of the conduction band, E_C, $Q_{a,it}$ can be calculated in terms of the Gauss hypergeometric function, $2F1$, as:

$$\begin{aligned}&Q_{a,it}\left(\psi_S,T\right)=\\&-qD_{it,T0}WTA\left[2F1\left(1,\frac{k_BT}{WTA};\frac{k_BT+WTA}{WTA};-\frac{N_CN_W}{n_i^2}e^{-\frac{\psi_S}{Vt}}\right)+\right.\\&\left.-\mathrm{e}^{\frac{E_V-E_C}{WTA}}2F1\left(1,\frac{k_BT}{WTA};\frac{k_BT+WTA}{WTA};-\frac{N_CN_W}{n_i^2}\mathrm{e}^{-\frac{0.5\times V_G+\psi_S}{Vt}}\right)\right]+\\&+D_{it,MA}\left[\frac{V_G}{2}-V_t\ln\left(1+\frac{N_CN_W}{n_i^2}e^{-\frac{\psi_S}{Vt}}\right)+V_t\ln\left(1+\frac{N_CN_W}{n_i^2}\mathrm{e}^{-\frac{0.5\times V_G+\psi_S}{Vt}}\right)\right]\end{aligned} \quad (2)$$

where N_W is the channel doping, coincident with that of the p-type well, N_C is the effective density of states, $V_G=3.2-3.3\times10^{-4}\left(T-300\right)$ is the temperature dependent band-gap, $V_t=k_BTq^{-1}$ the thermal voltage and $2F1\left(a,b;c;z\right)=\sum_{i=0}^{\infty}\frac{\left(a\right)_i\left(b\right)_i z^i}{\left(c\right)_i\, i!}$, being $\left(n\right)_i$ the Pochhammer symbol. Fig. 2 shows the accuracy of (2) by comparing analytical and simulated curves of $Q_{a,it}$ when the trap distribution of Fig. 1 is used, namely $D_{it,T0}=5\times10^{13}cm^{-2}eV^{-1}$, WTA=WTD=$0.09eV$ and $D_{it,MA(D)}=2\times10^{11}cm^{-2}eV^{-1}$ [10], when ψ_S varies from $2V$ to $3.05V$, corresponding to a V_{GS} variation from $0.5V$ to $13V$. It is worth noting that (2) keeps the same accuracy also for the calculation of the interface

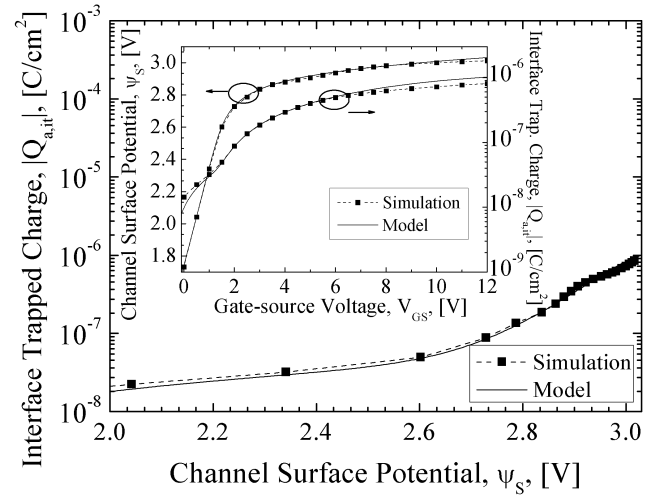

Fig. 2. Simulation-model comparison of $Q_{a,it}$ as a function of ψ_S. The inset shows simulation-model comparison of ψ_S and $Q_{a,it}$ as a function of V_{GS}.

trapped charge in the accumulation region, $Q_{a,it}^{ACC}$ as a function of the accumulation surface potential ψ_S^{ACC}.

B. Surface Potential

In order to introduce (2) into the *I-V* characteristics, $\psi_S\left(V_{GS}\right)$ must be explicitly calculated. By jointly solving the Poisson and the Gauss equation into the channel, in presence of a not null free carrier density, V_{GS} can be calculated as:

$$\begin{cases}V_{GS}=V_{FB}\left(T\right)-V_{traps}\left(\psi_S,T\right)+\psi_S+\dfrac{\sqrt{2\varepsilon qN_WV_t}}{C_{OX}}F\left(\dfrac{\psi_S}{V_t},\dfrac{n_i}{N_W}\right)\\ F\left(\dfrac{\psi_S}{V_t},\dfrac{n_i}{N_W}\right)=\left[\dfrac{\psi_S}{V_t}+\left(e^{-\frac{\psi_S}{Vt}}-1\right)+\left(\dfrac{n_i}{N_W}\right)^2\left(e^{\frac{\psi_S}{Vt}}-1\right)\right]^{1/2}\end{cases} \quad (3)$$

where $V_{FB}=\Phi_m-\chi-V_T\ln\left(N_Wn_i^{-1}\right)-0.5V_G-V_{it}$ is the flat-band voltage, Φ_m the gate-metal work-function, χ, the electron affinity, $C_{OX}=\varepsilon_{OX}t_{OX}^{-1}$ and $V_{traps}\left(\psi_S,T\right)=\left(Q_{a,it}\left(\psi_S,T\right)-qN_{fix}\right)C_{OX}^{-1}$, being N_{fix} the fixed charge density into the gate oxide. Since the approximated solutions to invert (3) [12,13] do not apply in our case for the presence of V_{trap}, in order to preserve the accuracy of (2), eq. (3) has been directly used to pre-calculate the $\left(V_{GS},\psi_S\right)$pairs. The inset of Fig. 2 proves the accuracy of this solution from V_{GS}=$0V$ up to the strong inversion, throughout the weak inversion condition of the channel, by comparing the analytical curves of $\psi_S\left(V_{GS}\right)$ and $Q_{a,it}\left(V_{GS}\right)$ of Fig. 2 with numerical simulations. It is worth noting that (3) can also be used to predict the onset of the strong inversion into the channel, by the expression of the threshold voltage, $V_{TH}=V_{GS}\left(\psi_{S0},T\right)$, where $\psi_{S0}=2V_t\log\left(n_i\,N_W^{-1}\right)$ is commonly accepted as the surface potential value at which the strong inversion occurs.

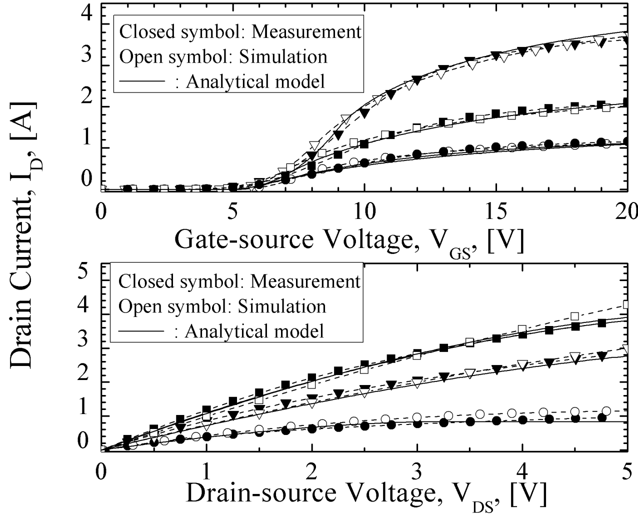

Fig. 3. Comparisons between analytical, experimental and simulated I_D-V_{GS} and I_D-V_{DS} curves of the device [14], at T=300K.

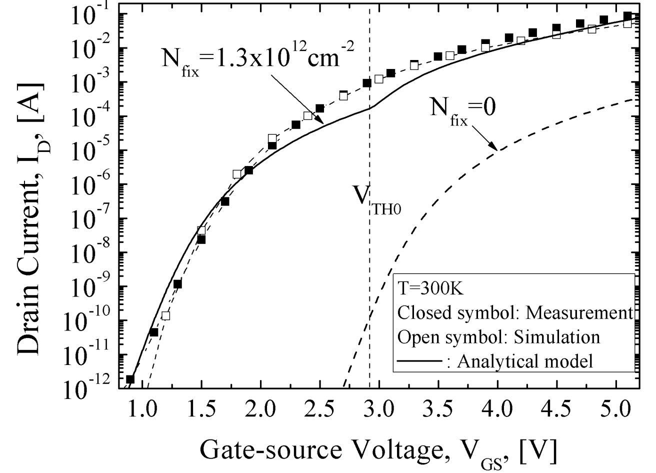

Fig. 4. Comparisons between analytical, experimental and simulated drain current of the device [19], from weak to the occurrence of the strong inversion, separated from the V_{TH0} vertical line. The dashed curve is the subthreshold current in absence of fixed charges into the oxide. Curves are taken at V_{DS}=5V and T=300K.

III. EXPERIMENTAL MEASUREMENTS

The equations derived in the previous section have been used in the current-voltage expressions of the VDMOS and compared with simulations and experimental measurements of the commercial device [14], performed by means of the Agilent 4155B semiconductor parameter analyser in conjunction with the Agilent 6651A power supply. Due to the minimum duration of the current pulse (1μs) allowed by the instruments, the experimental voltage ranges have been limited to [0V; 5V] for V_{DS} and [0V; 20V] for V_{GS}, in order to avoid self-heating degradation of the measurements. The geometrical and physical quantities of the device under test, reported in the previous sections and the inset of Fig. 1, have been extracted from measurements or estimated by simulation tuning. The subthreshold current, $I_{DS,SUB}$, has been calculated by using the surface potential in the channel as:

$$I_{DS,\mathrm{SUB}}(\mathrm{V_{GS}}) = \mu_{CH}\frac{W}{L_n}V_t^2\sqrt{\frac{q\varepsilon N_W}{2\psi_S}}\left(\frac{n_i}{N_W}\right)^2 \mathrm{e}^{\frac{\psi_S}{Vt}}\left(1-\mathrm{e}^{-\frac{V_{DS}}{Vt}}\right) \quad (5)$$

where μ_{CH} has been calculated as in [5], while (6) have been used for the above threshold curves, in order to make explicit the dependence from, V_{GS}, V_{DS}, and R_{TOT}:

$$I_{DS} = \begin{cases} R_{TOT}^{-1}\left(V_{DS}-V_{GS}+V_{TH}-\dfrac{1}{K_nR_{TOT}}\right)+ & \\ +\sqrt{\left|\left(\dfrac{1}{K_nR_{TOT}^2}+\dfrac{V_{GS}-V_{TH}}{R_{TOT}}\right)^2-2\dfrac{V_{DS}}{K_nR_{TOT}^3}\right|} & V_{DS}\le V_{GS}-V_{TH} \\ \dfrac{K_n\left(V_{GS}-V_{TH}\right)^2\left(1+\lambda V_{DS}\right)}{2+K_n\left(V_{GS}-V_{TH}\right)^2\lambda R_{TOT}} & V_{DS}>V_{GS}-V_{TH} \end{cases} \quad (6)$$

where $K_n = \mu_{CH}C_{OX}WL_n^{-1}$. Fig. 3 shows the accuracy of the model by comparisons with simulations and measurements of the output, I_{DS}-V_{DS}, and trans-characteristics, I_{DS}-V_{GS}, of the VDMOS [14], while Fig. 4 compares analytical, simulated and measured I_{DS}-V_{GS} characteristics of the tested device from weak to the beginning of the strong inversion. Curves refers to V_{DS}=5V but no significant variations of the trans-characteristics have been observed in all the examined V_{DS} range. The dashed, vertical line conventionally separates the two regions at V_{GS}=V_{TH0}=2.8V that is calculated by using $V_{traps}\left(\psi_{S0}\right)$ in (4). The strong dependency of V_{TH} from V_{GS} causes a significant increment of the slope of the I_D-V_{GS} curves and its shift, with significant effects on the thermal stability of the device [5].

The fixed charges into the oxide play an important role in subthreshold operation, because of the scarce density of interface trapped charge at the corresponding V_{GS} values. This is correctly predicted by the model in Fig. 4 where the dashed curve is obtained by imposing in all the quantities a null fixed charge density, namely N_{fix}=0. In turn, to obtain the agreement of the continuous curve with measurement and simulation N_{fix}=1.32x10^{12}cm^{-2} must be imposed, which is a value consistent with the related literature [15].

IV. CONCLUSION

In this paper an analytical description of the potential dependence of the interface trapped charge in 4H-SiC VDMOS is presented, with the purpose to give an accurate description of the static operations of the device from weak to strong inversion. Comparisons with numerical simulations and experimental measurements validate the model and stimulates further development on the blocking behaviour of the device.

REFERENCES

[1] B. J. Baliga, Advanced Power MOSFET Concepts. New York: Springer, 2010.

[2] J. A. Cooper, Jr. and A. Agarwal, "SiC Power-Switching Devices-The Second Electronics Revolution ?", *Proc. IEEE*, vol. 90, no. 6, pp. 956-968, June 2002.

[3] S. Bellone, L. Di Benedetto and G.D. Licciardo, "A Quasi-One-Dimensional Model of the Potential Barrier and Carrier Density in the Channel of Si and 4H-SiC BSITs", *IEEE Trans. on Electron Device*, vol. 59, no. 9, pp. 2546-2549, Sept. 2012.

[4] S. Bellone, F. Della Corte, L. Di Benedetto and G.D. Licciardo, "An Analytical Model of the Switching Behavior of 4H−SiC p+−n−n+ Diodes from Arbitrary Injection Conditions", *IEEE Trans. on Power Electron*., Vol. 27, no. 3, pp. 1641−1652, March 2012.

[5] G.D. Licciardo, S. Bellone and L. Di Benedetto, "Analytical Model of the Forward Operation of 4H-SiC Vertical DMOSFET in the Safe Operating Temperature Range", *IEEE Trans on Power Electron.*, vol. 30, no. 10, pp. 5800-5809, Oct. 2015.

[6] S. Bellone, L. Di Benedetto and G.D. Licciardo, "A model of the off-behaviour of 4H–SiC power JFETs", *Solid-state Electron*., vol. 109, no. 7, pp. 17-24, Jul. 2015.

[7] A. Consoli, F. Gennaro, A. Testa, G. Consentino, F. Frisina, R. Letor and A. Magri, "Thermal Instability of Low Voltage Power-MOSFETs", *IEEE Trans. Power Electron.*, vol.15, no.3, pp.575-581, May 2000;

[8] O.M. Alatise, N.-A. Parker-Allotey and P. Mawby, "Modeling the Electrothermal Stability of Power MOSFETs During Switching Transients", *IEEE Electron Device Letters*, vol.33, no.7, pp.1039-1041, July 2012.

[9] A. Castellazzi, T. Funaki, T. Kimoto and T. Hikihara, "Thermal instability effects in SiC Power MOSFETs", *Microelectronics Reliability,* vol. 52, no. 9–10, pp. 2414–2419, September-October 2012;

[10] S. Potbhare, N. Goldsman, A. Lelis, J.M. McGarrity, F. B. McLean and D. Habersat, "A Physical Model of High Temperature 4H-SiC MOSFETs", *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2029-2040, August 2008.

[11] D. Haasmann and S. Dimitrijev, "Energy position of the active near-interface traps in metal–oxide–semiconductor field-effect transistors on 4H–SiC", *Applied Physics Letters*, vol.103, no.11, pp.113506-113506-3, September 2013.

[12] A. Ortiz-Conde, F.J. García Sánchez, M. Guzmán, "Exact analytical solution of channel surface potential as an explicit function of gate voltage in undoped-body MOSFETs using the Lambert W function and a threshold voltage definition therefrom" *Solid-State Electronics*, vol. 47, no 11, pp. 2067-2074, Nov. 2003.

[13] R. van Langevelde, , F. M. Klaassen, "An Explicit Surface-Potential-Based MOSFET Model for Circuit Simulation", *Solid-State Electronics*, vol. 44, no 3, pp. 409-418, Mar. 2000.

[14] CREE model C2M1000170D [Online Available: http://www.cree.com/~/media/Files/Cree/Power/Data%20Sheets/C2M1000170D.PDF];

[15] S. Potbhare, N. Goldsman, and G. Pennington, "*A* quasi-two-dimensional depth-dependent mobility model suitable for device simulation for Coulombic scattering due to interface trapped charges" *Journal of Applied Physics*, vol. 100, no. 4, Apr. 2006.

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