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An 868 MHz 7.5 µW wake-up receiver with −60 dBm sensitivity

Sadok Bdiri[1], Faouzi Derbel[1], and Olfa Kanoun[2]

[1]Faculty of Electrical Engineering and Information Technology, Leipzig University of Applied Sciences, Wächter Str. 13, 04107 Leipzig, Germany
[2]Faculty of Electrical Engineering and Information Technology, Chemnitz University of Technology, Reichenhainer Str. 70, 09126 Chemnitz, Germany

Correspondence to: Sadok Bdiri (sadok.bdiri@htwk-leipzig.de)

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Abstract. In wireless sensor networks (WSNs), batteries are unlikely to be replaced or recharged once they get depleted, because of costs and feasibility. In a typical application, sensor nodes should be accessible and able to respond within a defined period of time, especially in real-time applications. However, the idle listening of the radio wastes most of the energy since the radio transceiver is constantly active. On the other hand, putting it into sleep state disconnects the node from the network. To cope with such a challenge, an ultra-low-power radio receiver referred to as a wake-up receiver (WuRx) handles the idle listening while keeping the main radio completely off. A WuRx consumes much less power than the main transceiver and triggers an interrupt only when a packet with a user-defined address is received. Embedding such a device enables better event-triggered applications where real-time behavior is required and a longer lifetime is mandatory. The proposed WuRx features practical sensitivity and includes the minimum number of active components in order to remain within the power budget. In this paper, an ultra-low-power WuRx with a power of 7.5 µW and a sensitivity of −60 dBm is developed. The decoding process of 16 bit of a wake-up packet (WuPt) takes less than 15 ms.

1 Introduction

The purpose of controlling one's surroundings in the physical world has become more relevant thanks to wireless sensor networks (WSNs). These networks include devices equipped with certain sensors in order to monitor the occurrence of ambient data and transmit them in an untethered manner. Depending on the field of application, commonly, sensor nodes should be able to be deployed with major independency of wired power sources and using batteries instead. Presently, without energy saving techniques, a small battery with a large capacity together with the amount of demanded energy from a single node presents a real challenge when the lifetime of years is a requirement. Besides, to applications like hazardous work environments, nodes are unreachable once deployed; thus, maintenance becomes an even harder task. Furthermore, as a WSN incorporates a large number of nodes, which can go from tens to hundreds, the cost of a single node from production to maintenance should be as minimal as possible. A sensor node mainly includes a processing unit, a radio chip, sensor(s), and a power source. The radio component spends most of the energy among the other parts. Researchers tend to reduce the power consumption by acting on the radio part. Commonly in WSNs, fewer data are transmitted in comparison to classical networks. Therefore, the radio can be principally turned off to save energy. On the other hand, this makes the sensor node unreachable and unable to respond to incoming packets from adjacent peers. Such an aspect causes a trade-off between the power consumption and the radio chip activity.

As a low-power constraint is severely challenging, the lifetime condition required for certain WSN applications must be fulfilled. One common solution targets communication protocols using a duty-cycled radio receiver scheme (illustrated in Fig. 1). Although the activity time of these radios is reduced, a price of higher latency is paid when the radio is in sleep state for a long period of time. Such a configuration

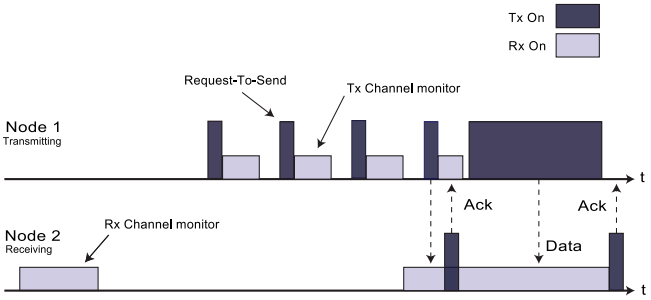

Figure 1. Communication scheme in a duty-cycled radio.

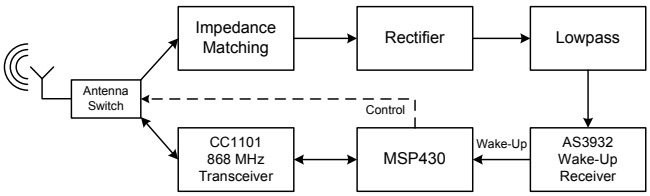

Figure 2. Proposed WuRx of Gamm et al. (2014).

applies to several scenarios. However, severe real-time preferences show that the overall system latency must be kept as short as possible, for which a very low duty-cycle radio scheme may be irrelevant. Conversely, an on-demand scheme is more likely to have very low communication latency with a reasonable energy consumption. Low-power radios known as wake-up receivers (WuRx) are intended to replace the main transceivers for idle listening tasks while consuming much less power. For extremely low latency communication, WuRx has to remain always on. If an ultra-low energy consumption can be realized, the sender network saves more energy and can last longer than a network using a duty-cycle scheme. The main feature of the WuRx is to induce an interrupt mostly to a processing unit upon reception of a special radio frequency (RF) or wake-up packet (WuPt). Afterwards, the host node powers on the main transceiver to initiate the conventional network communication.

A WuRx, with a unique identifier, should incorporate a digital baseband (DBB) to identify WuPt and avoid false positives. Commonly, WuRx designs adopt the ON/OFF keying (OOK) modulation technique due to its architectural simplicity. As WuRx consumes much less than conventional receivers, performance parameters such as sensitivity are degraded. State-of-the-art WuRxs work on improving the energy consumption and sensitivity by either enhancing the receiver architecture or choosing a more suitable technology. A passive radio receiver architecture was introduced by Gu and Stankovic (2004). The device uses the RF signal to raise a voltage level which will behave as an interrupt to the microcontroller (MCU). As an addressing technique, each WuRx receives a wake-up packet on a different frequency. Undoubtedly, such a hardware design increases complexity for both a wake-up transmitter (WuTx) and WuRx. The WuRx has an interesting power consumption, but with a poor sensitivity. Improving the latter requires active elements. Nonetheless, more recent WuRxs manage to carefully realize it to end up with a balanced trade-off of energy/performance.

In this paper, we realize a low-power sensor node equipped with an ultra-low-power WuRx with at least −56 dBm sensitivity. The WuRx performs in sub-GHz bands, specifically 868 MHz. A discussion of recent WuRx designs is presented in Sect. 2. In Sect. 3, the proposed WuRx's system design is introduced. Hardware implementation details followed by the measurement results and a comparison with other designs are given in Sect. 4. Finally, conclusions and a summary of the results will be given in Sect. 5.

2 Design space

2.1 Architecture considerations

Realizing that the possibility of lowering the power consumption to an extreme low level is an idea which has been suggested by many contributors through the years. It starts by wondering how to detect an RF signal and how sensitive and power-hungry an RF detector can be. We can find sophisticated techniques which achieve excellent detection sensitivity, but they dissipate more energy. As a commonly pursued strategy, the focus on designing wake-up radios using passive detection to guarantee the low-power budget is followed by attempts at enhancing sensitivity as well as other features.

Recent works (Pletcher et al., 2008; Marinkovic and Popovici, 2011) have focused on improving a single feature at the cost of another, a trade-off of power consumption and sensitivity. In the real world, most applications require a practical balance of this trade-off in order to respond to the desired performance. Publications like Gamm et al. (2014) and Hambeck et al. (2011) considered coping with that challenge. The efforts can be seen in the introduced WuRxs with −53 and −71 dBm sensitivity levels and consuming 8.4 and 2.4 µW, respectively.

The WuRx as seen in Fig. 2 from Gamm et al. (2014) mainly down-converts the RF signal from 868 MHz to 125 kHz using zero bias Schottky diodes, which are configured as an AC–DC rectifier.

The incoming signal is OOK modulated where from the transmitter side, a digital bit "1" is encoded by transmitting the RF carrier, while a "0" is simply the absence of the carrier. The rectified signal is a square-wave waveform with a frequency equal to OOK signal bandwidth. The latter is, then, fed to a low-frequency WuRx AS3932. The device can correlate an up to 32 bit OOK modulated address with a sensitivity of 100 μV_{RMS}, and it represents the main wanted feature (Austrian Mikro Systeme, 2009). In the end, when the address pattern, encoded in the incoming signal, matches the one configured in the AS3932's registers, the device generates an interrupt to the MCU. In Magno et al.

(2016), a −55 dBm WuRx is introduced. It utilizes a comparator to digitize the signal coming from the passive envelope detector to further feed it to a MCU. The offset voltage of the comparator sets the sensitivity of WuRx and dominates the entire WuRx energy consumption (1.2 µW) when MCU is in deep sleep. As soon as the MCU starts decoding, the energy consumption increases to nearly 65 µW, which makes it highly susceptible to interferences and unwanted packets. A super-regenerative-based WuRx featuring a high sensitivity of −97 dBm is introduced in Petäjäjärvi et al. (2016). The WuRx has a power of 40 µW at a operational frequency of 28 MHz. As high-speed elements tend to consume more energy, the consumption for this WuRx is only reasonable.

2.2 Technology considerations

WuRxs have been designed using either CMOS or off-the-shelf components. Concerning CMOS-based chips, publications have introduced prototypes with practically higher sensitivity (Pletcher et al., 2008; Hambeck et al., 2011; Huang et al., 2014) than that of other architectures. In spite of draining a considerably high current, the overall power consumption remains low since they can operate at a very low voltage. In Pletcher et al. (2008) and Huang et al. (2014), the energy consumption is over 50 µW, which is still considered high for most event-triggered WSN applications. Passive envelope detectors based on nonlinear passive components such as Schottky diodes are often used to remain within the power budget. Standard CMOS features nonlinear characteristics and can be expressed by the exponential function of a diode's current I_D in Eq. (1).

$$I_D = I_S \left(e^{\frac{V_D}{nV_T}} - 1 \right), \quad (1)$$

where V_D and I_S are the diode's forward voltage and saturation current, n is the ideality factor, and V_T is the thermal voltage (Hambeck et al., 2011). At a small signal, which represents the weak-inversion region of a MOS transistor, Schottky diodes and MOS transistors perform in a very similar manner when equally current biased. However, such detectors have poor sensitivity. Therefore, pre-amplification is required to improve the radio sensitivity. Power-hungry components can accomplish such a task. It is challenging to implement them in a WuRx design.

A time-to-market factor has to be acknowledged when choosing a technology to design a WuRx. Particularly, designing CMOS integrated circuits (ICs) such as application-specific integrated circuits (ASICs) is pricey in terms of designing time and prototyping costs in spite of the potential performance. However, the benefit occurs when mass production is planned. Moreover, field programmable gate arrays (FPGAs) have the benefit of reducing production and non-recurring engineering (NRE). Some works incorporated FPGA chips mainly to perform as a DBB for address correlation with an energy consumption of a minimum of 5 µW

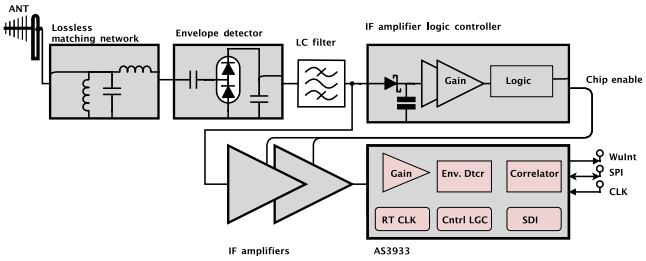

Figure 3. Wake-up receiver block diagram.

(Al-Uraiby et al., 2012; Pons et al., 2012; Jean-François et al., 2013; Rosello et al., 2011). The proposed WuRx uses off-the-shelf components with the purpose of accomplishing expeditious prototyping.

3 System design

Simplicity, sensitivity and energy consumption represent the main characteristics of an ultra-low-power WuRx. However, trade-offs exist between all the mentioned features; thus, finding an optimal point in between has been an interesting challenge. All along the designing process of the WuRx, power consumption remained the number one issue to be controlled in every single step. Low-power active components are incorporated for the purpose of enhancing the sensitivity of the WuRx. In this section, the design analysis of all blocks of WuRx are discussed. The different parts of a WuRx circuit are illustrated in Fig. 3.

3.1 Envelope detector

The overall performance of WuRx severely depends on the envelope detector characteristics. For such a reason, components are carefully chosen in order to achieve the desired objectives of the introduced design. The envelope detector detects the incoming signal by means of a passive receiver, notably using Schottky diodes HSMS-2852. The latter are zero biased and they provide fast switching. The diodes are optimized to be used with an input power of less than −20 dBm and below a frequency of 1.5 GHz (Avago Technologies, 2009).

The detector is configured as a Greinacher voltage doubler. Such a configuration provides higher output voltage. The advantage of using such a configuration over a single diode is the voltage doubling at the output and also the increase in the signal-to-noise ratio (SNR).

The slopes of the output voltage of both configurations are illustrated in Fig. 4. The voltage doubler also acts as a half-wave rectifier in order to perform an RF-to-DC conversion. Conversely, the envelope detector is able to interpret an incoming OOK modulated signal. As mentioned earlier, the output signal swings between two voltage levels with respect to the input signal. Accordingly, the resulting output is

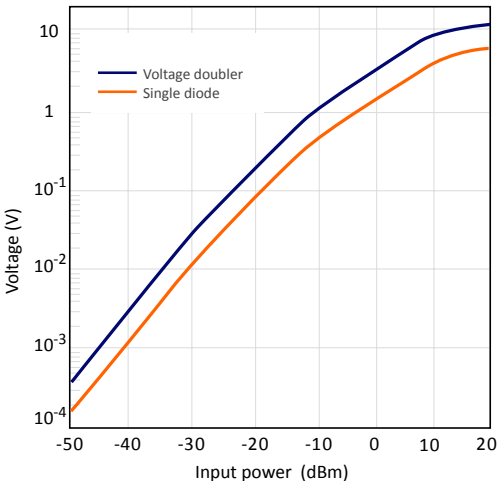

Figure 4. Envelope output variation at two different configurations.

a square signal with a frequency equal to the ON/OFF frequency of an OOK signal.

3.2 Ripple filter

As the rectifier tends to convert a sinusoidal signal into a DC signal, the output voltage will have AC components referred to as ripples. The circuit is configured as a half-wave rectifier. A distorted DC output has an impact on the overall performance of the complete circuit. Therefore, a ripple filter is added to fade out the undesired AC component.

With a shunt capacitor C_2 connected to the rectifier (Fig. 5a), the ripple voltage is decreased, thus having a smoothed output. However, at very low RF input power (< -50 dBm), the reduced ripple voltage still severely affects the output signal, which results in an alternating voltage instead of a constant DC output. Fig. 6 illustrates a simulation of rectified output voltage with an input power of -55 dBm at 868 MHz.

A decrease in R_L will induce less output voltage with larger ripples. Adding a series inductor L forms an L-type LC filter (Fig. 5b). The reactance of the inductor X_L opposes the AC components without reducing the DC output voltage. A capacitor filter is connected across the load resistance R_L. The property of a capacitor is that it blocks the DC component and lets the AC component through. When the rectifier is fed with an AC signal, the capacitor charges rapidly to the peak voltage of the initial pulse. Depending on the value of R_L, the capacitor will discharge until it is fed with the second pulse. Thus, the ripple is shorted to the ground but DC appears at the output. Considering the reactance X_L and X_C of L and C, respectively, where

$$X_C = \frac{1}{2\omega C} \quad X_L = 2\omega L \quad \omega = 2\pi f, \tag{2}$$

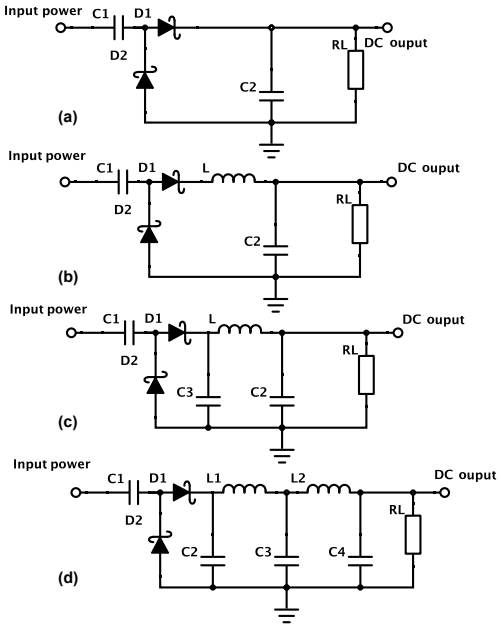

Figure 5. RF–DC rectifier with **(a)** capacitor filter, **(b)** L-type LC filter, **(c)** π-type LC filter and **(d)** π-type and L-type LC filters.

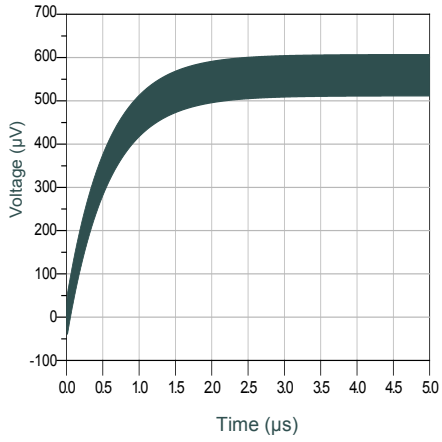

Figure 6. Output voltage of the rectifier with an L-type LC filter (Fig. 5b).

the ripple factor γ in terms of X_L and X_C is calculated according to the following expression.

$$\gamma_L = \frac{\sqrt{2}X_C}{3X_L} = \frac{\sqrt{2}}{12\omega^2 LC_2} \tag{3}$$

An increase in L and C narrows the ripple factor. Nevertheless, L has to be large enough (> 10 µH) to significantly reduce the ripple which will result in a big inductor size and manufacturing costs. Further improvement is made by adding another capacitor C_3 configured according to Fig. 5c. This setup is called a π-type LC filter and the new ripple

factor expression is as follows:

$$\gamma_\pi = \frac{\sqrt{2}}{8\omega^3 C_2 L C_3 R_L}. \quad (4)$$

From Eqs. (3) and (4), a comparison between the performance of a π filter and an LC filter yields the expression (Eq. 5)

$$\gamma_\pi = \frac{3}{2\omega C_3 R_L}\gamma_L. \quad (5)$$

Consequently, the DC output has less ripple, with the advantage of an acceptable inductor value range. This configuration depends additionally on R_L and C_3, which means the lower the R_L and C_3, the higher the γ. A transient simulation of the output voltage is shown in Fig. 7. Use of high-impedance R_L is acceptable since the circuit does not drive high loads. Besides, by cascading stages of L-type LC filters (Fig. 5d), γ is much more reduced but requires additional components. In the introduced design, one π-type LC filter meets the required needs.

3.3 Intermediate-frequency amplifiers

Address decoder AS3933 (Austrian Mikro Systeme, 2010) has a sensitivity of a minimum of 80 μV_{RMS}, which is similar to that of AS3932. Concerning HSMS-2852, tangential sensitivity TSS is −57 dBm for carrier frequency f_c = 915 MHz and video bandwidth B_v = 2 MHz (Avago Technologies, 2009). TSS stands for the lowest input signal power level higher than the minimum detectable signal, which corresponds to an 8 dB SNR at the output (Avago Technologies, 2010). Several noise sources contribute to degrading TSS, most notably, thermal noise, shot noise and flicker noise. Lowering B_v mainly reduces thermal noise, thus improving TSS (SkyWorks Inc., 2008). Other efforts can be made to improve the noise quality. According to Gamm et al. (2014), the decoder is able to decode a signal with a minimum input power of −52 dBm. It can be seen that AS3932 limits the overall WuRx sensitivity as it is directly connected to the detector. An amplification needs to be performed in order to shift a small-signal voltage level coming from the detector above the minimum detectable voltage level of the AS3933.

Small-signal amplification within the micro-power budget faces several challenges. As a matter of fact, available commercial low-power amplifiers generally feature a high input offset voltage V_{OS}, a low slew rate and a low gain–bandwidth product (GBP). To raise an 18 kHz signal voltage level from µV to a detectable voltage, such amplifiers are not suitable for accomplishing the task. Instead, higher-performance devices are required. To preserve energy, amplifiers should function only during the WuPt decoding and remain shut down during channel monitoring of WuRx. In this work, the ON/OFF switching is controlled by a different block named an intermediate-frequency logic controller (IFLC). Now, the

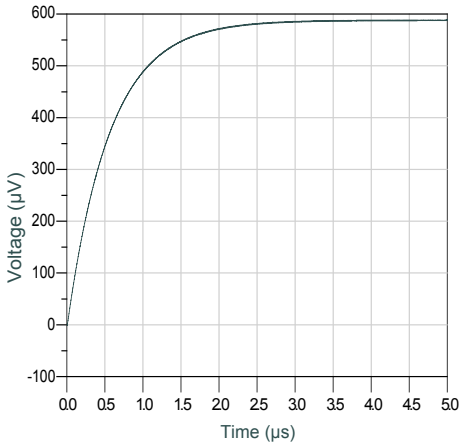

Figure 7. Output voltage of the rectifier with a π-type LC filter (Fig. 5c).

nature of on-demand applications of WSNs and WuRx shows that, generally, nodes are in sleep state and power on only when the necessary communication takes place. Despite the amplifiers' high power consumption, with such a communication scheme, the resulting low duty-cycled amplifiers offer a very low overall energy consumption, which meets the power efficiency requirements. The overall power consumption of IF amplifiers P_{Amp} is calculated in the following expression:

$$I_{Amp} = D I_{Amp\_Active} + (1 - D) I_{Amp\_Sleep}, \quad (6)$$

where P_{Amp_Active} is the power consumption of the amplifier when active for t_{Active} and P_{Amp_Sleep} when sleep/shutdown for t_{Sleep} and the applied duty cycle $D = \frac{t_{Active}}{t_{Active}+t_{Sleep}}$. Now, according to the bandwidth expressed in Eq. (7) of an operational amplifier, the higher the gain, the lower the bandwidth.

$$\text{Bandwidth} = \frac{\text{Gain–bandwidth product}}{\text{Closed loop gain}} \quad (7)$$

The proposed design requires high precision and efficiency amplifiers with an optimal frequency / performance ratio. Other than V_{OS}, GBP, I_{Amp_Sleep}, and I_{Amp_Active}, other parameters should be taken into consideration to achieve the desired precision. Characteristics like input offset current I_{OS} and input bias current I_B affects directly the V_{OS}, which represents the DC error added to the desired voltage output. With the increase in the stage gain, errors become more significant and disturb the following circuit block. These errors affect more the performance of opAmp when configured as non-inverting, inverting or follower. However, instrumentation amplifiers overcome offset problems and are compensated for a specific gain with high precision and increased common-mode rejection (CMRR) performance. The proposed WuRx adopts three stages of the MAX4461T in-

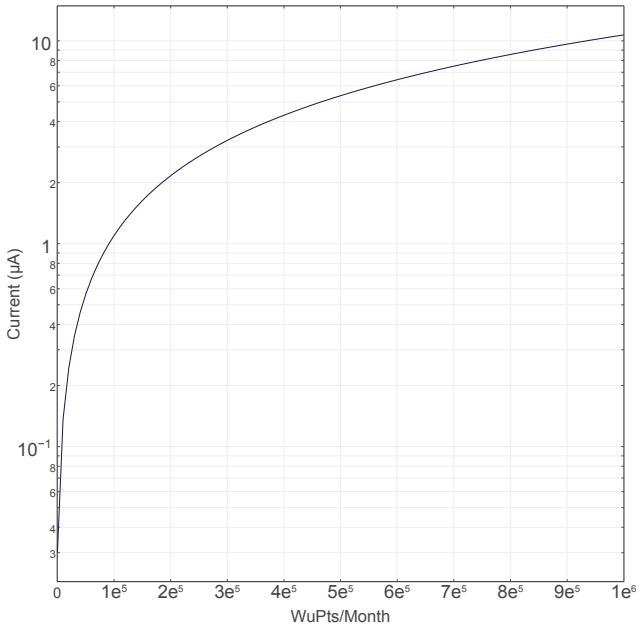

Figure 8. Overall IF amplifier power consumption deviation according to the number of received WuPts per month.

strumentation amplifier where GBP = 250 kHz at a closed-loop gain of 20 dB, CMRR = 120 dB, $I_{\text{Amp\_Active}} = 700\,\mu\text{A}$, $V_{\text{OS}} = 750\,\mu\text{V}$, and $I_{\text{Amp\_Sleep}} = 10\,\text{nA}$ (Maxim Integrated, 2006). The MAX4461 has to last in active mode for a minimum amount of time ($t_{\text{WuPt}} \leq t_{\text{Active}}$) to fully amplify the WuPt signal. Activating the amplifier is done through a $\overline{\text{SHDN}}$ pin.

The operation durations (t_{Active} and t_{Sleep}) of the IF amplifier are controlled by a different circuit block. The WuPt lasts $t_{\text{WuPt}} = 10.36\,\text{ms}$ and the $\overline{\text{SHDN}}$ is guaranteed to be driven for $t_{\text{Active}} = 15\,\text{ms}$ to meet the condition expressed earlier. To simulate the overall power consumption of the IF amplifier, the number of the received packets increases and the duty cycle D is set for a total period of 1 month. According to Eq. (6), the total energy consumption changes proportionally and the variation is plotted in Fig. 8.

Once a wake-up packet (WuPt) is received, the IF amplifiers switch to active mode by means of an incoming signal at the $\overline{\text{SHDN}}$ pin. The signal is a low-to-high pulse which has to last slightly more than wake-up packet duration to avoid additional power loss. A current drain of $I_{\text{Amp}} = 0.13\,\mu\text{A}$ for a number of received packets of 10^4 per month satisfies the required energy budget of the WuRx. However, $10e^4$ packets per month is considered very high traffic based on the nature of on-demand or real-time applications.

3.4 Intermediate-frequency logic controller

The IF amplifier activates only when $\overline{\text{SHDN}}$ is driven HIGH by an IFLC. The idea is to generate a low-to-high pulse us-

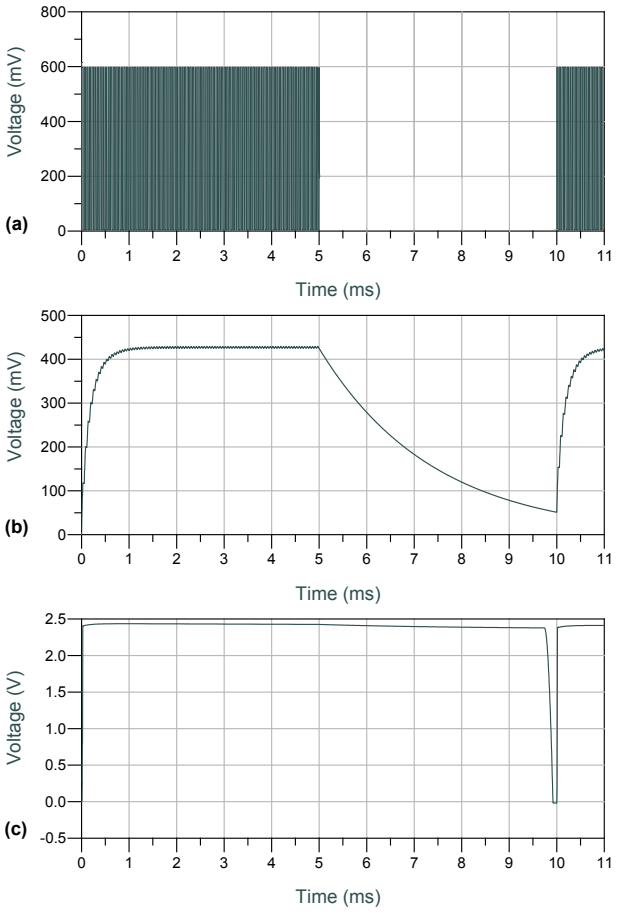

Figure 9. **(a)** 18 kHz WuPt simulation (carrier burst); **(b)** peak detector waveform. **(c)** Final generated pulse by an IFLC.

ing the received WuPt signal. The AS3933 decodes a specific WuPt structure illustrated in Fig. 10. Unlike the data in WuPt, the carrier burst length is set to be unchanged. Accordingly, the preamble and data pulses in WuPt are not taken into consideration to generate the wanted $\overline{\text{SHDN}}$ signal. The carrier burst lasts $t_{\text{C}} \simeq \frac{1}{2} t_{\text{WuPt}} \simeq 5\,\text{ms}$. The carrier burst has a square-wave nature with a frequency of 18 kHz, as can be seen in the simulation (Fig. 9a). Extracting a pulse from an AC signal is similar to signal frequency down-conversion. In the current design, the IFLC is configured to perform a frequency down-conversion from 18 kHz to 33 Hz. The rectification process in the IFLC is done by means of two stages of operational amplifiers (opAmp). Because of a GBP of 3.5 kHz, the opAmps rise and fall durations of the output voltage are longer than that of the input signal. The circuit is configured as a non-inverting configuration with a gain of at least 30 dB per stage. An increase in gain results in an increase in rise and fall time. Therefore, the obtained signal is a rectified voltage of the carrier burst. A simulation is illustrated in Fig. 9b. The amplitude varies proportionally with the input power of the WuRx. Moreover, the logic level of

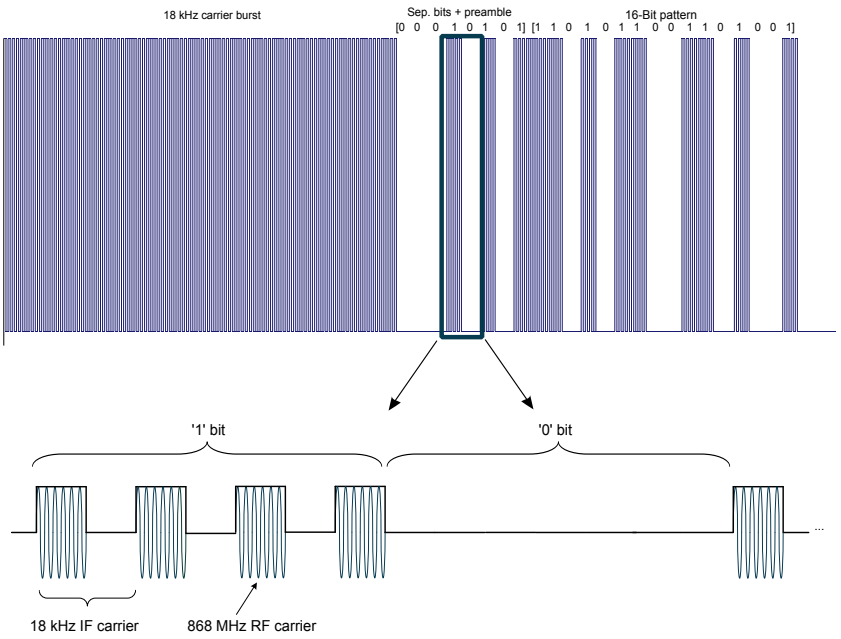

Figure 10. AS3933 wake-up packet structure.

$\overline{\text{SHDN}}$ implies that a HIGH signal should have an amplitude of minimum 0.7 VCC, and a LOW signal has to be maximum of 0.3 VCC. A comparator is incorporated to guarantee such logic control. The $\overline{\text{SHDN}}$ pulse is illustrated in Fig. 9c. The opAmp has a typical input voltage offset $V_{\text{OS}} = -100\,\mu\text{V}$, which proportionally increases with the gain and consumes $I_{\text{OpAmp}} = 330\,\text{nA}$. The comparator functions by comparing the input signal voltage to a reference voltage, and then yields a digital signal indicating which is greater. In this design, a suitable reference voltage together with comparator hysteresis are used to overcome false positives induced by either noise or DC offset. The chosen comparator TLV3691 consumes $I_{\text{Cmp}} = 75\,\text{nA}$ with a maximum propagation delay $t_{\text{PD}} = 45\,\mu\text{s}$ (Texas Instruments, 2013). The overall power consumption of the IFLC is calculated in the following expression.

$$I_{\text{IFCL}} = 2I_{\text{OpAmp}} + I_{\text{Cmp}} = 735\,\text{nA} \tag{8}$$

3.5 Address decoder

AS3933 is a three-channel low-frequency WuRx which operates within the 15–150 kHz frequency range. In the proposed design, the WuRx uses the ON/OFF low-power listening mode for energy economy. The mode functions by activating all three channels simultaneously for a duration of 1 ms and deactivating them for a specific duration $t_{\text{AS3933\_Sleep}}$ which reaches a maximum value of 8 ms. The decoder is able to decode a 16/32 bit OOK modulated wake-up pattern. The WuPt structure should comply with the decoder's as described by the manufacturer. The sequence contains a carrier burst, separation bits, a preamble, and a user-defined pattern. The AS3933 supports Manchester-encoded packets. However, to avoid further complications in WuPt generation, Manchester encoding is disabled. On the other hand, the decoder has a set of timing rules regarding carrier burst, preamble, and pattern durations and that depends on carrier and clock frequencies. For a carrier frequency $f_{\text{c}} = 18\,\text{kHz}$, the two following relations are mainly used to determine the exact timings of the different parts of the WuPt in order to fulfill the AS3933 protocol rules.

$$f_{\text{RCClk}} = f_{\text{c}} \frac{14}{8}, \tag{9}$$

$$\frac{92}{f_{\text{RCClk}}} + \frac{8}{f_{\text{c}}} < t_{\text{C}} < \frac{155}{f_{\text{RCClk}}}, \tag{10}$$

where f_{RCClk} is the clock frequency. From Eqs. (9) and (10), $t_{\text{C}} = 4.9\,\text{ms}$ is chosen in the current design and $f_{\text{RCClk}} = 31.5\,\text{kHz}$. Moreover, the decoder incorporates a specific protocol with the purpose of recognizing preamble and pattern bits. A "1" bit for the decoder is a successive number $N_{\text{C\_}T}$ of ON/OFF periods of the carrier signal which has to last a user-defined number $N_{\text{CLK\_}T}$ of clock periods. The same principle applies for a "0" bit, but only with the complete absence of the carrier (OFF periods). The internal RC oscillator is used to generate the clock signal. The AS3933 supports a bit rate within the range of $[1, 8]\,\text{kbit}\,\text{s}^{-1}$. According to the design requirements, AS3933 is programmed to perform an address decoding at a bit rate of $4.57\,\text{kbit}\,\text{s}^{-1}$. The decoder uses a clock signal to help frequency and bit detection. The number of clock periods varies depending on the chosen bit rate and, in this case, $N_{\text{CLK\_}T} = 7$. Conversely, the carrier has to last a number of ON/OFF periods $N_{\text{C\_}T}$ equal to seven clock peri-

ods. The relation is calculated in the following expression.

$$N_{C\_T} = \frac{f_c}{f_{RCClk}} N_{CLK\_T} \quad (11)$$

A WuPt, which complies with the above settings, is illustrated in Fig. 10, where $f_c = 18$ kHz, $N_{C\_T} = 4$ and the pattern is `0xD669`. The total WuPt duration is $t_{WuPt} = 10.3$ ms. With a 16 bit address length it is possible to have 256 unique patterns when Manchester encoding is disabled and 65 536 otherwise. AS3933 supports three modes of operation: standard listening, scanning mode and ON/OFF mode. For the first, all channels are active simultaneously. For scanning mode, the listening is done on the channels one by one with the condition of having one active channel only at a time. The last mode scans all three channels at once for 1 ms, then switches them off to conserve energy for a configurable time t_{off} ranging from 1 to 8 ms. For $t_{off} = 8$ ms, the current consumption of AS3933 is measured at 1.7 µA.

3.6 Wireless module

An open-source WSn platform referred to as PanStamp AVR (PanStamp, 2014) is used as a host for the designed WuRx. It features a low-power 8 bit 8 MHz MCU, the Atmega328P from Atmel (Atmel, 2016). Additionally, the PanStamp incorporates the CC1101 radio chip (Texas Instruments, 2007), which operates at 433 and 868–915 MHz. The total power consumption of both chips in the lowest power-saving modes is $P_{Pan.S\_Sleep} = 159$ nA, which represents the main reason for choosing the wireless module. To wake up the mote, an interrupt has to be induced through a user-defined pin. The WuRx induces the corresponding interrupt once the correctly addressed WuPt is received. The PanStamp is also used as a wake-up transmitter (WuTx) since the radio chip is able to handle amplitude-shift keying (ASK) and OOK modulation schemes. With the chosen configuration of the AS3933 in this design, the WuPt has a total length of 48 bytes. The CC1101 supports a 64 byte transmission FIFO queue, enough to handle the transmission of the complete WuPt.

Unlike Gamm et al. (2014), the number of bytes of a WuPt exceeds the FIFO size because of the higher carrier frequency (125 kHz) and the use of Manchester encoding. A solution they adopted is by re-filling the FIFO queue each time it is saturated until the WuPt is completely transmitted. Such a procedure elevates the complexity of the design. Moreover, the CC1101 contains a specific packet structure provided in Fig. 11. The packet is programmed in such a way that it matches the desired WuPt. Therefore, preamble, synchronization, length and address fields are set to the `0xAA` value to represent the carrier burst of WuPt. The data field contains the rest of the carrier burst, separation bits, preamble and pattern bytes. The code redundancy check (CRC) is disabled and its corresponding field contains `0x0` bytes. The CC1101 is able to transmit a packet with transmission power up to +11 dBm.

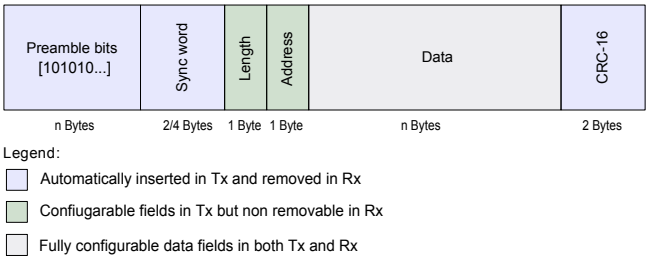

Figure 11. CC1101 packet structure.

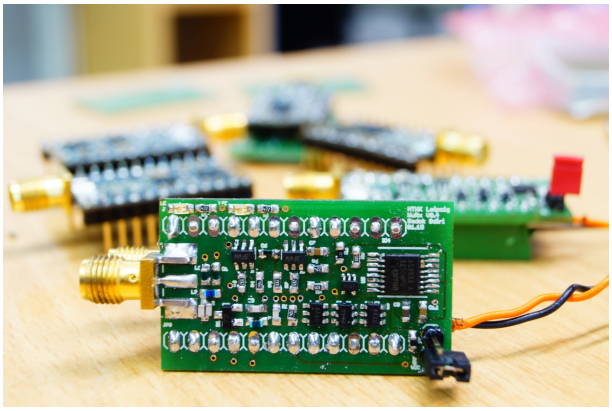

Figure 12. Assembled WuRx PCB and attached to a host node.

4 System evaluation

In this section, a proof of concept for the presented WuRx design is carried out for experimental evaluation. Performance evaluation is expressed in terms of input impedance matching, power consumption, sensitivity, range communication and addressing capability. Different test beds are necessary to fill in a complete survey of measurements. A developed proof of concept can be seen in Fig. 12.

4.1 Hardware implementation

To concretize the explored design, prototypes are realized in order to gather multiple measurements. The circuitry is based on off-the-shelf commercially available components. The manufactured printed circuit board (PCB) is a two-layer 1.55 mm FR4 substrate with 35 µm copper width. The WuRx is interfaced with the host nodes through 24 pins. The WuTx node and the WuRx are programmed for the evaluation purpose. The execution flow chart is provided in Fig. 13.

Table 1 shows the general PCB characteristics of both devices. Various aspects like crosstalk, electromagnetic interference (EMI), electromagnetic compatibility (EMC) and impedance matching are represented under the umbrella term of "signal integrity". Most important for the proposed design interest is the impedance matching. It can affect the circuit to a great extent when dealing with high-frequency

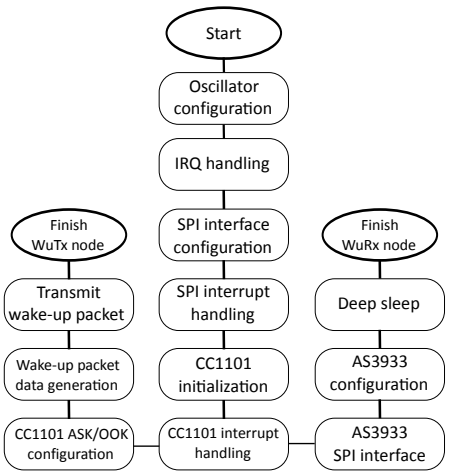

Figure 13. WuTx and WuRx node execution flow chart.

Table 1. PCB settings of PanStamp AVR and WuRx.

	WuRx	PanStamp AVR PanStamp (2014)
Layers (mm)	2	4
Substrate	FR4	FR4
Thickness (mm)	1.55	1
Width (mm)	22	17.7
Length (mm)	37	30.5

signals. To avoid problems caused by such aspects, PCB traces and transmission lines are carefully designed and kept as short as possible. The theoretical load impedance of the WuRx using the available diode model in advanced design system (ADS) from Agilent (Agilent Technologies, 2016) is $Z_{\text{load}} = 33.6 - j392\,\Omega$. An impedance matching network is essential to match the circuit to a 50 Ω system for maximum power transfer between source and load. Manufacturing conditions alter the impedance of diodes with every released product, thus deriving from a theoretical load impedance. For such reasons, practical Z_{load} is measured by means of a network analyzer to be able to determine the appropriate impedance matching network. However, the parasitic resistance of the Schottky diodes changes with the induced signal power, which alters the Z_{load} of the circuit. A quasi-optimal matching network is designed with respect to an input signal power of less than −40 dBm. Nonetheless, component trimming is also necessary to overcome the matching errors. A measurement of the reflection coefficient S_{11} at the WuRx input on a log-magnitude plot and a Smith chart is provided in Fig. 14.

Changing the operation frequency of the WuRx within [867, 870] MHz does not alter the performance of the circuit, although a benefit is found as the frequency can be changed freely within a certain bandwidth. An example could be the

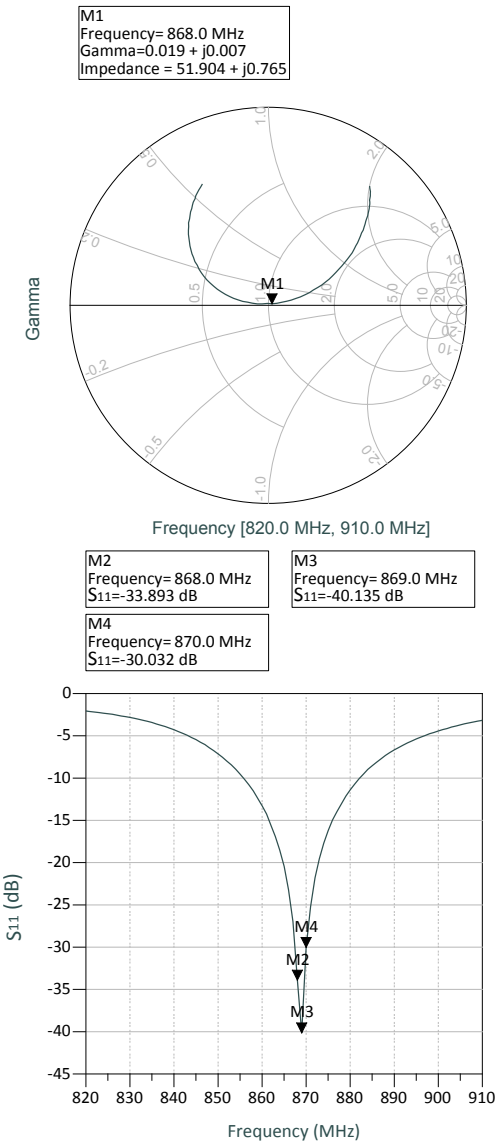

Figure 14. Measurement of the reflection coefficient (S_{11} / Γ) at the input of the WuRx.

use of one channel for WuRx and another channel for normal communication between nodes to avoid collision or interference.

To characterize the performance of the WuRx, a voltage output measurement of each block is performed individually during the WuPt decoding phase. A data capture from an oscilloscope is shown in Fig. 15.

The WuTx is programmed to send two WuPts successively every 0.5 s. The oscilloscope is triggered upon a received HIGH level signal from the decoder. As explained in the previous chapter, the IFLC has to generate an enable pulse in order to enable the IF amplifiers during reception of a WuPt. The waveform of the pulse can be observed in Fig. 15.

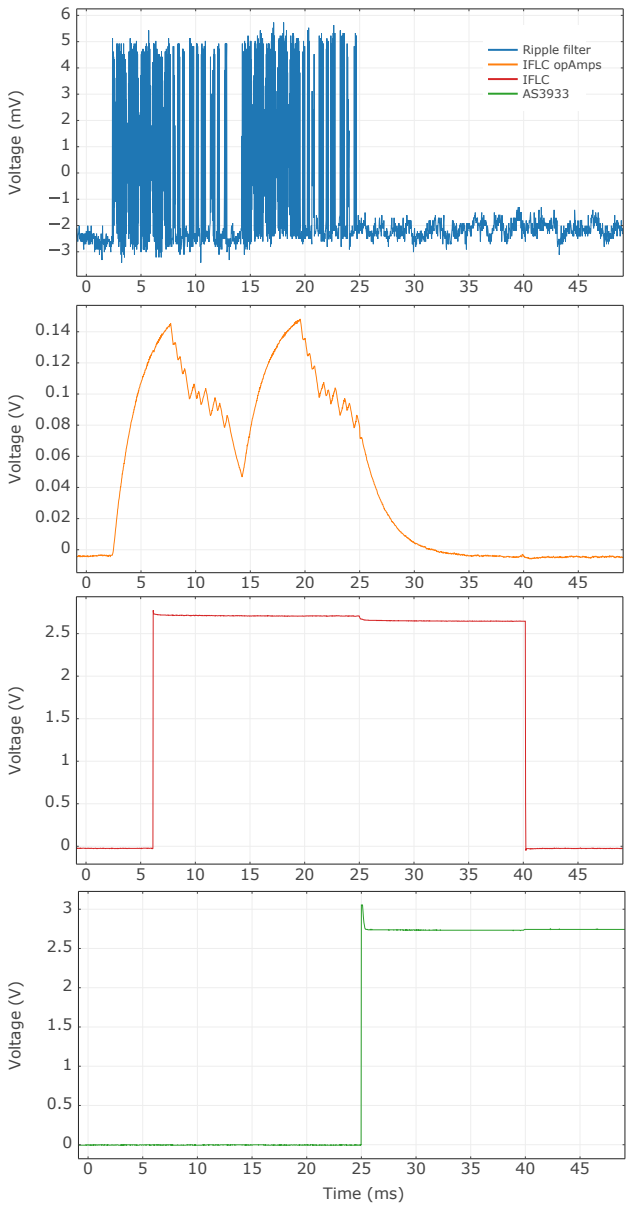

Figure 15. Measurement of ripple filter, IFLC opAmps, IFLC and AS3933 outputs while receiving a WuPt with an input power of −40 dBm.

However, a delay is noticeable between the first WuPt and the pulse, thus making the IF amplifiers amplify an incomplete WuPt. The latter does not comply with the decoder's WuPt protocol. The rise time of the opAmps output signal causes the delay. Moreover, the second WuPt is sent after 1.6 ms, which is shorter than the fall time of the opAmps and prevents the generated pulse from going LOW. Accordingly, the second WuPt is not compromised and fed to the AS3933 after amplification. Furthermore, as a practice, two WuPts are sent each time to compensate for the delay problem or by extending the carrier burst.

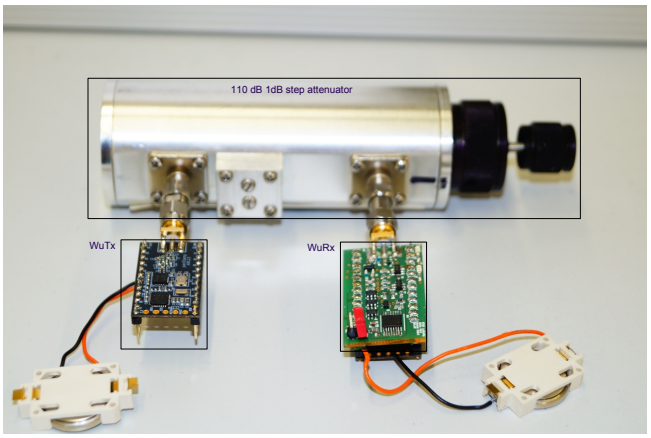

Figure 16. Assembled WuRx PCB and attached to a host node.

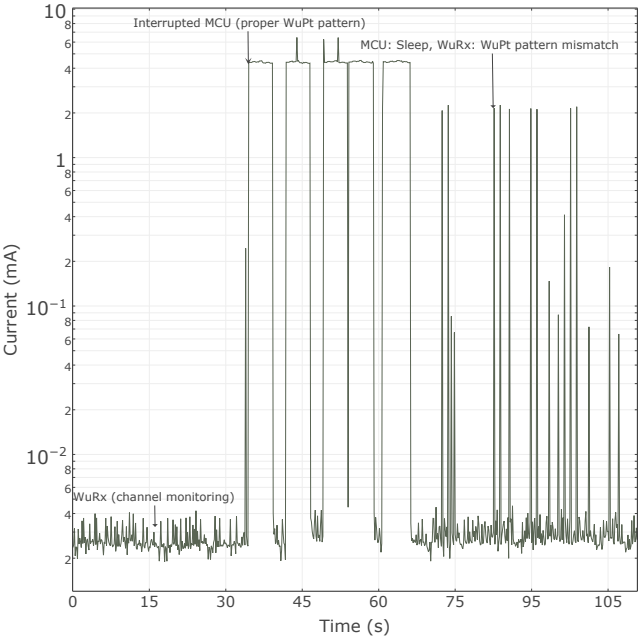

Figure 17. System current consumption in different operation states.

4.2 Sensitivity

One of the main challenges of designing the WuRx is to achieve at least −55 dBm of sensitivity while remaining within the ultra-low-power budget in order to have practical network coverage. Sensitivity is defined by the minimum received signal power at which the circuit is able to successfully interpret the received packets. Nonetheless, packet error rate (PER) is also essential to characterize the performance of a radio receiver. A value of 1 % of PER is the tolerated performance for WuRx. In order to retrieve experimental measurement of the WuRx's sensitivity, a WuTx is connected to the WuRx with an attenuator in between as described in Fig. 16. The WuRx is configured to transmit 100 WuPts with

Table 2. Current consumption of WuRx and PanStamp in different states.

Components	Channel monitoring (µA)	WuPt decoding (µA)
Envelope detector	0	0
Ripple filter	0	0
IFLC	0.73	0.735
IF amplifiers	0.03	2090
AS3933	1.7	8
PanStamp	0.159	0.159
Total	2.53	2099

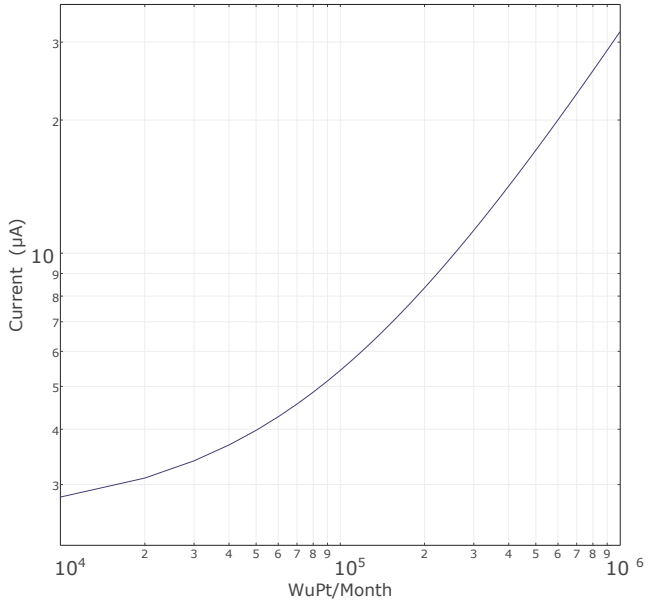

Figure 18. Average WuRx current usage as a function of the number of received WuPts per month.

a transmission power of $P_{Tx} = 3$ dBm. Upon reception of a WuPt, the decoder interrupts the MCU, resulting in a blinking blue LED. A step further using the attenuator, the transmission power is attenuated until no interrupt is induced to the MCU. A successful interrupt can be seen till an attenuation level of 63 dB. Now, a spectrum analyzer is connected to the attenuator instead of the WuRx. At 868.01 MHz, the measured signal amplitude varies within $[-60.5, -60]$ dBm, with the same attenuation level. Therefore, the WuRx's minimum sensitivity is considered to be $P_S = -60$ dBm.

4.3 Power consumption

Energy usage characterizes a WuRx design. With that in mind, an energy usage profile analysis is performed on a host node with an embedded WuRx. The measurement covers possible system operational modes. As illustrated in Fig. 17, the measurements last 110 s. At first, the WuTx is configured to continuously send two WuPts every 0.5 ms. The pattern included in the WuPts matches the one configured in the WuRx's decoder. By starting the measurement, the receiving node is set to deep sleep mode, while the WuRx monitors the channel for an incoming WuPt. On average, the system consumes 2.5 µA of current. After an elapsed time of ∼ 35 s, the WuTx starts transmitting WuPts, making the WuRx successfully interrupt the MCU. The consumption jumps to 4 mA; the MCU remains active for certain time while performing tasks, and then switches back to deep sleep mode. After a total duration of 70 s, the WuTx is programmed to send WuPts with patterns different than that of the WuRx. After initiating the WuPts transmissions, the WuRx consumes 2.1 mA, which is mostly caused by the IF amplifier stages.

Table 3. Range test at different WuTx transmission powers.

Transmission power (dBm)	Distance (m)
−10	8.3
0	26.2
3	40.2
10	82.5
11	92.9

Table 4. Wake-up receiver specifications summary.

Specification	Value	Condition
Sensitivity	−60 dBm	4.57 kbit s^{-1}, PER = 1 % 10.3 ms latency
Input impedance	$33.6 - j392\Omega$	Simulated
Wake-up pattern	16 bit	No Manchester
Bit rate	1–8 kbit s^{-1}	Decoder bit rate
Supply voltage	2.85–3.6 V	
Current supply	2.53 µA	Channel monitoring
	2099 µA	WuPt decoding
Power-on time	10 ms	

Furthermore, Table 2 summarizes the current consumption of WuRx parts for different operation modes including the host node. The WuPt power consumption is crucial when decoding a WuPt.

Application of a WuRx implies that a WuPt is sent only at event-triggering trends. For such reasons, the total duration in which the WuRx decodes a WuPt is significantly less than the duration of channel monitoring. For evaluation purposes, the WuRx's activity time is set at $t_{Active} = 35$ ms. The average current consumption I_{WuRx} is calculated in Eq. (12).

$$I_{WuRx} = I_{CM} + D(I_D - I_{CM}), \tag{12}$$

where I_{CM} and I_D are the current consumptions of WuRx in the channel monitoring and WuPt decoding states, respectively. In this case, D is the duty cycle of the WuRx's activity over a total period $t_{total} = 1$ month, and it is expressed in

Table 5. Wake-up receiver prototype comparison.

	This work	Hambeck et al. (2011)	Marinkovic and Popovici (2011)	Gamm et al. (2014)	Pletcher et al. (2008)
Frequency (GHz)	0.868	0.868	0.433	0.868	2
Current (µA)	2.5	2.4	0.270	2.78	104
Sensitivity (dBm)	−60	−71	−51	−53	−72
Range (m)	82[b]	304[c]	10[d]	37[b]	N/A
Data rate (kbps)	4.5	20/200	5.5	NA	100
Addressing	✓	✓	✓	✓	
Implementation	OtS[a]	130 nm	OtS[a]	OtS[a]	90 nm

[a] Off-the-shelf. [b] 10 dBm Tx power. [c] 6.5 dBm Tx power. [d] 0 dBm Tx power.

Eq. (13).

$$D = N_{\mathrm{Pt/M}} \frac{t_{\mathrm{active}}}{t_{\mathrm{total}}} \tag{13}$$

The resulting relation is plotted in Fig. 18.

For 10^4 received WuPts packets in 1 month, the average current consumption is $I_{\mathrm{WuRx}} = 2.76\,\mu\mathrm{A}$.

4.4 Range

Improving a radio receiver's sensitivity is mainly performed to extend the wireless coverage of the network. Nevertheless, other parameters like antenna gains and path losses also have an impact on the communication distance R. The relations between these parameters are expressed in the Friis equation (Eq. 14).

$$\frac{P_{\mathrm{r}}}{P_{\mathrm{t}}} = G_{\mathrm{r}} G_{\mathrm{t}} \left(\frac{\lambda}{4\pi R} \right)^2, \tag{14}$$

where P_{r} and P_{t} are, respectively, the received and transmitted signal power. G_{r} and G_{t} represent the antenna gains of the receiver and the transmitter, respectively. However, such a relation stands in an ideal condition where reflections, diffractions and atmospheric absorption are not present. Therefore, the communication range is significantly different between indoor and outdoor applications. A practical range test of the network is realized in a free-space line-of-sight glance to measure the maximum possible coverage. The WuTx is set fixed on a pole at a height of 1.5 m and the WuRx is reallocated until no WuPt is received. The used antennas are omnidirectional monopole antennas with a gain of 2 dBi. Depending on the WuTx transmission power, different obtained ranges are listed in Table 3.

With a sensitivity of −60 dBm, the resulting range between the WuRx and the WuTx is considered the widest coverage achieved by a WuRx implemented with off-the-shelf components whilst regarding the energy consumption. At 10 dBm, a received WuPt is observed at a maximum distance of 82 m. As expected, this is lower than the equivalent distance of 137.7 m, calculated from Eq. (14). Nevertheless, these results are still better than Gamm et al. (2014), Marinkovic and Popovici (2011), and Magno et al. (2016). Characteristic WuRx parameters are summarized in Table 4.

The present WuRx features are compared to those of recently published ultra-low-power radios and are provided in Table 5.

5 Conclusion

Ultra-low power for real-time constrained wireless WSNs is introduced. The paper describes the rationale behind the system design and the protocol details of a wake-up receiver. A novel WuRx architecture is adopted by taking the benefit from the communication scheme of an event-triggering application. Such architecture makes it possible to enhance the WuRx sensitivity while remaining within the micro-power budget. The current design is able to achieve a sensitivity of −60 dBm while consuming 2.53 µA of a current in channel monitoring mode and is able to decode a 16 bit wake-up pattern. At 10 dBm of WuPt transmission power, a communication range of nearly 82 m in the line-of-sight scheme is observed. Such coverage enables most of the on-demand WSNs applications. The WuRx performance is affected by the interferences. Further revisions aim to resolve this issue as well as incorporate an MCU and transceiver on the same board.

6 Data availability

The dataset of the envelope detector simulation can be accessed in an open repository by using the link below: http://dx.doi.org/10.17632/6d44wht7n3.1 (Bdiri, 2016).

Sadok Bdiri received the engineering diploma in computer and embedded systems from the National Engineering School of Sousse (ENISo), Sousse, Tunisia, in 2011, an MS degree in robotics from the National Engineering School of Sfax (ENIS), Sfax, Tunisia, in 2013, and is currently pursuing a PhD degree in information technology and electrical engineering at the Leipzig University of Applied Sciences, Germany. In addition to wake-up receivers, he is also concerned with low-power radios and embedded systems.

Faouzi Derbel has been Professor for Smart Diagnostic and Online Monitoring at the Leipzig University of Applied Sciences, Germany, since 2013. His research activities are focused on wireless sensor networks and sensor systems with intelligent signal processing. In 2001, he obtained his PhD degree in electrical engineering from the University of the Bundeswehr Munich. From 2000 to 2012 he held different positions within Siemens and Qundis Advanced Measuring Solutions, e.g., systems engineer, head of the product innovation department and head of research and development. In 2012, he was Professor for Electrical Measurement Technologies at the University of Applied Sciences Zwickau, Germany. Faouzi Derbel is a member of many technical groups dealing with short-range devices. He is Editor-in-Chief of the ASSD (Advances in Systems, Signals and Devices, Issues on Communication and Signal Processing, De Gruyter Verlag, Germany) and holds many awards and patents.

Olfa Kanoun has been a university professor of measurement and sensor technology at Chemnitz University of Technology, Germany, since 2007. Her research focus is on the design of sensors and sensor systems. For more than 15 years, she has worked on power-aware wireless sensors with a focus on energy harvesting and energy management. Other research interests are in nanocomposite sensors and impedance spectroscopy.

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