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Article

Synthesis of Cascadable DDCC-Based Universal Filter Using NAM

Huu-Duy Tran [1,2], Hung-Yu Wang [1,*], Min-Chuan Lin [3] and Quoc-Minh Nguyen [1]

[1] Department of Electronic Engineering, National Kaohsiung University of Applied Sciences, Kaohsiung 807, Taiwan; E-Mails: duyth@dlu.edu.vn (H.-D.T.); minhoba@ymail.com (Q.-M.N.)

[2] Department of Physics, University of Dalat, Dalat City, Vietnam

[3] Department of Electronic Engineering, Kun Shan University, Tainan 710, Taiwan; E-Mail: mc.lin@seed.net.tw

* Author to whom correspondence should be addressed; E-Mail: hywang@kuas.edu.tw; Tel.: +886-7-381-4526 (ext. 5640); Fax: +886-7-381-1182.

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Abstract: A novel systematic approach for synthesizing DDCC-based voltage-mode biquadratic universal filters is proposed. The DDCCs are described by infinity-variables' models of nullor-mirror elements which can be used in the nodal admittance matrix expansion process. Applying the proposed method, the obtained 12 equivalent filters offer the following features: multi-input and two outputs, realization of all five standard filter functions, namely lowpass, bandpass, highpass, notch and allpass, high-input impedance, employing only grounded capacitors and resistors, orthogonal controllability between pole frequency and quality factor, and cascadable, low active and passive sensitivities. The workability of some synthesized filters is verified by HSPICE simulations to demonstrate the feasibility of the proposed method.

Keywords: voltage-mode; universal filter; cascadable; NAM; DDCC

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1. Introduction

Due to the capability to realize simultaneously multiple filter functions with the same topology, continued researches have focused on the realization of universal filters. The design of biquadratic voltage-mode active filters with high-input impedance has received much interest since they can be directly cascaded to implement higher order filters without the use of additional buffer circuits [1]. Many voltage-mode universal biquadratic filters using current conveyors with multi-input/multi-output were proposed in the literature [2–10].

Recently, a symbolic framework for systematic synthesis of a linear active circuit without any detailed prior knowledge of the circuit form was presented [11–15]. This method, called nodal admittance matrix (NAM) expansion, is very useful to generate various novel circuits in a systematic way. Based on this method, various active networks such as filters, oscillators and gyrators employing OTA, CCII, BOCCII, DVCC and CCCCTA have been synthesized [16–21]. The circuit synthesis procedure proposed in [12] is suitable to synthesize discrete transfer functions with different circuit topologies. It is difficult to synthesize multiple filter functions using an identical topology. The systematic generation of current-mode filters using NAM expansion was reported in [16]. The trans-impedance filter synthesis based on NAM expansion was reported in [17]. In [19], the synthesis of CCII-based voltage-mode high-Q biquadratic notch filter was reported recently.

Since the differential difference current conveyor (DDCC) is a circuit similar to a DDA at the input side and a CCII at the output side [22], it enjoys the combined advantages of the CCII and DDA with high-input impedance, low-output impedance, greater design flexibility, larger signal bandwidth and wider current dynamic range, several universal filters using DDCCs have been proposed [23–26]. Unfortunately, most papers just propose their novel circuits; the design or synthesis methods for DDCC-based universal filters are not available.

In this paper, a systematic generation of cascadable DDCC-based universal voltage-mode biquadratic filters is presented. The obtained 12 filters configurations with two outputs can be used to realize all the five generic filter functions. They comprise three active elements and five passive grounded capacitors and resistors, with the features of high input impedance, low active and passive sensitivities, and orthogonal adjustability of the resonance angular frequency and quality factor. The filter with grounded capacitors is helpful for easing the elimination/accommodation of various parasitic effects for monolithic integration. HSPICE simulations for two illustrated derived filters confirm the workability of the obtained circuits, and hence demonstrate the feasibility of the proposed approach.

2. Description of the Proposed Method

The port relations of an ideal DDCC can be characterized by (1), where the plus and minus signs indicate whether the current conveyor is DDCC+ or DDCC−. Figure 1 shows the symbolic pathological representations of DDCCs. It is clear that each of terminal-Y_i (i = 1–3) possesses high input impedance.

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm 1 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{bmatrix} \quad (1)$$

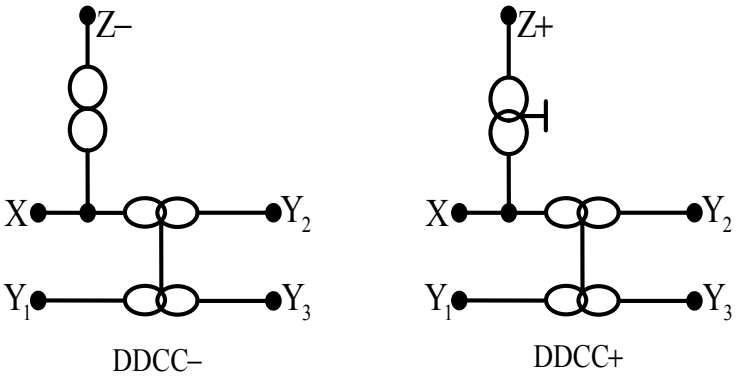

Figure 1. The symbolic pathological representations of DDCCs.

In the NAM expansion process, the addition of row and column of zero terms and infinity-variable terms with a common node on the primary diagonal of the admittance matrix is needed to transform the admittance terms to their correct form. The correct form set of admittance terms includes a unique positive term on the primary diagonal realizing a grounded admittance and a group of four terms with two positive terms on the primary diagonal and two negative terms on the off-diagonal representing a floating admittance. Therefore, in the synthesized circuits, pairs of pathological elements with a common node can be realized by the proper type of CCIIs [19].

The DDCC is similar to a CCII but with two more additional terminals, *i.e.*, terminal-Y_2 and terminal-Y_3. Thus, the DDCC- and DDCC+ can be respectively represented by infinity-variables notation given by Equations (2) and (3) in NAM expansion with the common node on the primary diagonal assigned to terminal-X. The signs of infinity-variables of terminal-Y_1 and terminal-Y_3 are different to that of terminal-X, while the signs of infinity-variables of terminal-X and terminal-Y_2 are identical. Based on the infinity-variables notation in (2) and (3), it can be seen that the connection between terminal-X and terminal-Y_1 or terminal-Y_3 corresponds to a nullator, and the connection between terminal-X and terminal-Y_2 corresponds to a voltage-mirror (VM). These relationships are very important for deriving the numerator of the transfer function of the synthesized filters.

$$\begin{matrix} Y_3 & Y_2 & Y_1 & X \end{matrix}$$
$$\begin{bmatrix} -\infty_i & \infty_i & -\infty_i & \infty_i \\ \infty_i & -\infty_i & \infty_i & -\infty_i \end{bmatrix} \begin{matrix} X \\ Z- \end{matrix} \quad (2)$$

$$\begin{matrix} Y_3 & Y_2 & Y_1 & X \end{matrix}$$
$$\begin{bmatrix} -\infty_i & \infty_i & -\infty_i & \infty_i \\ -\infty_i & \infty_i & -\infty_i & \infty_i \end{bmatrix} \begin{matrix} X \\ Z+ \end{matrix} \quad (3)$$

It is known that to synthesize filter circuits using NAM expansion, the denominator D(s) of a transfer function of a filter should be expressed as an admittance matrix in NAM equations shown in Equation (4). This matrix can be used as a starting matrix to find the circuit configuration with no input signals. Then, the equivalent circuit of an input voltage source as shown in Figure 2 can be injected to the obtained circuit represented by expanded NAM of (4) to obtain the voltage-mode filters [19].

$$\begin{bmatrix} y_{1,1} & y_{1,2} & \cdots & y_{1,j} & \cdots & y_{1,n} \\ y_{2,1} & y_{2,2} & \cdots & y_{2,j} & \cdots & y_{2,n} \\ \vdots & \vdots & \cdots & \vdots & \cdots & \vdots \\ y_{i,1} & y_{i,2} & \cdots & y_{i,j} & \cdots & y_{i,n} \\ \vdots & \vdots & \cdots & \vdots & \cdots & \vdots \\ y_{n,1} & y_{n,2} & \cdots & y_{n,j} & \cdots & y_{n,n} \end{bmatrix} \quad (4)$$

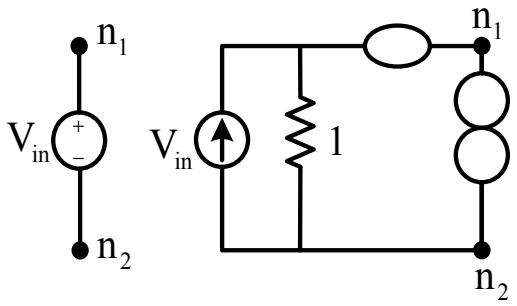

Figure 2. R-nullor equivalent circuit of a voltage source.

To synthesize DDCC-grounded capacitor-based filters using NAM expansion, we firstly use the NAM stamps of CCIIs [15] to expand the starting matrix in (4). The expanded NAM of (4) includes the correct form of admittance elements and pairs of infinity-variables represented terminal-X, terminal-Z and one terminal-Y_i of DDCCs. The remained Y_i-terminals can be used to inject the input voltage source for deriving high input impedance filters. The procedure can be summarized as follows.

Step 1: Of the desired transfer function of the synthesized filter in the form of the Matrix (4). It must be noted that each capacitor in the denominator must be arranged to have only a single position on the primary diagonal to obtain circuits with grounded capacitors.

Step 2: Introduce a row and a column of zeros to row 1 and column 1 and place a unity resistor to position (1,1) of (4). The existing columns and rows are moved to the right and to the bottom, as given by (5). Then add infinity variables and zero terms to realize a nullator between column 1 and column 2 and a norator between row 2 and ground. The Step 2 corresponds to the adding of the equivalent circuit of voltage source in Figure 2 [19]. So, Matrix (5) becomes (6).

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & y_{1,1} & y_{1,2} & \cdots & y_{1,j} & \cdots & y_{1,n} \\ 0 & y_{2,1} & y_{2,2} & \cdots & y_{2,j} & \cdots & y_{2,n} \\ \vdots & \vdots & \vdots & \cdots & \vdots & \cdots & \vdots \\ 0 & y_{i,1} & y_{i,2} & \cdots & y_{i,j} & \cdots & y_{i,n} \\ \vdots & \vdots & \vdots & \cdots & \vdots & \cdots & \vdots \\ 0 & y_{n,1} & y_{n,2} & \cdots & y_{n,j} & \cdots & y_{n,n} \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & y_{1,1} & y_{1,2} & \cdots & y_{1,j} & \cdots & y_{1,n} \\ 0 & 0 & y_{2,1} & y_{2,2} & \cdots & y_{2,j} & \cdots & y_{2,n} \\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots & \cdots & \vdots \\ 0 & 0 & y_{i,1} & y_{i,2} & \cdots & y_{i,j} & \cdots & y_{2,n} \\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots & \cdots & \vdots \\ 0 & 0 & y_{n,1} & y_{n,2} & \cdots & y_{n,j} & \cdots & y_{n,n} \end{bmatrix} \tag{6}$$

Step 3: Use the NAM expansion method to expand the Matrix (6) [12,15]. The obtained matrix can be expressed by (7), for example.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & y_{1,1} & \infty_i & \cdots & y_{1,j} & \cdots & y_{1,n} & -\infty_i \\ 0 & 0 & y_{2,1} & y_{2,2} & \cdots & y_{2,j} & \cdots & y_{2,n} & 0 \\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots & \cdots & \vdots & \vdots \\ 0 & 0 & y_{i,1} & y_{i,2} & \cdots & y_{i,j} & \cdots & y_{i,n} & 0 \\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots & \cdots & \vdots & \vdots \\ 0 & 0 & y_{n,1} & y_{n,2} & \cdots & y_{n,j} & \cdots & y_{n,n} & 0 \\ 0 & 0 & 0 & -\infty_i & 0 & 0 & 0 & 0 & y_{1,2} + \infty_i \end{bmatrix} \tag{7}$$

Step 4: Add pair of infinity-variables of remained Y_i-terminals represented by (2) or (3) to the suitable positions in column 2 of the Matrix (7) to realize the infinity-variables notation of a DDCC+ or DDCC−. This operation will duplicate the existing admittance terms to the first column of (5), so the numerator of the desired transfer function is obtained. For example, by adding a pair of $\pm \infty_i$ to the second column of (7), the term $y_{1,2}$ will be duplicated in the first column of (5) to obtain the desired numerator, as shown in (8). The addition of infinity-variable pairs to column 2 corresponds to applying input voltage signal to the added Y_i-terminals at node 2. This operation will not affect the denominator of the transfer function. The obtained matrix represents the full matrix of the synthesized circuit.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \pm\infty_i & y_{1,1} & \infty_i & \cdots & y_{1,j} & \cdots & y_{1,n} & -\infty_i \\ 0 & 0 & y_{2,1} & y_{2,2} & \cdots & y_{2,j} & \cdots & y_{2,n} & 0 \\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots & \cdots & \vdots & \vdots \\ 0 & 0 & y_{i,1} & y_{i,2} & \cdots & y_{i,j} & \cdots & y_{i,n} & 0 \\ \vdots & \vdots & \vdots & \vdots & \cdots & \vdots & \cdots & \vdots & \vdots \\ 0 & 0 & y_{n,1} & y_{n,2} & \cdots & y_{n,j} & \cdots & y_{n,n} & 0 \\ 0 & \pm\infty_i & 0 & -\infty_i & 0 & 0 & 0 & 0 & y_{1,2}+\infty_i \end{bmatrix} \quad (8)$$

It can be observed that in the starting Matrix (5), the node 1 is chosen as input voltage node and other nodes can be output nodes. In (6), the node 1 and node 2 are connected by a nullator then they are equivalent to the input node, and other nodes can be output nodes. In Step 4, each pair of infinity-variables added to the second column of the obtained matrix in Step 3 corresponds to the injecting of input voltage signal to one Y-terminal of DDCCs. So, the circuits with high input impedance and multi-input and multi-output properties can therefore be synthesized.

3. Application Examples

We hope to synthesize biquadratic voltage-mode universal filters using a minimum number of passive elements with independent adjustable parameters of Q factor and pole frequency. The denominator of the transfer function is chosen as (9).

$$D(s) = s^2C_1C_2 + sC_2G_1 + G_2G_3 \quad (9)$$

According to the procedure of Step 1 in Section 2, the Equation (9) is expressed by (10) and (11) in the form of (4).

$$\begin{bmatrix} G_1 + sC_1 & -G_2 \\ G_3 & sC_2 \end{bmatrix} \quad (10)$$

$$\begin{bmatrix} G_1 + sC_1 & G_2 \\ -G_3 & sC_2 \end{bmatrix} \quad (11)$$

The Matrices (10) and (11) are defined as NAM type-A and NAM type-B, respectively. They are used as the starting matrices in NAM expansion.

3.1. Synthesis of Type-A Universal Filters

Following Step 2 of the procedure in Section 2, the equivalent NAMs (12) and (13) are obtained from (10). In the Matrix (12), the node 1 is chosen as input node, nodes 2 and 3 are chosen as outputs, respectively denoted by V_{ou1} and V_{out2}. In (13), the output voltage nodes V_{out1} and V_{out2} are moved to node 3 and 4, respectively.

$$\begin{bmatrix} 1 & 0 & 0 \\ 0 & G_1 + sC_1 & -G_2 \\ 0 & G_3 & sC_2 \end{bmatrix} \tag{12}$$

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 \\ 0 & 0 & G_1 + sC_1 & -G_2 \\ 0 & 0 & G_3 & sC_2 \end{bmatrix} \tag{13}$$

Using Step 3, three columns and rows of zero terms are added and pairs of nullor-mirror elements represented by ∞_2, ∞_3 and ∞_4 are introduced to the right and bottom of Matrix (13). So, Matrix (13) can be expanded as (14). There are eight alternative cases (cases 1–8) in expanding the Matrix (13), as shown in Table 1.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1 + \infty_2 & -\infty_3 & -\infty_2 & \infty_3 & 0 \\ 0 & 0 & \infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1 + \infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2 + \infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3 + \infty_4 \end{bmatrix} \tag{14}$$

In (14), the DDCC(1), DDCC(2) and DDCC(3) are represented by terms $\pm\infty_2$, $\pm\infty_3$ and $\pm\infty_4$, respectively. Based on the NAM stamps in (2) and (3) and the common node on the primary diagonal assigned for terminal-X of a DDCC, the terminal-X of DDCC(1) can be node 5, terminal-Y_1 and terminal-Z (of minus-type DDCC) are connected to node 3. For the DDCC(2), the terminal-X is connected to node 6, terminal-Y_1 is connected to node 4 and terminal-Z (plus-type DDCC) is connected to node 3. For the DDCC(3), the terminal-X is connected to node 7, terminal-Y_1 is connected to node 3 and terminal-Z (minus type DDCC) is connected to node 4. All of the terminal-Y_2 and terminal-Y_3 of DDCC(1), DDCC(2) and DDCC(3) can be used to inject the input voltage source.

Using Step 4, by injecting the input voltage source into terminal-Y_2 of DDCC(1), the term $-sC_1$ will be added to position (2,1) of (12), then a highpass function at V_{out1} and bandpass function at V_{out2} can be obtained. This operation corresponds to the inserting of term $\pm\infty_2$ to the second column of (14), as shown in (15). The obtained filter represented by (15) is shown in Figure 3a with nodes V_{in2}, V_{in3}, V_{in4}, V_{in5} and V_{in6} being grounded.

By applying the input voltage source to terminal-Y_3 of DDCC(1), the term sC_1 will be also created in position (2,1) of (12). Therefore, the admittance matrix is shown in (16) and the obtained transfer functions at nodes V_{out1} and V_{out2} are identical to that obtained in (15) but with reverse signs. The derived circuit is shown in Figure 3a with moving the injected voltage source equivalent circuit to node V_{in2} and grounding nodes V_{in1}, V_{in3}, V_{in4}, V_{in5} and V_{in6}.

Table 1. Eight cases of expanding NAM Type-A.

NAM Type-A (Case 1)

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & -\infty_3 & -\infty_2 & \infty_3 & 0 \\ 0 & 0 & \infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix}$$

NAM Type-A (Case 2)

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & -\infty_3 & -\infty_2 & \infty_3 & 0 \\ 0 & 0 & \infty_4 & sC_2 & 0 & 0 & \infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & \infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix}$$

NAM Type-A (Case 3)

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & -\infty_3 & -\infty_2 & -\infty_3 & 0 \\ 0 & 0 & \infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & \infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix}$$

NAM Type-A (Case 4)

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & -\infty_3 & -\infty_2 & -\infty_3 & 0 \\ 0 & 0 & \infty_4 & sC_2 & 0 & 0 & \infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & \infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & \infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix}$$

NAM Type-A (Case 5)

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & -\infty_3 & \infty_2 & \infty_3 & 0 \\ 0 & 0 & \infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & 0 & \infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix}$$

NAM Type-A (Case 6)

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & -\infty_3 & \infty_2 & \infty_3 & 0 \\ 0 & 0 & \infty_4 & sC_2 & 0 & 0 & \infty_4 \\ 0 & 0 & \infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & \infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix}$$

NAM Type-A (Case 7)

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & -\infty_3 & \infty_2 & -\infty_3 & 0 \\ 0 & 0 & \infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & 0 & \infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & \infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix}$$

NAM Type-A (Case 8)

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & -\infty_3 & \infty_2 & -\infty_3 & 0 \\ 0 & 0 & \infty_4 & sC_2 & 0 & 0 & \infty_4 \\ 0 & 0 & \infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & \infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & \infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix}$$

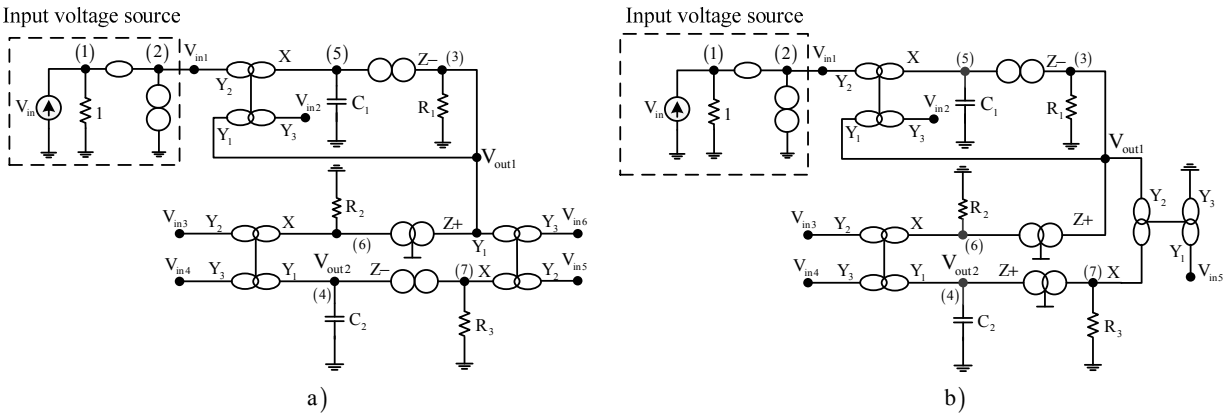

Figure 3. *Cont.*

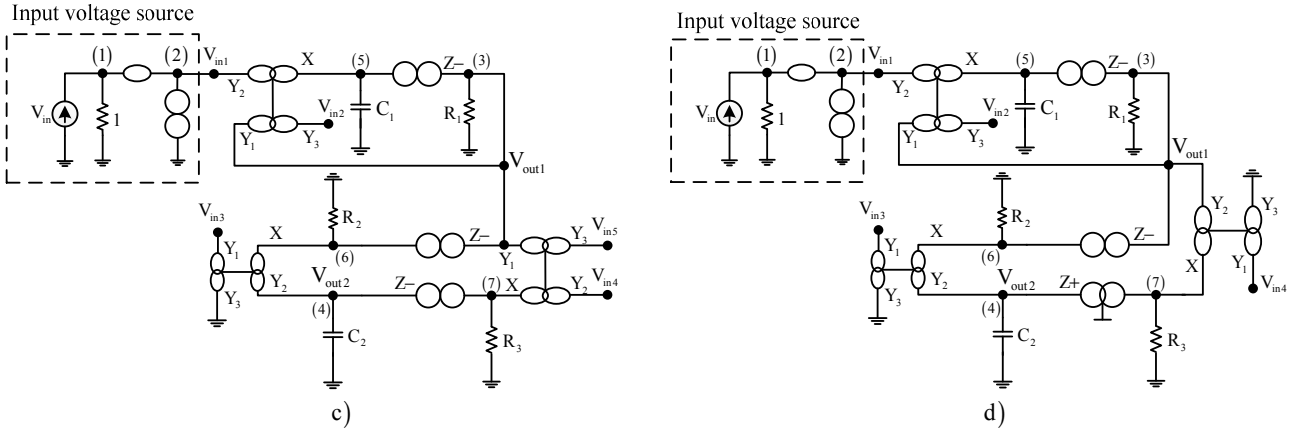

Figure 3. The pathological representations of derived type-A filters (cases 1–4).

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\infty_2 & G_1+\infty_2 & -\infty_3 & -\infty_2 & \infty_3 & 0 \\ 0 & 0 & \infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & \infty_2 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \quad (15)$$

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & \infty_2 & G_1+\infty_2 & -\infty_3 & -\infty_2 & \infty_3 & 0 \\ 0 & 0 & \infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & -\infty_2 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \quad (16)$$

Similarly, by applying the input voltage source to terminal-Y_2 of DDCC(2), term G_2 will appear in the position (2,1) of (12), then a bandpass function at V_{out1} and a lowpass function at V_{out2} can be obtained. The admittance matrix can be given in (17) and the derived circuit is shown in Figure 3a with moving the injected voltage source to node V_{in3} and grounding nodes V_{in1}, V_{in2}, V_{in4}, V_{in5} and V_{in6}.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & \infty_3 & G_1+\infty_2 & -\infty_3 & -\infty_2 & \infty_3 & 0 \\ 0 & 0 & \infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & \infty_3 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \quad (17)$$

By applying the input voltage source to terminal-Y_3 of DDCC(2), the term $-G_2$ will appear in position (2,1) of (12), then we can obtain the admittance matrix in (18) and the filter with identical

transfer functions as (17) but with different signs at nodes V_{out1} and V_{out2}. For the circuit in Figure 3a, moving the injected voltage source equivalent circuit to node V_{in4} with nodes V_{in1}, V_{in2}, V_{in3}, V_{in5} and V_{in6} as grounded nodes, we can obtain the filter represented by (18).

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\infty_3 & G_1+\infty_2 & -\infty_3 & -\infty_2 & \infty_3 & 0 \\ 0 & 0 & \infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & -\infty_3 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \quad (18)$$

Also, a lowpass function at V_{out1} can be achieved by applying the input voltage source to terminal-Y_2 of DDCC(3) when the term $-G_3$ appear in position (3,1) of (12). This operation corresponds to the inserting of terms $\pm\infty_4$ to the second column of (14), as shown in (19). The obtained circuit is shown in Figure 3a by moving the injected voltage source to node V_{in5} with nodes V_{in1}, V_{in2}, V_{in3}, V_{in4} and V_{in6} being grounded.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & -\infty_3 & -\infty_2 & \infty_3 & 0 \\ 0 & -\infty_4 & \infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & \infty_4 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \quad (19)$$

By applying the input voltage source to terminal-Y_3 of DDCC(3), term G_3 will arise in position (3,1) of (12), then the obtained transfer function at node V_{out1} is identical to the circuit represented by (19) with reverse sign. Its admittance matrix is shown in (20) and the circuit is given in Figure 3a by moving the injected voltage source to node V_{in6} with nodes V_{in1}, V_{in2}, V_{in3}, V_{in4} and V_{in5} being grounded.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & -\infty_3 & -\infty_2 & \infty_3 & 0 \\ 0 & \infty_4 & \infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & -\infty_4 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \quad (20)$$

In addition, a notch function at V_{out1} can be achieved by applying the input voltage source to terminal-Y_2 of DDCC(1) and terminal-Y_2 of DDCC(3) when the terms $-sC_1$ and $-G_3$ arise in positions (2, 1) and (3, 1) of (12), respectively. This operation corresponds to the inserting of terms $\pm\infty_2$ and $\pm\infty_4$ to the second column of (14), as shown in (21). The obtained circuit is given in Figure 3a by moving the injected voltage source to the merged node of V_{in1} and V_{in5} with nodes V_{in2}, V_{in3}, V_{in4} and V_{in6} being

grounded. Another notch function at V_{out1} can be also obtained by injecting the input voltage source to the merged node of V_{in2} and V_{in6} in Figure 3a with nodes V_{in1}, V_{in3}, V_{in4} and V_{in5} being grounded.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\infty_2 & G_1+\infty_2 & -\infty_3 & -\infty_2 & \infty_3 & 0 \\ 0 & -\infty_4 & \infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & \infty_2 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & \infty_4 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \quad (21)$$

Applying the input voltage source to terminal-Y_2 of DDCC(1), terminal-Y_2 of DDCC(2) and terminal-Y_2 of DDCC(3), terms $-sC_1+G_2$ and $-G_3$ will be created in positions (2, 1) and (3, 1) of (12), respectively, then an allpass function at V_{out1} (with $G_2 = G_1$) can be achieved. This operation corresponds to the insertion of the terms $\pm\infty_2$, ∞_3 and $\pm\infty_4$ to the second column of (14) as shown in (22). In Figure 3a, moving the injected voltage source to the merged node of V_{in1}, V_{in3} and V_{in5} with nodes V_{in2}, V_{in4} and V_{in6} being grounded, we can obtain the filter represented by (22). Another allpass function at V_{out1} can be also obtained by injecting the input voltage source to the merged node of V_{in2}, V_{in4} and V_{in6} in Figure 3a with nodes V_{in1}, V_{in3}, and V_{in5} being grounded.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\infty_2+\infty_3 & G_1+\infty_2 & -\infty_3 & -\infty_2 & \infty_3 & 0 \\ 0 & -\infty_4 & \infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & \infty_2 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & \infty_3 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & \infty_4 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \quad (22)$$

In the same way, the synthesized procedure can be applied to the matrices for cases 2–8 in Table 1. Four equivalent circuits of the derived filters for cases 1–4 of derived type-A filters in Table 1 are shown in Figure 3. The output transfer functions of the synthesized circuits for case 1 are given by (23) and (24). Besides, four equivalent circuits of the synthesized filters for cases 5–8 of derived type-A filters in Table 1 are shown in Figure 4. The output transfer functions of the synthesized circuits for case 5 are given by (25) and (26). Figure 5a–d and e–h show the practical configurations for the pathological equivalents in Figures 3 and 4, respectively.

$$V_{out1} = \frac{s^2C_1C_2V_{in1} - s^2C_1C_2V_{in2} - sC_2G_2V_{in3} + sC_2G_2V_{in4} + G_2G_3V_{in5} - G_2G_3V_{in6}}{s^2C_1C_2 + sC_2G_1 + G_2G_3} \quad (23)$$

$$V_{out2} = \frac{-sC_1G_3V_{in1} + sC_1G_3V_{in2} + G_2G_3V_{in3} - G_2G_3V_{in4} + G_3(G_1+sC_1)V_{in5} - G_3(G_1+sC_1)V_{in6}}{s^2C_1C_2 + sC_2G_1 + G_2G_3} \quad (24)$$

$$V_{out1} = \frac{s^2C_1C_2V_{in1} - sC_2G_2V_{in2} + sC_2G_2V_{in3} + G_2G_3V_{in4} - G_2G_3V_{in5}}{s^2C_1C_2 + sC_2G_1 + G_2G_3} \quad (25)$$

$$V_{out2} = \frac{-sC_1G_3V_{in1} + G_2G_3V_{in2} - G_2G_3V_{in3} + G_3(G_1 + sC_1)V_{in4} - G_3(G_1 + sC_1)V_{in5}}{s^2C_1C_2 + sC_2G_1 + G_2G_3} \quad (26)$$

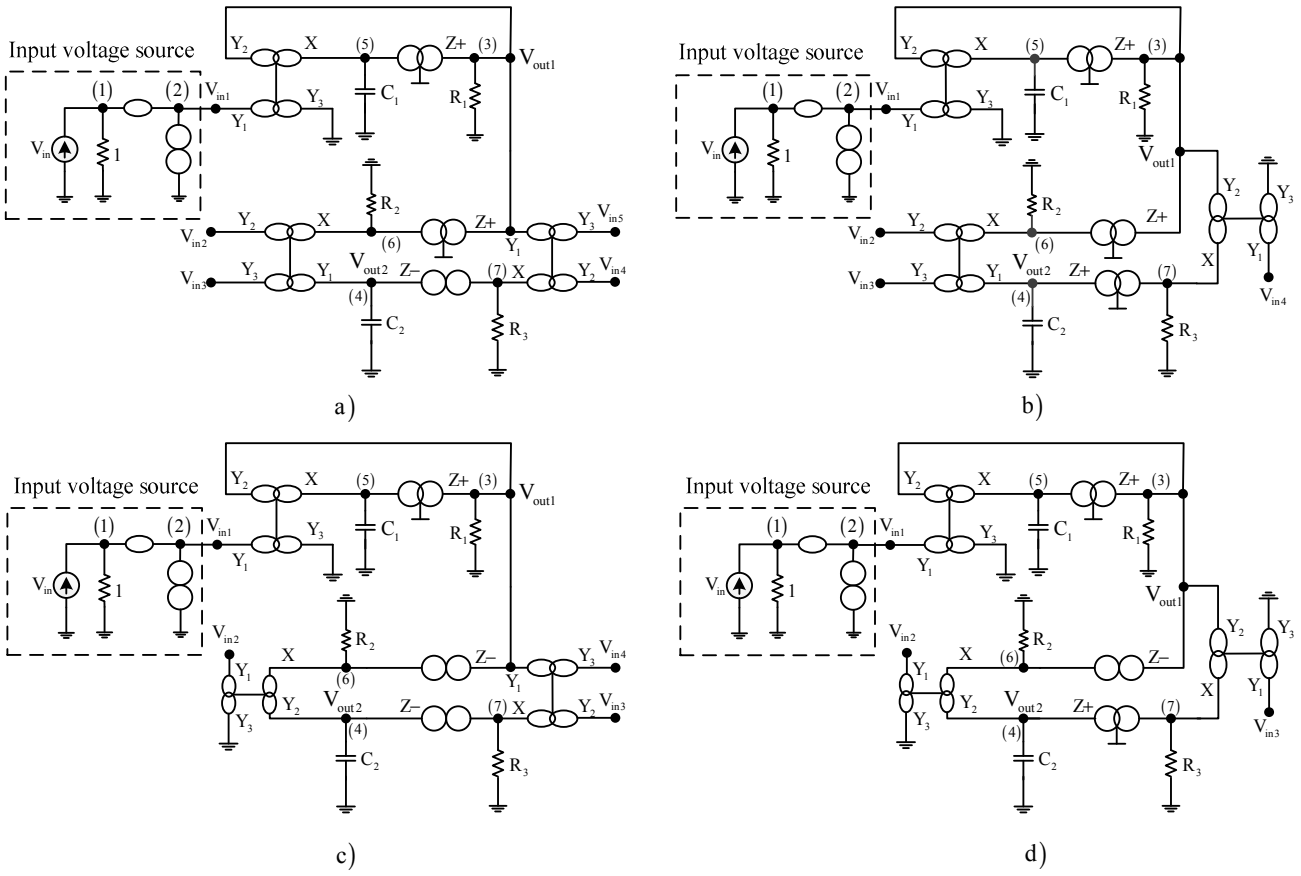

Figure 4. The pathological representations of derived type-A filters (cases 5–8).

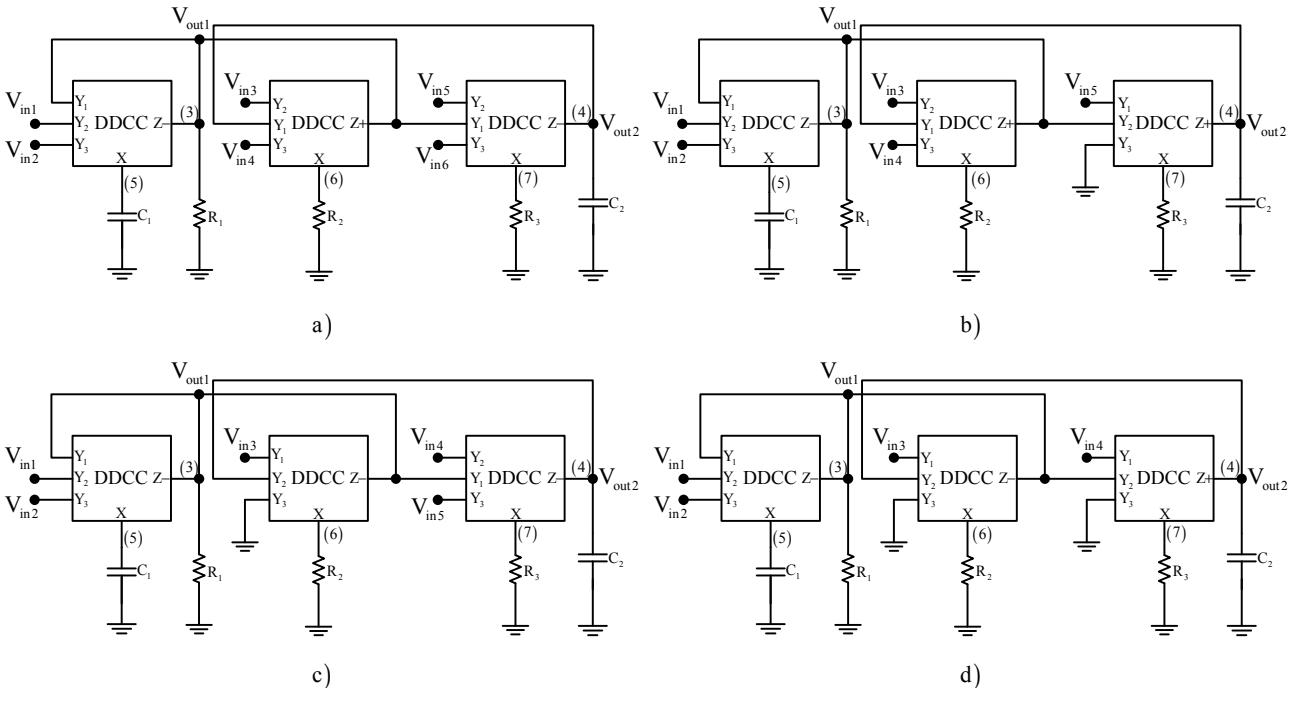

Figure 5. *Cont.*

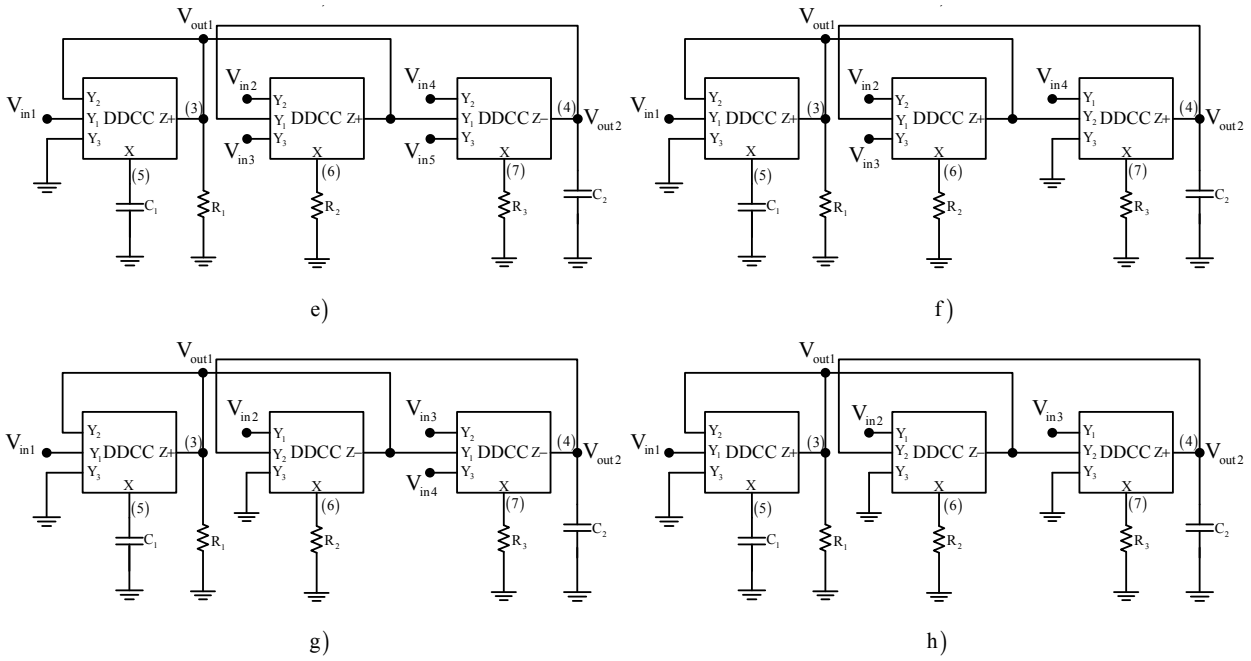

Figure 5. The practical configuration of type-A filters.

3.2. Synthesis of Type-B Universal Filters

Similarly, by applying Step 2, the equivalent NAMs (27) and (28) are obtained from (11). Applying Step 3, the Matrix (28) can be expanded as (29). There are four alternative cases (cases 1–4) that can be derived by expanding Matrix (28), as shown in Table 2.

$$\begin{bmatrix} 1 & 0 & 0 \\ 0 & G_1+sC_1 & G_2 \\ 0 & -G_3 & sC_2 \end{bmatrix} \tag{27}$$

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 \\ 0 & 0 & G_1+sC_1 & G_2 \\ 0 & 0 & -G_3 & sC_2 \end{bmatrix} \tag{28}$$

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & \infty_3 & -\infty_2 & -\infty_3 & 0 \\ 0 & 0 & -\infty_4 & sC_2 & 0 & 0 & \infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \tag{29}$$

Table 2. Four cases of expanding NAM Type-B.

NAM Type-B (Case 1)

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & \infty_3 & -\infty_2 & -\infty_3 & 0 \\ 0 & 0 & -\infty_4 & sC_2 & 0 & 0 & \infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix}$$

NAM Type-B (Case 2)

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & \infty_3 & -\infty_2 & -\infty_3 & 0 \\ 0 & 0 & -\infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & \infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix}$$

NAM Type-B (Case 3)

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & \infty_3 & \infty_2 & -\infty_3 & 0 \\ 0 & 0 & -\infty_4 & sC_2 & 0 & 0 & \infty_4 \\ 0 & 0 & \infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix}$$

NAM Type-B (Case 4)

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & \infty_3 & \infty_2 & -\infty_3 & 0 \\ 0 & 0 & -\infty_4 & sC_2 & 0 & 0 & -\infty_4 \\ 0 & 0 & \infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & \infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix}$$

In (29), the DDCC(1), DDCC(2) and DDCC(3) are represented by terms $\pm\infty_2$, $\pm\infty_3$ and $\pm\infty_4$, respectively. The terminal-X of DDCC(1) can be node 5, terminal-Y_1 and terminal-Z (minus type) are connected to node 3. For the DDCC(2), terminal-X is connected to node 6, terminal-Y_1 is connected to node 4 and terminal-Z (minus type) is connected to node 3. For the DDCC(3), the terminal-X is connected to node 7, terminal-Y_1 is connected to node 3 and terminal-Z (plus type) is connected to node 4. All of the terminal-Y_2 and terminal-Y_3 of DDCC(1), DDCC(2) and DDCC(3) can be used to inject the input voltage source.

Applying Step 4, term $-sC_1$ will be created in position (2,1) of (27) by injecting the input voltage source to terminal-Y_2 of the DDCC(1), then a highpass function at V_{out1} and bandpass function at V_{out2} can be obtained. This operation corresponds to the insertion of the term $\pm\infty_2$ to the second column of (29), as shown in (30). The obtained filter represented by (30) is shown in Figure 6a with nodes V_{in2}, V_{in3}, V_{in4}, V_{in5} and V_{in6} being grounded.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\infty_2 & G_1+\infty_2 & \infty_3 & -\infty_2 & -\infty_3 & 0 \\ 0 & 0 & -\infty_4 & sC_2 & 0 & 0 & \infty_4 \\ 0 & \infty_2 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \quad (30)$$

By injecting the input voltage source to terminal-Y_3 of DDCC(1), the admittance matrix is shown in (31) and the obtained transfer functions at node V_{out1} and V_{out2} are identical to that obtained in (30) with reverse signs. The obtained circuit is shown in Figure 6a, moving the injected voltage source equivalent circuit to node V_{in2} and grounding nodes V_{in1}, V_{in3}, V_{in4}, V_{in5} and V_{in6}.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & \infty_2 & G_1+\infty_2 & \infty_3 & -\infty_2 & -\infty_3 & 0 \\ 0 & 0 & -\infty_4 & sC_2 & 0 & 0 & \infty_4 \\ 0 & -\infty_2 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \quad (31)$$

Also, by applying the input voltage source to terminal-Y_2 of DDCC(2), a bandpass function at V_{out1} and a lowpass function at V_{out2} can be obtained. This is equivalent to the inserting of term $\pm\infty_3$ to the second column of (29), as shown in (32). The obtained filter is shown in Figure 6a, moving the injected voltage source equivalent circuit to node V_{in3} and grounding nodes V_{in1}, V_{in2}, V_{in4}, V_{in5} and V_{in6}.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\infty_3 & G_1+\infty_2 & \infty_3 & -\infty_2 & -\infty_3 & 0 \\ 0 & 0 & -\infty_4 & sC_2 & 0 & 0 & \infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & \infty_3 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \quad (32)$$

Injecting the input voltage source to terminal-Y_3 of DDCC(2), the obtained transfer functions at nodes V_{out1} and V_{out2} are identical to that obtained in (32) but with different signs, as shown in (33). The derived filter is shown in Figure 6a by moving the injected voltage source equivalent circuit to node V_{in4} with grounding nodes V_{in1}, V_{in2}, V_{in3}, V_{in5} and V_{in6}.

Besides, a lowpass function at V_{out1} can be achieved by applying the input voltage source to terminal-Y_2 of DDCC(3). This operation corresponds to the inserting of terms ∞_4 to the second column of (29), as given in (34). The obtained circuit is shown in Figure 6a by moving the injected voltage source equivalent circuit to node V_{in5} and grounding nodes V_{in1}, V_{in2}, V_{in3}, V_{in4} and V_{in6}.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & \infty_3 & G_1+\infty_2 & \infty_3 & -\infty_2 & -\infty_3 & 0 \\ 0 & 0 & -\infty_4 & sC_2 & 0 & 0 & \infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & -\infty_3 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & 0 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \quad (33)$$

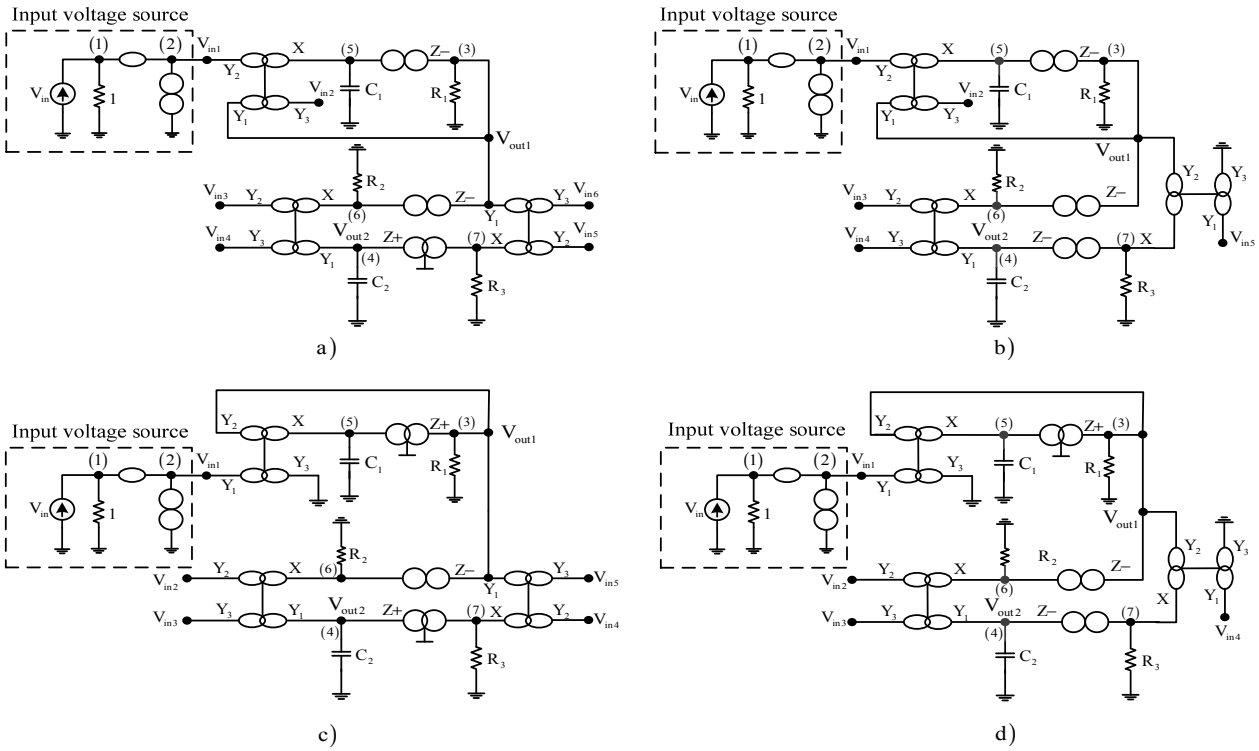

Figure 6. The pathological representations of type-B filters.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & \infty_3 & -\infty_2 & -\infty_3 & 0 \\ 0 & \infty_4 & -\infty_4 & sC_2 & 0 & 0 & \infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & \infty_4 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \quad (34)$$

Injecting the input voltage source to terminal-Y_3 of DDCC(3), the obtained transfer function at node V_{out1} is identical to the circuit represented by (34) with reverse signs. The obtained matrix is shown in (35) and the circuit is shown in Figure 6a by moving the injected voltage source equivalent circuit to node V_{in6} with grounding nodes V_{in1}, V_{in2}, V_{in3}, V_{in4} and V_{in5} grounded.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & \infty_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_1+\infty_2 & \infty_3 & -\infty_2 & -\infty_3 & 0 \\ 0 & -\infty_4 & -\infty_4 & sC_2 & 0 & 0 & \infty_4 \\ 0 & 0 & -\infty_2 & 0 & sC_1+\infty_2 & 0 & 0 \\ 0 & 0 & 0 & -\infty_3 & 0 & G_2+\infty_3 & 0 \\ 0 & -\infty_4 & -\infty_4 & 0 & 0 & 0 & G_3+\infty_4 \end{bmatrix} \quad (35)$$

Different type-B filter functions at V_{out1} and V_{out2} can be obtained by using similar method as mentioned in Section 3.1. The notch function at V_{out1} can be achieved by injecting the input voltage

source to terminal-Y_2 of DDCC(1) and terminal-Y_2 of DDCC(3). The obtained filter is shown in Figure 6a by moving the injected voltage source equivalent circuit to the merged node of V_{in1} and V_{in5} and grounding nodes V_{in2}, V_{in3}, V_{in4} and V_{in6}. Another notch function at V_{out1} in Figure 6a can be also obtained by injecting the input voltage source to the merged node of V_{in2} and V_{in6} with nodes V_{in1}, V_{in3}, V_{in4} and V_{in5} being grounded. Similarly, an allpass function at V_{out1} (with $G_2 = G_1$) can be achieved by injecting the input voltage source to terminal-Y_2 of DDCC(1), terminal-Y_3 of DDCC(2) and terminal-Y_2 of DDCC(3). The obtained circuit is shown in Figure 6a by moving the injected voltage source equivalent circuit to the merged node of V_{in1}, V_{in4} and V_{in5} and grounding nodes V_{in2}, V_{in3} and V_{in6}. Another allpass function at V_{out1} can be also obtained by injecting the input voltage source to the merged node of V_{in2}, V_{in3} and V_{in6} in Figure 6a with nodes V_{in1}, V_{in4} and V_{in5} being grounded.

In the same way, the above synthesized procedure can be applied to other matrices in Table 2. Four equivalent circuits of synthesized filters are shown in Figure 6. The transfer functions of the synthesized circuit for the case 1 of Table 2 are given by (36) and (37). Figure 7 shows the practical configurations realizing the pathological equivalents in Figure 6. Table 3 shows the comparison of obtained filters using the proposed method and related systematic synthesis approaches [16,17,19,21]. It clarifies the benefits of the proposed method.

$$V_{out1} = \frac{s^2C_1C_2V_{in1} - s^2C_1C_2V_{in2} + sC_2G_2V_{in3} - sC_2G_2V_{in4} + G_2G_3V_{in5} - G_2G_3V_{in6}}{s^2C_1C_2 + sC_2G_1 + G_2G_3} \tag{36}$$

$$V_{out2} = \frac{sC_1G_3V_{in1} - sC_1G_3V_{in2} + G_2G_3V_{in3} - G_2G_3V_{in4} - G_3(G_1 + sC_1)V_{in5} + G_3(G_1 + sC_1)V_{in6}}{s^2C_1C_2 + sC_2G_1 + G_2G_3} \tag{37}$$

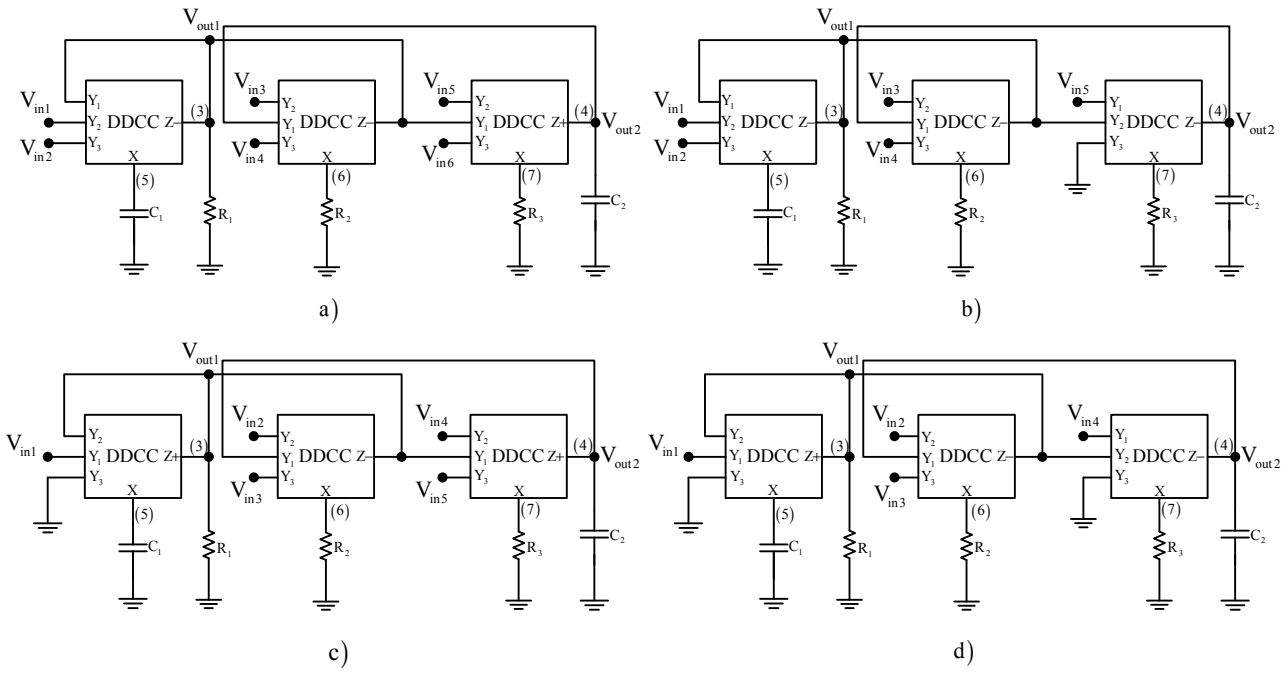

Figure 7. The practical configuration of type-B filters.

Table 3. Comparison of the obtained filter of related works.

Related work	Operating mode	Filter type	Using grounded capacitors	Number of active elements	Cascadable property
[16]	Current	Universal	Yes	4	Yes
[17]	Transimpedance	Single function	No	1 or 2	Yes
[19]	Voltage	Notch	No	3	No
[21]	Voltage	Lowpass and bandpass	Yes	2	Yes
This work	Voltage	Universal	Yes	3	Yes

3.3. Non-Ideal Effect of Active Elements

Taking into account the non-idealities of DDCCs, the relationship of the terminal voltages and currents is given as

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{bmatrix} = \begin{bmatrix} \alpha_{k1} & -\alpha_{k2} & \alpha_{k3} & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm\beta_k \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{bmatrix} \tag{38}$$

where α_{k1} , α_{k2} and α_{k3} respectively denote the voltage tracking errors from V_{Y1} to V_X, V_{Y2} to V_X, and V_{Y3} to V_X of the *k*th DDCC; and β_k denotes the current tracking error of the *k*th DDCC. The denominator of non-ideal transfer function of all obtained filters can be expressed by (39).

$$D(s) = \alpha_{1i}\beta_1 s^2 C_1 C_2 + sC_2 G_1 + \alpha_{2j}\alpha_{3k}\beta_2\beta_3 G_2 G_3 \tag{39}$$

where *i, j, k* = 1–2. The pole frequency ω_0 and the Q factor are expressed by (40) and (41), respectively. The active and passive sensitivities of ω_0 and Q of all obtained filters are shown in (42). It can be seen that all active and passive sensitivities are small.

$$\omega_0 = \sqrt{\frac{\alpha_{2j}\alpha_{3k}\beta_2\beta_3 G_2 G_3}{\alpha_{1i}\beta_1 C_1 C_2}} \tag{40}$$

$$Q = \frac{1}{G_1}\sqrt{\frac{\alpha_{1i}\alpha_{2j}\alpha_{3k}\beta_1\beta_2\beta_3 C_1 G_2 G_3}{C_2}} \tag{41}$$

$$\begin{aligned} &S_{G_2,G_3}^{\omega_0} = -S_{C_1,C_2}^{\omega_0} = S_{C_1,G_2,G_3}^{Q} = -S_{C_2}^{Q} = \frac{1}{2}; \\ &S_{G_1}^{Q} = -1; S_{\beta_2,\beta_3}^{\omega_0} = S_{\beta_1,\beta_2,\beta_3}^{Q} = \frac{1}{2}; S_{\beta_1}^{\omega_0} = -\frac{1}{2}; \\ &S_{\alpha_{2j},\alpha_{3k}}^{\omega_0} = S_{\alpha_{1i},\alpha_{2j},\alpha_{3k}}^{Q} = \frac{1}{2}; S_{\alpha_{1i}}^{\omega_0} = -\frac{1}{2}; \end{aligned} \tag{42}$$

4. Simulation Results

To verify the workability of the proposed method, HSPICE simulations using TSMC 0.35 μm process parameters were performed for two of the obtained type-A and type-B filters. The CMOS implementation of the DDCC shown in Figure 8 was used for the simulations [27]. The aspect ratios of each NMOS and PMOS transistor are (W/L = 5 μm/1 μm) and (W/L = 10 μm/1 μm), respectively. The supply voltages of DDCC are $V_{DD} = -V_{SS} = 1.65$ V with the biasing voltages $V_B = -V_{B1} = 0.76$ V.

We simulated the filters in Figure 5f (type-A) and Figure 7b (type-B) for illustration. The values of capacitors are chosen as $C_1 = C_2 = 10$ pF for all simulations. The values of resistors are given by $R_1 = 11.26$ kΩ and $R_2 = R_3 = 15.92$ kΩ for the simulations of lowpass, bandpass and highpass filters. Figure 9 and Figure 10 show the lowpass and bandpass responses at V_{out1} and V_{out2} of the filter in Figure 5f with node V_{in3} as input node and nodes V_{in1}, V_{in2}, and V_{in4} being ground node. The frequency responses of highpass output in Figure 5f with node V_{in1} as input node and nodes V_{in2}, V_{in3}, and V_{in4} being grounded is shown in Figure 11. Figure 12 shows the notch responses at V_{out1} of the circuit in Figure 7b, with the merged node of V_{in1} and V_{in5} as input node and nodes V_{in2}, V_{in3} and V_{in4} being ground node, and $R_1 = 79.62$ kΩ, $R_2 = R_2 = R_3 = 15.92$ kΩ. Figure 13 represents the frequency responses of the allpass function in Figure 7b with the merged node of V_{in1}, V_{in4}, and V_{in5} as input node and V_{in2} and V_{in3} grounded. The $R_1 = R_2 = 11.26$ kΩ and $R_3 = 22.52$ kΩ is used. All the simulated results are consistent with our theoretical prediction. The workability of the synthesized filters is verified.

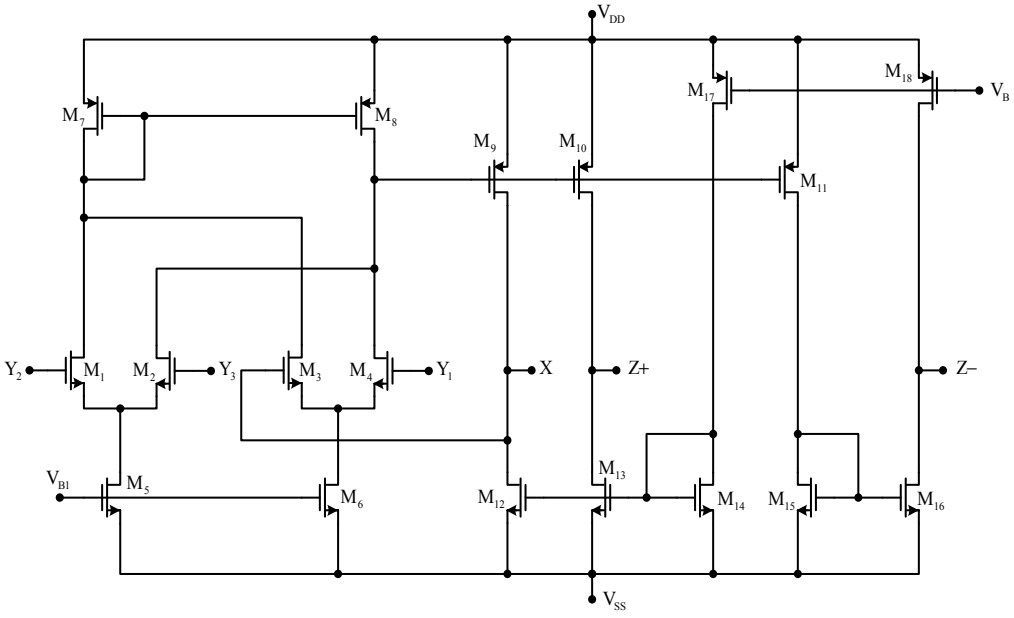

Figure 8. The CMOS circuit of DDCC [27].

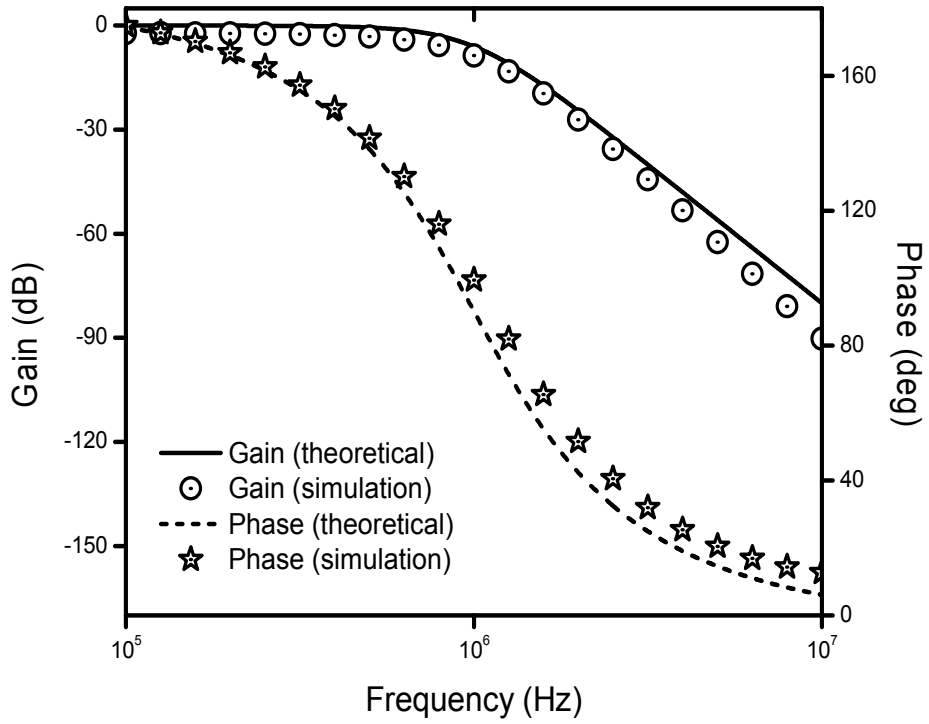

Figure 9. Frequency responses of the lowpass function in Figure 5f.

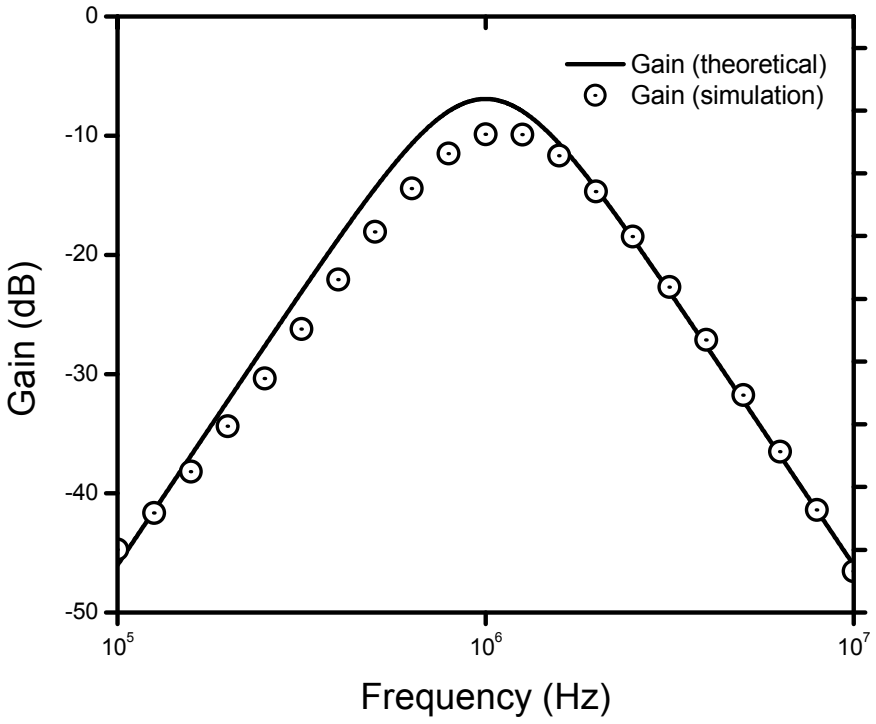

Figure 10. Frequency responses of the bandpass function in Figure 5f.

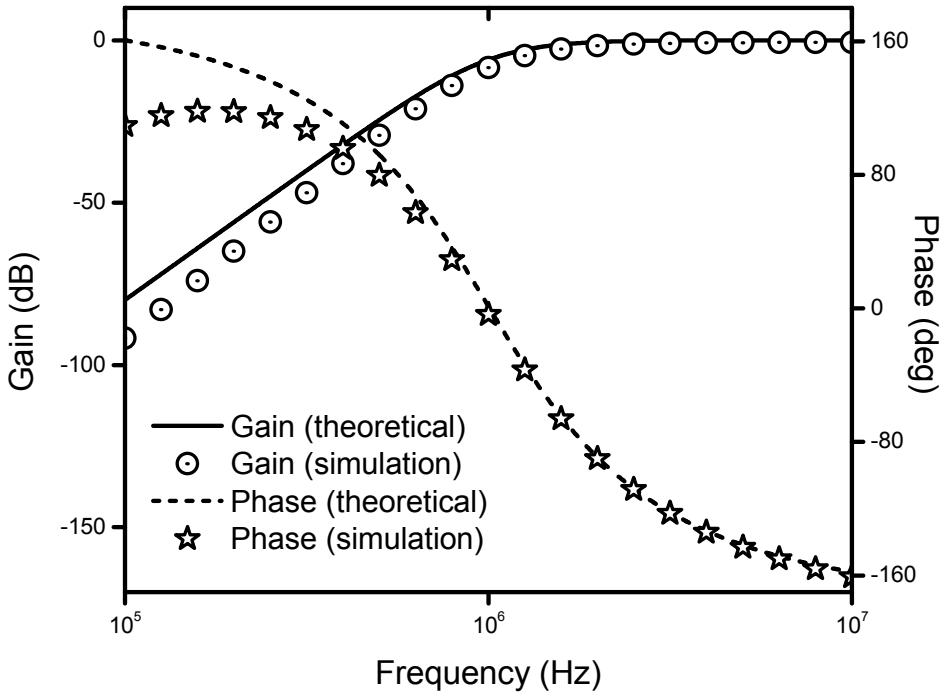

Figure 11. Frequency responses of the highpass function in Figure 5f.

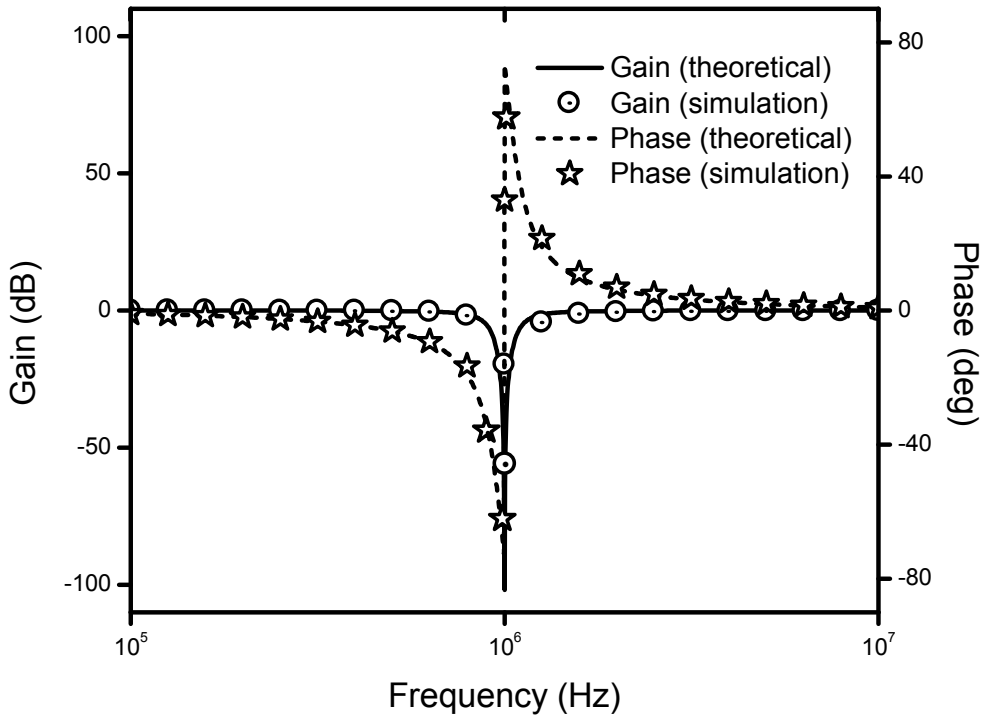

Figure 12. Frequency responses of the notch function in Figure 7b.

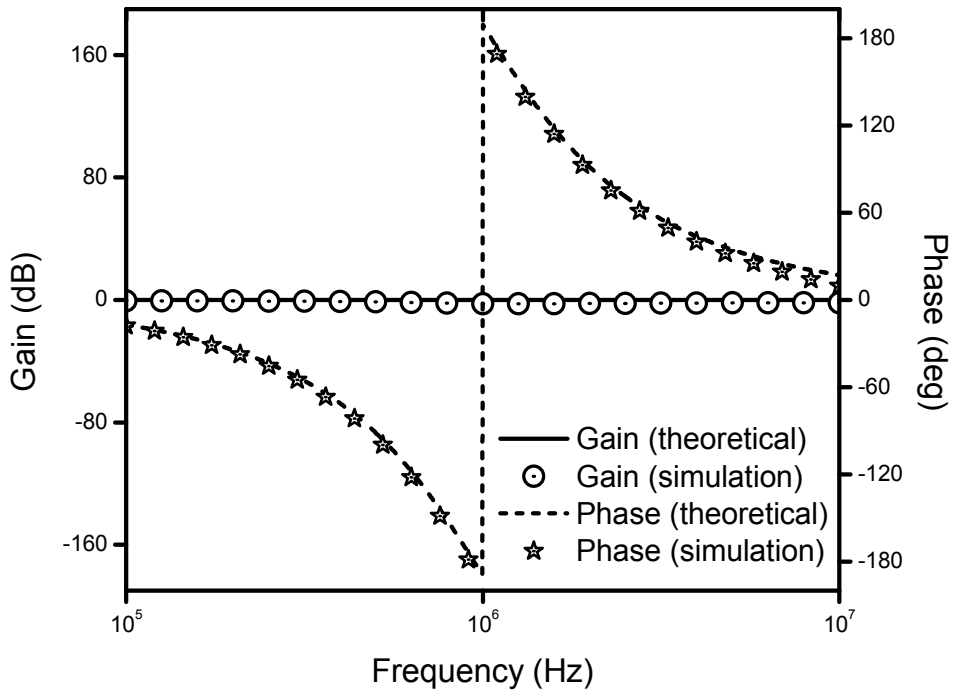

Figure 13. Frequency responses of the allpass function in Figure 7b.

5. Conclusions

Based on the infinity-variables notation of the DDCC and NAM expansion technique, a systematic method for synthesis of voltage-mode DDCC-based universal biquadratic filters is proposed. The obtained filters with two outputs can realize all five generic filter functions. They have the properties of high-input impedance, employing only grounded capacitors and resistors, orthogonal controllability between pole frequency and quality factor, and low active and passive sensitivities. HSPICE simulated results show the workability of the synthesized circuits, and the feasibility of the proposed approach is confirmed.

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Author Contributions

Huu-Duy Tran and Quoc-Minh Nguyen conceived and designed the theoretical verifications; the optimization ideas were provided by Min-Chuan Lin; Hung-Yu Wang and Huu-Duy Tran analyzed the results and wrote the paper.

Conflicts of Interest

The authors declare no conflict of interest.

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