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Graphene transistors with ultrahigh-κ gate oxide

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To my Parents…

Abstract

For a decade, being at the centre of interest in different research disciplines, graphene has already made its profound place in some of these disciplines, particularly in electronics. Graphene is the first truly two-dimensional material being realised theoretically as well as experimentally. Having very high mobility at room temperature and being just single atom thick, along with ambipolar nature and strong field effect, it has gained much attention for electronics applications. But still, absence of a band gap has restricted its use in logic devices. Nevertheless, high frequency devices using graphene as channel material, have already been demonstrated with competitive results to current best MOSFET devices. Keeping in mind the current scaling problem faced by Si CMOS technology, and to push further the performance of graphene transistors, in this thesis different high-κ materials were examined, as a candidate gate dielectric. Particular attention was given to those oxides which are not possible to use in Si CMOS, due to band mismatch. Ultimately much work was done for strontium titanate (STO) based devices during this thesis work.

This thesis work focuses on realisation and characterisation of graphene transistors using ultrahigh-κ gate oxide. Different samples were realised using epitaxially grown STO as gate oxide and CVD grown graphene as channel material. Various graphene-based field effect transistors (GFETs) were fabricated: starting from simple back gated GFETs and then using them as building block for graphene inverters. It was found that electrical performance of the GFETs do vary significantly from sample to sample based on graphene microstructure. As well as due to dielectric charging, persistent hysteresis was observed in all the devices. It was also noticed that the electron mobility was lower than hole mobility in all the fabricated GFETs, which can only be happened due to effect from dielectric, as graphene has symmetric band structure. In any case, results obtained can serve as a starting point for realisation of GFETs with ultrahigh-κ materials, to reach higher performance in graphene devices which currently lagging behind the dominant Si CMOS technology.

Keywords: Graphene; Strontium titanate; Field effect; Ultrahigh-κ; Chemical vapor deposition; Nanofabrication

Estratto

Da più di una decade il grafene è al centro degli studi di diverse discipline e tra queste un'attenzione particolare è stata rivolta al campo dell'elettronica. Il grafene è stato il primo materiale bidimensionale ad essere stato isolato e studiato sia dal punto di vista teorico che sperimentale. Grazie alla sua altissima mobilità a temperatura ambiente, al suo spessore monoatomico oltre che alla sua natura ambipolare, ha catturato l'attenzione per diverse applicazioni elettroniche. D'altra parte, però, l'assenza di un band – gap rende il suo uso nei dispositivi logici difficoltoso. Comunque, dispositivi utilizzanti grafene come materiale attivo e funzionanti ad alta frequenza, sono stati dimostrati con risultati comparabili a quelli dei tradizionali MOSFET. Tenendo a mente le problematiche di scaling che si riscontrano oggi nella tecnologia CMOS basata su silicio e cercando di spingere oltre le performance dei transistor in grafene, differenti materiali con alta costante dielettrica sono stati analizzati in questa tesi come possibili candidati per l'ossido di gate. Un'attenzione particolare è stata data a quegli ossidi che non possono essere utilizzati con il silicio a causa del mismatch tra le bande. Molto del lavoro qui descritto è stato svolto con titanato di stronzio (STO).

Questo lavoro di tesi si focalizza sulla fabbricazione e caratterizzazione di transistor in grafene utilizzando ossidi di gate ad alta costante dielettrica. Sono stati realizzati campioni differenti con STO cresciuto epitassialmente e grafene cresciuto tramite deposizione chimica da fase vapore (CVD). Differenti tipologie di transistor in grafene (GFETs) e piccoli circuiti integrati sono stati fabbricati. Si è dimostrato che le performance elettriche dei GFETs variano significativamente da campione a campione a seconda della microstruttura del grafene utilizzato. Allo stesso modo, un'isteresi persistente nelle misure elettriche è da imputare al caricamento del materiale dielettrico. Inoltre in tutti i campioni fabbricati la mobilità degli elettroni è minore di quella delle lacune, fattore imputabile alla tipologia di dielettrico utilizzato dato che il grafene ha una dipendenza lineare delle bande energetiche. In ogni caso i risultati ottenuti sono un punto di partenza per la realizzazione id GFETs con materiali ad altissima costante dielettrica per il raggiungimento di performance che possano competere con l'attualmente dominante tecnologia CMOS in silicio.

Keywords: Grafene; Titanato di stronzio; Effetto di campo; Ultrahigh-κ; Deposizione chimica da fase vapore; Nanofabbricazione

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List of symbols

a	Lattice constant
a_1, a_2	Lattice vectors
A	Capacitor area
A_V	Voltage gain
b_1, b_2	Reciprocal-lattice vectors
c	Speed of light
C	Optical contrast
C_g	Gate capacitance per unit area
C_{GD}	Gate-drain capacitance
C_{GS}	Gate-source capacitance
d_1, d_2	Thickness of graphene and SiO_2 layer respectively
E	Energy of charge carriers
E_F	Fermi energy
E_G	Energy band gap
f_T	Cut-off frequency
f_{max}	Maximum frequency of oscillation
g_m	Transconductance
g_{ds}	Drain conductance
G_{int}	Intrinsic gain
I	Light intensity
I_D	Drain current
I_{off}	Off-current
I_{on}	On-current
k, k_x, k_y	Wave vector components for charge carriers
K, K’	Dirac points
L	Gate channel length
n	Refractive index
p	Momentum of charge carriers
r	Relative indices of refraction
R_{Ch}	Gate channel resistance
R_D	Drain resistance
R_S	Source resistance
t	Dialectic thickness
v_f	Fermi velocity of charge carriers
V_{BG}	Breakdown voltage of dielectric material
V_{ch}	Gate channel potential
V_D	Drain voltage
V_{DD}	Drain-drain voltage
V_{DS}	Drain-source voltage
V_G	Gate voltage
V_{Gch}	Gate-channel voltage

V_{GD} Gate-drain voltage
V_{GS} Gate-source voltage
V_{IN} Input voltage for graphene inverter
V_{OUT} Output voltage from graphene inverter
V_S Source voltage
V_{th} Threshold voltage
$q_{\parallel}$, $q_{\perp}$ Reciprocal scattering vector components
Q Accumulated charge
W Gate channel width
x Distance from source in gate channel
ε_0 Vacuum permittivity
κ Relative dielectric constants
μ_{FE} Field-effect mobility of charge carriers
ρ Density of states for charge carriers
σ Surface charge density
λ Wave length
2ϑ Scattering angle
ω Incident angle
φ Optical path shift

List of abbreviations

2D	Two dimensional
AFM	Atomic force microscopy
BZ	Brillouin zone
CAD	Computer aided design
CMOS	Complementary metal–oxide semiconductor
CVD	Chemical vapour deposition
DOS	Density of state
EBL	Electron beam lithography
FET	Field effect transistor
FOM	Figure of merit
GFET	Graphene field effect transistor
HOPG	Highly oriented pyrolytic graphite
LSMO	Lanthanum strontium manganite
MOSFET	Metal–oxide–semiconductor field effect transistor
NEP	N-ethyl-2-pyrrolidone
PLD	Pulsed laser deposition
RF	Radiofrequency
RHEED	Reflection high-energy electron diffraction
RIE	Reactive ion etching
RMS	Root mean square
PMMA	Poly methyl methacrylate
SEM	Scanning electron microscopy
SMU	Source measurement unit
STO	Strontium titanate
XRD	X-ray diffraction

1 Introduction

1.1 Graphene

Electronic properties

1.3 Electric field effect in graphene

Optical visibility

1.5 Graphene production

1.5.1 Micromechanical cleavage

1.5.2 Liquid-phase exfoliation

1.5.3 Epitaxial growth

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1.6 High-κ materials

1.6.1 Possible high-κ materials for GFETs

1 Introduction

Technological evolution and progress is always being marked by breakthrough in development of materials. Historically humans have always explored nature to get new materials, which can be used directly or by some modifications, to make their life more comfortable and productive. Modern civilization, who is more and more technology dependent, demands next generation of devices - which are smart, advanced, flexible and at the same time do not waste energy, have low power consumption, and are environment friendly. Most of the materials may have one or maybe two of the properties needed for such futuristic applications, while for a material to be truly revolutionary it needs to comprise many of these properties. In recent years a new class of materials that can fulfil these needs have emerged: two-dimensional (2D) materials. Graphene is probably the most famous example for such kind of materials with amazing electronic and structural properties.

Graphene as the building block for a new technological area will be reviewed in this chapter. In section 1.1, overview of graphene and its properties are presented. In section 1.2, a brief description of the band structure and carrier transport in graphene is reported. One of the important properties of graphene for electronics, electrical field effect, is described in section 1.3. A quick theoretical check for its visibility over different substrates is described in section 1.4. And in section 1.5, different methods used to produce graphene are discussed. At last a brief introduction to high-κ materials is reported in section 1.6.

1.1 Graphene

As such graphene is not a new material, if we look in history first notable mentioning of graphene was by chemist B. C. Brodie in 1859 where he mentioned suspension of tiny graphene oxide crystals in strong acid as “graphon” [1]. Theoretically graphene is known since late 40’s of last century, when physicist P. R. Wallace had started study on band theory of graphite using simple model of graphene [2]. Although at that time graphene was not practically realised material and was just theoretical model to understand properties of various carbon-based materials. During 1962 U. Hofmann, H. P. Boehm and their group continued to study graphene oxide and reduced

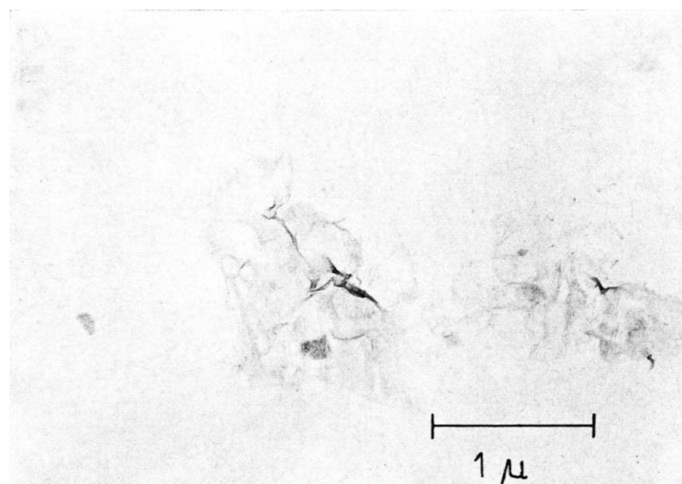

Figure 1.1 TEM image of ultrathin graphitic flakes from the early 1960s. [3]

graphene oxide, and they were first to obtain ultrathin graphitic flakes [3]. Later they give graphene its name, as a combination of the word graphite from crystalline form of carbon and -ene suffix for polycyclic aromatic hydrocarbons [4]. But it was not till 2004, when graphene was rediscovered by A.K Geim and K.S. Novoselov [5-6], the actual gold rush of 2D materials started.

Graphene is a one atom thick 2D honeycomb lattice of carbon atoms, a 2D allotrope of sp2-hybridized carbon. It can be considered as the building block for all sp2-hybridized carbon allotropes, covering a range of dimensionality which can be seen in Figure 1.2. It can be wrapped up into 0D fullerenes, rolled into 1D nanotubes or stacked into 3D graphite. The strong σ bonds are responsible for the mechanical properties and the inertness of the materials, while the π electrons can move freely and give rise to the high electrical conductivity.

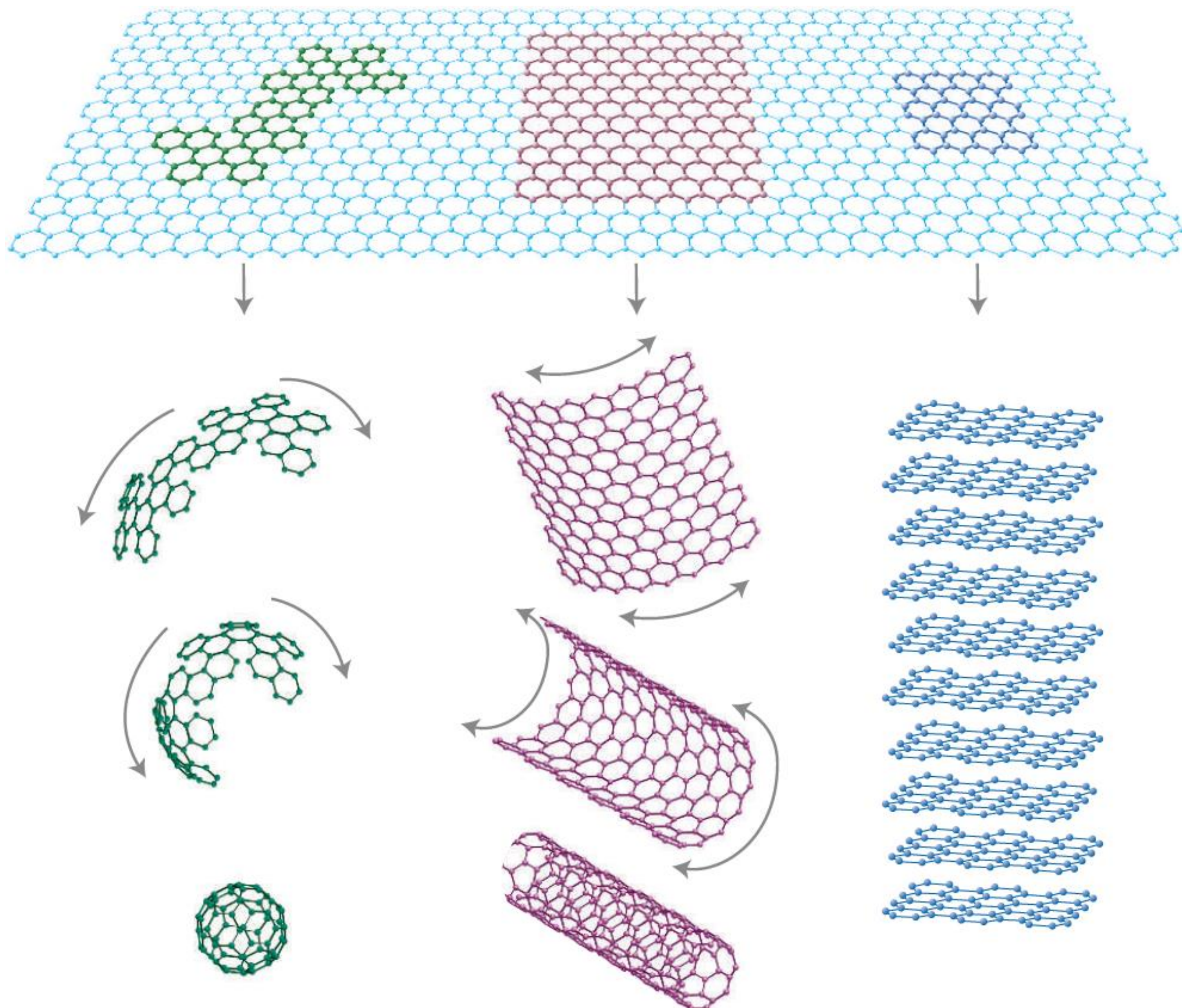

Figure 1.2 Mother of all graphitic forms. Graphene is a 2D building material for carbon materials of all other dimensionalities. It can be wrapped up into 0D fullerenes, rolled into 1D nanotubes or stacked into 3D graphite. [7]

It has been a great topic of debate for long time, whether a strictly 2D crystal could exist at any finite temperature or not. As the melting temperature of thin films decreases rapidly with decrease in thickness, the atomic monolayers can only be observed as part of large 3D structures [8]. However, after experimental discovery of graphene [5] many experiments were done, and it was shown that indeed 2D crystals could be obtained on top of non-crystalline support substrates, in liquid suspensions [5-7] and as suspended membranes [9].

Graphene is considered as extraordinary material, not just because of some extraordinary property it has, but it inhibits many of them – which makes it a multipurpose material. Firstly, it is true 2D material – just one atom thick, but still stable at room temperature. It is the strongest material ever known with Young's modulus of ~1 TPa (between 100-300 times stronger than steel) and at the same time is stretchable up to 25 % [10]. It is the best conductor of heat at room temperature with heat conductivity of ~4.84 ± (0.44) $\times 10^3$ to 5.30 ± (0.48) $\times 10^3$ W/mK [11]. And also the best conductor of electricity, having a mobility exceeding 10^6 cm^2/Vs, which is due to zero effective mass of charge carriers which behave like massless Dirac fermions [12]. It is also almost transparent material with absorption of ~2.3 % of visible light [13]. Even being just single atom layer, it is still impermeable to standard gases including helium [14]. Using many of its properties it can be used for different applications. Some of the possible applications of graphene are shown in Figure 1.3 [15-16].

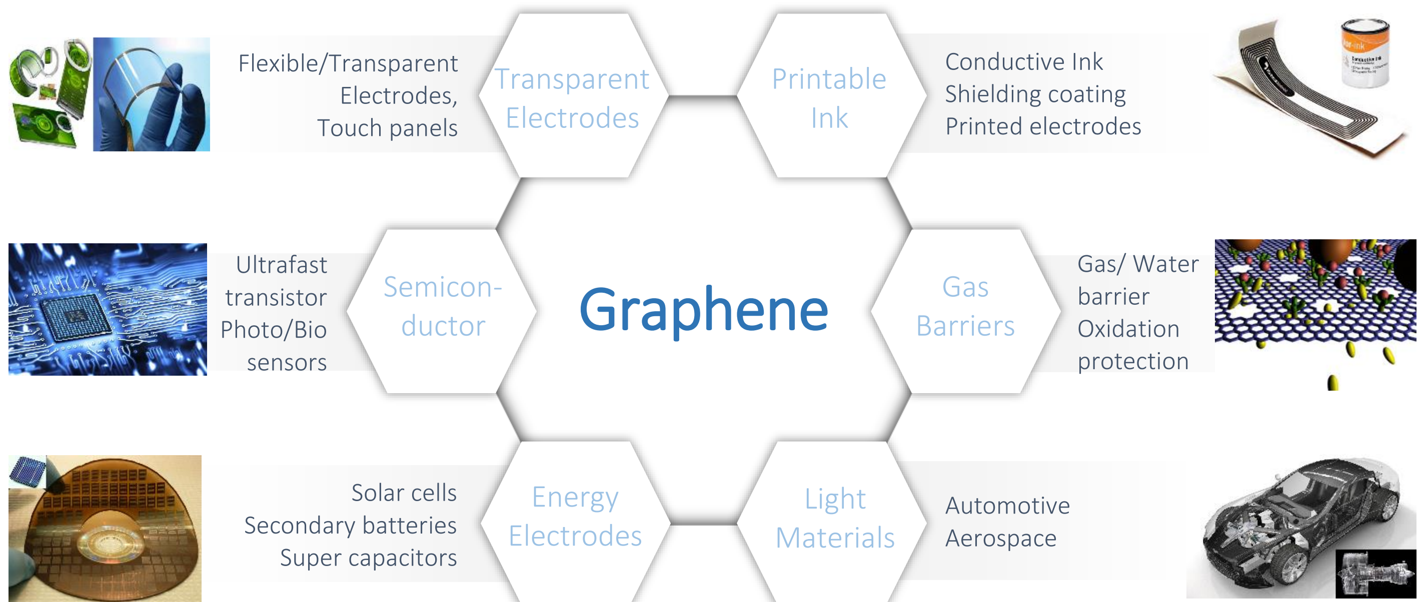

Figure 1.3 Some of the possible application of graphene.

1.2 Electronic properties

Maybe the most significant feature of graphene is, its electronic properties. Graphene is made out of carbon atoms arranged in a honeycomb structure. The sp2 hybridization between one 2s orbital and two 2p orbitals of carbon atoms leads to a trigonal planar structure of graphene, which forms σ bonds between carbon atoms with bond length of 1.42 Å. These bonds are responsible for the robustness of the lattice structure in all allotropes of carbon. Due to the Pauli exclusion principle, bands form by σ bonds are filled and form a deep valence band. The unaffected 2p orbital, which is perpendicular to the planar structure, when the carbon atoms are put close in contact, can bind covalently with neighbouring carbon atoms, leading to the formation of a delocalized π band. Since each p orbital has one extra electron, the π band is half filled, which is the responsible of the electron mobility through the graphene sheet.

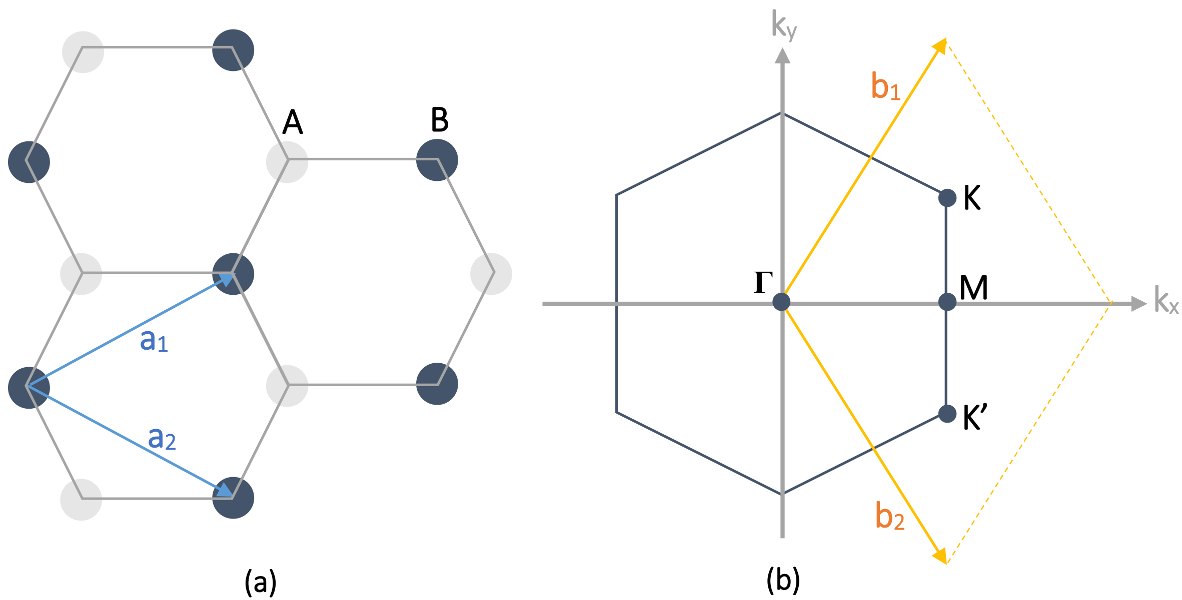

Figure 1.4 Honeycomb lattice and its Brillouin zone. (a) lattice structure of graphene, made out of two interpenetrating triangular lattices (a_1 and a_2 are the lattice unit vectors). (b) corresponding Brillouin zone. [17]

The honeycomb lattice of graphene is not a Bravais lattice, as it is not possible to **have** translation lattice unit vectors for all the nodes of the graphene, however it can be considered as a Bravais lattice, when taking into account a triangular primitive cell with base formed by two atoms separated by a distance a = 1.42 Å, which is the carbon-carbon distance. The lattice vectors can be written as,

$$a_1 = \frac{\mathrm{a}}{2}\left(3, \sqrt{3}\right), a_2 = \frac{\mathrm{a}}{2}\left(3, -\sqrt{3}\right) \tag{1.1}$$

And the reciprocal-lattice vectors are given by,

$$b_1 = \frac{2\pi}{3\mathrm{a}}\left(1, \sqrt{3}\right), b_2 = \frac{2\pi}{3\mathrm{a}}\left(1, -\sqrt{3}\right) \tag{1.2}$$

Figure 1.4 (b) show an illustration of the first Brillouin zone (BZ) based on the construction of the reciprocal lattice. In the BZ it is possible to distinguish some high symmetry points, the Γ and the M points are situated respectively at the centre of the BZ and at the middle of the edges of BZ, whereas the K and K' points (Dirac points) are placed at the six vertices of the BZ [18]. Their positions in momentum space are given by,

$$\mathrm{K} = \left(\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a}\right), \mathrm{K}' = \left(\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a}\right) \tag{1.3}$$

The band structure of single-layer graphene is accurately extracted using a tight-binding approach, considering that electrons can hop to both nearest and next-nearest neighbour atoms and a single π electron per carbon atom [17] [19] [20]. The resultant dispersion relation can be written as,

$$E^{\pm}(k_x, k_y) = \pm\gamma_0 \sqrt{1 + 4\cos\frac{\sqrt{3}k_x a}{2}\cos\frac{k_y a}{2} + 4\cos^2\frac{k_y a}{2}} \tag{1.4}$$

γ_0 is found by fitting experimental data. The most common practice is to adjust the tight-binding dispersion to a correct description of the π bands at the K point, and γ_0 can have value between -2.5 and -3 eV [20]. Figure 1.5 represents dispersion relation for graphene, and in the same figure, a zoom in of the dispersion relation close to one of the Dirac points (K or K' point in the BZ) is shown.

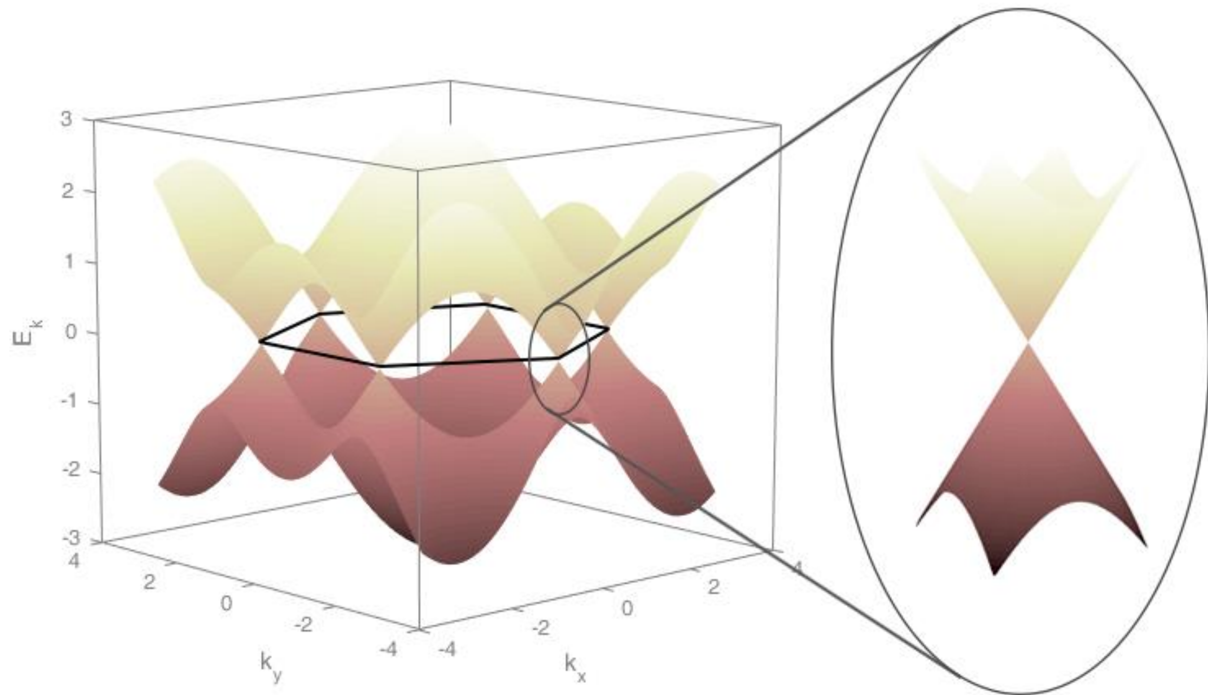

Figure 1.5 Dispersion relation for graphene. Conductance and valence bands meet at the vertices of BZ. Close to these Dirac points, the energy E is linear in momentum (right side zoom in figure).

The Taylor series expansion of the equation 1.4 close to the Dirac point (K or K′), **where the conductance and valence bands meet,** the energy dispersion relation at those points is linear in momentum,

$$E^{\pm}(q) = \pm\hbar v_{\mathrm{f}} q \qquad (1.5)$$

where v_f is the Fermi velocity for the electron, and in graphene it is defined as,

$$v_{\mathrm{f}} = \frac{3}{2}\frac{a\,\gamma_0}{\hbar} \approx 10^6 \left[\frac{m}{s}\right] \approx \frac{c}{300} \qquad (1.6)$$

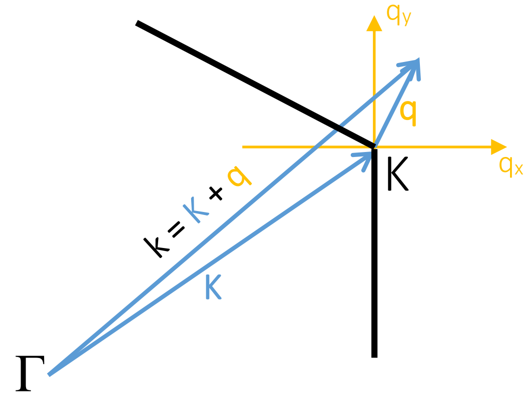

Figure 1.6 Wave vector expansion around the Dirac point.

Where **c** is the speed of light. Equation 1.5 is a good approximation as long as the momentum does not deviate so far from the K or K' point. As shown in Figure 1.5 the effect is the creation of two conic shape bands touching at the Dirac point. Being linear for low energies, it mimics relativistic Dirac particles with zero effective mass. As the dispersion relation of energy is linear with respect to momentum, the definition of effective mass is not applicable to graphene.

$$m^* = \frac{\hbar^2}{\frac{\partial^2 E(k)}{\partial k^2}} \qquad (1.7)$$

Where m^* is the effective mass defined in conventional way in solid-state physics [18], but it may turn out as infinite effective mass for the charge particles in graphene if using this equation. While, as previously mentioned charge particles in graphene can be considered as relativistic Dirac particles, so it is better to use relativistic expression to define the relation between energy and mass of particles. Which can be written as,

$$E = \sqrt{m_0{}^2 c^4 + p^2 c^2} \qquad (1.8)$$

Where m_0 is the rest mass, and p is the crystalline momentum, defined as $p = \hbar k$. When in this equation rest mass taken as zero and considered that fermi velocity is the light velocity in the graphene, it deduced to the equation 1.5. So in this description electron and holes cab be considered as massless Dirac Fermions traveling with a group velocity defined by the Fermi velocity v_f.

Now calculating density of state (DOS) for graphene, limiting the calculation near the Dirac points. Using the equation 1.5 and the number of states available for graphene, DOS for graphene can be written as [17] [18] [21],

$$\rho(E) = \frac{4|E|}{\pi\hbar^2 v_{\mathrm{f}}{}^2} \qquad (1.9)$$

which is linearly dependent on energy, compare to constant DOS for 2D quantum systems. This is because for graphene energy dispersion relation is linear while for 2D quantum systems it has parabolic dependence. DOS for graphene near Dirac points can be represented as shown in Figure 1.7 (b), DOS far from Dirac point has influence of non-linear energy dispersion relationship.

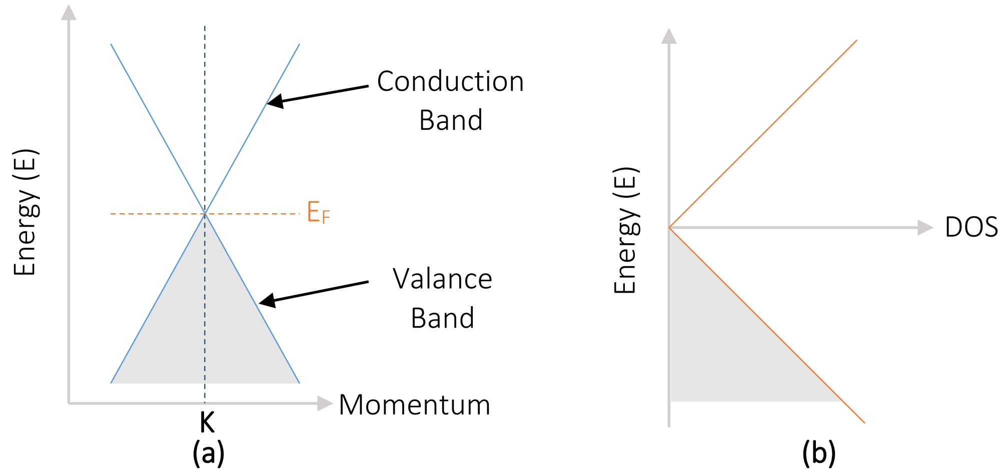

Figure 1.7 Dispersion relation and DOS for graphene near Dirac points. (a) Electronic band structure around Dirac point in graphene. (b) DOS of graphene near Dirac point.

Fermi energy (E_F) for graphene (pristine) is at the energy level where conduction and valance band meet, as shown in figure 1.7 (a) [22]. Which means conduction band is completely empty and valance band is completely filled. Moreover, as it doesn't have any band gap, graphene can be defined as both - semimetal and zero-bandgap semiconductor. And at the fermi energy level (E_F) of graphene density of state is zero, due to unavailability of energy states, which can be seen in Figure 1.7 (b).

1.3 Electric field effect in graphene

One of the main aspect of modern electronics is the field-effect, in which the electronic properties of a material are controlled by an external electric field. This effect is not seen in all materials, particularly conventional metals do not exhibit this effect due to high charge carrier density and screening of the electrical field at very short distance. While semiconductors are the main family of material, which shows good alteration in electrical properties by this effect. On the other hand, for semimetal like graphene, with charge carrier's concentrations as high as 10^{13} cm^{-2} and with mobility exceeding 15,000 $cm^2V^{-1}s^{-1}$ even at ambient conditions, can be tuned continuously between electrons and holes transport [7]. Depending on the bias of the gate voltage, the carrier concentration can be tuned from positive charge carrier - holes to negative charge carrier - electrons, showing the bipolar field effect – which is generally refer as ambipolar electric field effect [5]. Due to this property of graphene, transfer curve (drain current(I_D) vs. gate voltage(V_{GS}) characteristic) of graphene base field effect transistors (GFETs) become a kind of V-shape in nature. This can be seen in the Figure 1.8, which shows a curve of resistivity change with respect to gate voltage of a GFET.

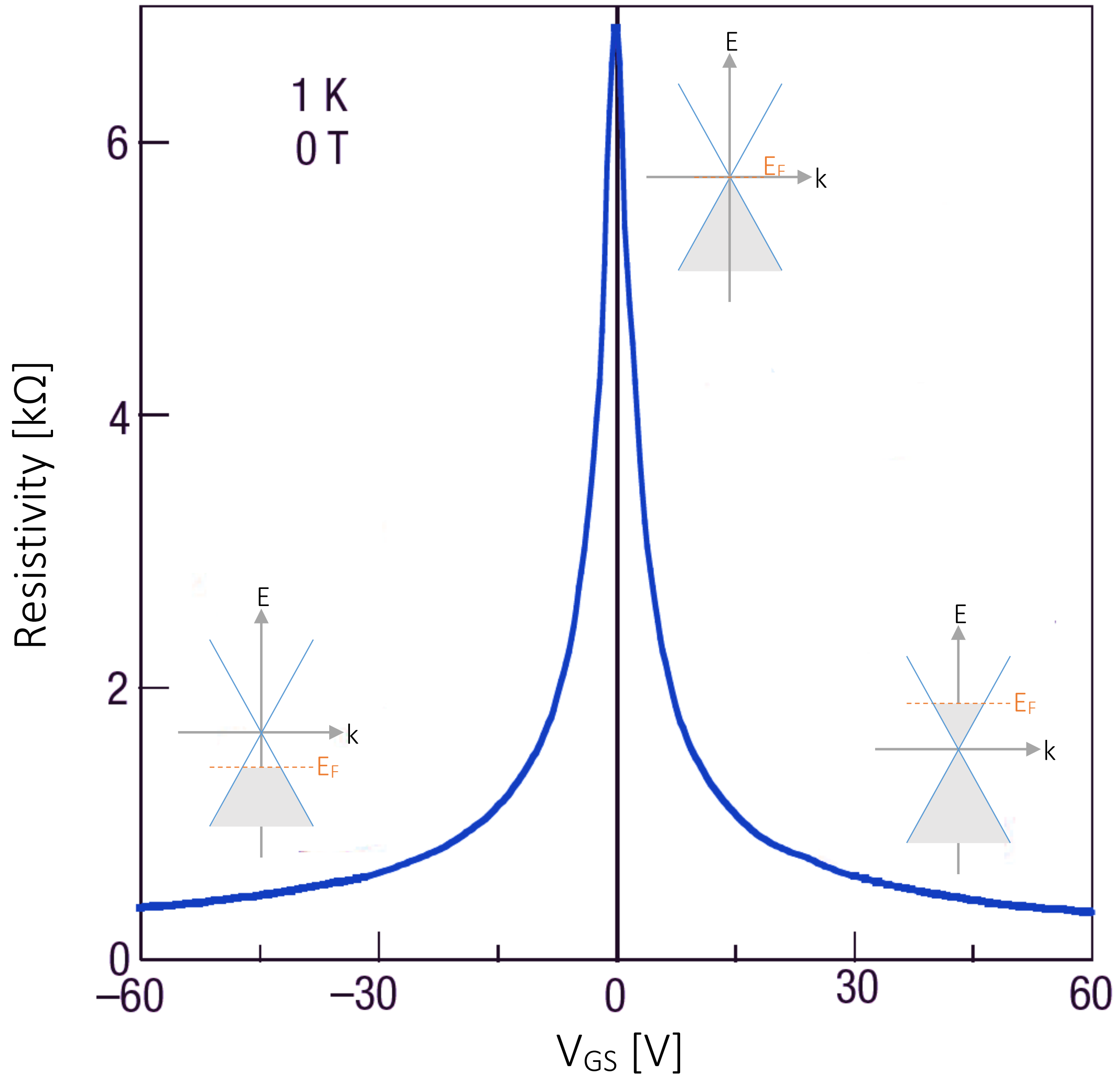

Figure 1.8 Ambipolar electric field effect in single-layer graphene. The insets show its conical low-energy spectrum E(k), indicating changes in the position of the Fermi energy E_F with changing gate voltage V_{GS}. [7]

As it is clear from this Figure 1.8, when negative gate voltage is applied the conduction is supported by holes whereas at positive gate voltage it is due to electrons. The rapid decrease in resistivity with higher gate bias is due to addition of charge carriers and because of their high mobility [7]. This peculiarity of graphene makes it a perfect choice for CMOS applications, as the material can be used to make both; p-type and n-type transistors, instead of the complex stacks of different materials required for classical MOSFETs.

The most frequently stated advantage of graphene to use in electronics is its high carrier mobility at room temperature [22]. If the extrinsic disorder and ripples are eliminated in graphene,

mobilities higher than 200,000 $cm^2V^{-1}s^{-1}$ have been reported [27]. And a mobility of the order of 10^6 $cm^2V^{-1}s^{-1}$ at liquid-helium temperature for suspended graphene has been observed [12]. While for exfoliated graphene on SiO_2 covered silicon wafers mobilities of the order of 10,000 $cm^2V^{-1}s^{-1}$ are measured at room temperature [5]. For large-area graphene grown by chemical vapour deposition (CVD) on nickel or copper and then transferred to a substrate, mobilities greater than 3,700 $cm^2V^{-1}s^{-1}$ have been measured [31]. Due to phonon interaction mobility of charge carriers, do influence a lot. Generally, in semiconductor phonon scattering has more effect on the charge carrier mobility, while in graphene due to very high energy of optical phonon there is no much interaction of it with charge carriers so mobility can be very high for graphene [28] [29]. Moreover, in graphene the mobility has a weak dependence on charge carrier concentration and remaining high even at high charge carrier concentration [7]. In addition to this, due to symmetrical band structure around the Dirac point, electrons and holes should have equal mobility, which is unlike the typical semiconductors where two different values are observed, with holes' mobility being particularly low. The high mobilities mentioned above are relate to large-area graphene, which is gapless. While for graphene nanoribbons mobilities measured are not that high [32] [33], due to rough and damaged edges.

1.4 Optical visibility

Graphene is probably produced every time one uses a pencil, but it is really hard to search for some small graphene crystallites among millions of thicker graphitic flakes deposited on most of the substrates. Graphene absorbs only 2.3 % of visible light [13]. In fact, most of the modern visualization techniques, such as atomic-force, scanning-tunnelling, and electron microscopies, are not useful to find graphene, as they have extremely low throughput at the atomic resolution or lack of capability to distinguishing atomic monolayers from thicker flakes. Even Raman microscopy, which is a powerful tool for distinguishing graphene monolayers, has limitation of very small area of spot to search, so it can't be used to search for graphene crystallites over a large area of substrates.

Till now, the best and most suitable way to identify monolayer graphene is by using an optical microscope. Which is possible as the thin graphene flakes add an optical path due to its transparency, which changes the interference colour with respect to the substrate. During 2004 when graphene was rediscovered [5] by fortunate coincidence, researchers were using Si substrates with a thin layer of silicon dioxide (SiO_2), which had just about the right thickness for graphene to be visible. Now it is possible to design the substrates to maximize the graphene visibility [34]. It is easy to calculate the contrast of graphene deposited on a substrate, which has an opaque base and a thin transparent film on top of it, using a simple optical model [34] [35]. Base on the wavelength of incident light and the oxide thickness, different contrast between graphene and the bare substrate can be observed due to interference between incident and reflected light from the oxide and graphene.

For graphene, on top of Si substrate with thin SiO_2 top layer, contrast can be calculated as described below. Considering opaque Si substrate as semi-infinite with complex refractive index $n_3(\lambda)$, which depend on wavelength of incident light. While the top oxide layer has thickness d_2 and refractive index $n_2(\lambda)$ but with a real part only. Over which single-layer graphene is deposited and it is assumed to have a thickness $d_1 = 0.34$ nm equal to the distance between graphene layers in graphite, and a complex refractive index n_1. Which is assumed to be same as bulk graphite, $n_1 \approx 2.6 - 1.3i$, which is independent of λ. And taking refractive index of air as $n_0 = 1$. For the described geometry (as per Figure 1.9), the reflected light intensity can be written as,

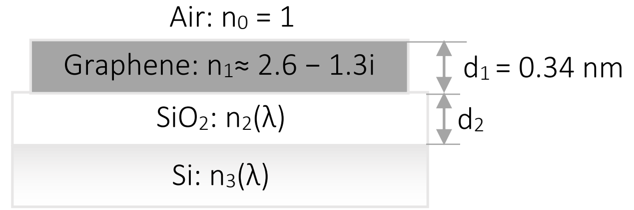

Figure 1.9 Substrate and graphene geometry used for optical analysis.

$$I(\mathrm{n}_1) = \left| \frac{\mathrm{r}_1 e^{i(\varphi_1+\varphi_2)} + \mathrm{r}_2 e^{-i(\varphi_1-\varphi_2)} + \mathrm{r}_3 e^{-i(\varphi_1+\varphi_2)} + \mathrm{r}_1\mathrm{r}_2\mathrm{r}_3 e^{i(\varphi_1-\varphi_2)}}{e^{i(\varphi_1+\varphi_2)} + \mathrm{r}_1\mathrm{r}_2 e^{-i(\varphi_1-\varphi_2)} + \mathrm{r}_1\mathrm{r}_3 e^{-i(\varphi_1+\varphi_2)} + \mathrm{r}_2\mathrm{r}_3 e^{i(\varphi_1-\varphi_2)}} \right|^2 \tag{1.10}$$

Where,

$$\mathrm{r}_1 = \frac{\mathrm{n}_0 - \mathrm{n}_1}{\mathrm{n}_0 + \mathrm{n}_1};\ \mathrm{r}_2 = \frac{\mathrm{n}_1 - \mathrm{n}_2}{\mathrm{n}_1 + \mathrm{n}_2};\ \mathrm{r}_3 = \frac{\mathrm{n}_2 - \mathrm{n}_3}{\mathrm{n}_2 + \mathrm{n}_3} \tag{1.11}$$

are the relative indices of refraction, and phase shifts due to changes in the optical paths are,

$$\varphi_1 = 2\pi\mathrm{n}_1\,\mathrm{d}_1/\lambda\,; and\ \varphi_2 = 2\pi n_2\,\mathrm{d}_2/\lambda \tag{1.12}$$

From this, the contrast can be defined as the relative difference of the intensity of reflected light from the areas with and without graphene, respectively. The intensity of reflected light from areas without graphene can be calculated by taking $n_1 = 1$, as the refractive index of air**.** So contract,

$$C = \frac{I\,(\mathrm{n}_1 = 1) - I\,(\mathrm{n}_1)}{I\,(\mathrm{n}_1 = 1)} \tag{1.13}$$

Thus the contrast for graphene can be optimized, by varying both the wavelength of incident light and the thickness of the oxide layer on the substrate. From the calculation using equations 1.10 to 1.13, contrast plot for graphene on top of SiO_2/Si substrates is shown in Figure 1.10. Using the green light of ∼550 nm wavelength and substrates with ∼90 nm or ∼280 nm of SiO_2 thickness, a contrast around 10 % can be achieved, which is more than twice than what is expected from the pure absorption of graphene. Moreover, changes in the light intensity due to graphene is relatively small, and this allows the observed contrast to be used for measuring the number of graphene layers, as shown by P. Blake et al. [34].

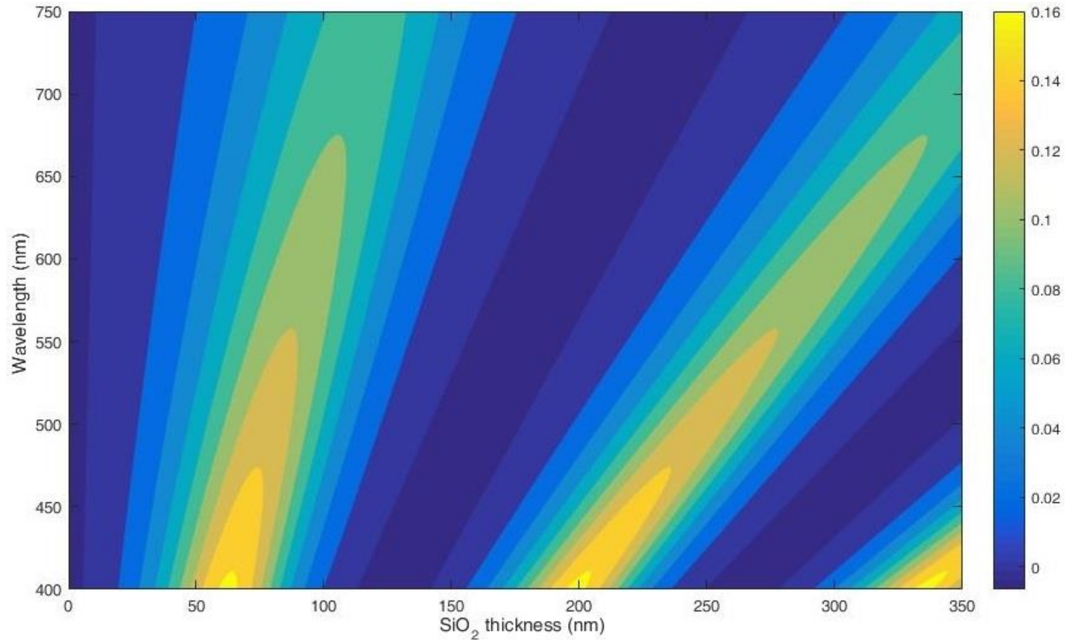

Figure 1.10 Color plot of the optical contrast of graphene on SiO_2/Si substrates as a function of wavelength and SiO_2 thickness. The color scale on right shows the theoretical contrast.

As such SiO_2/Si substrates is the most commonly used substrate for graphene experiments. But in this work we had used different substrate, typically strontium titanate (STO) substrate. Which has the configuration as, STO base substrate with thin layer of lanthanum strontium manganite (LSMO) and then again thin layer of STO. Over which graphene is transferred. For this system also optical

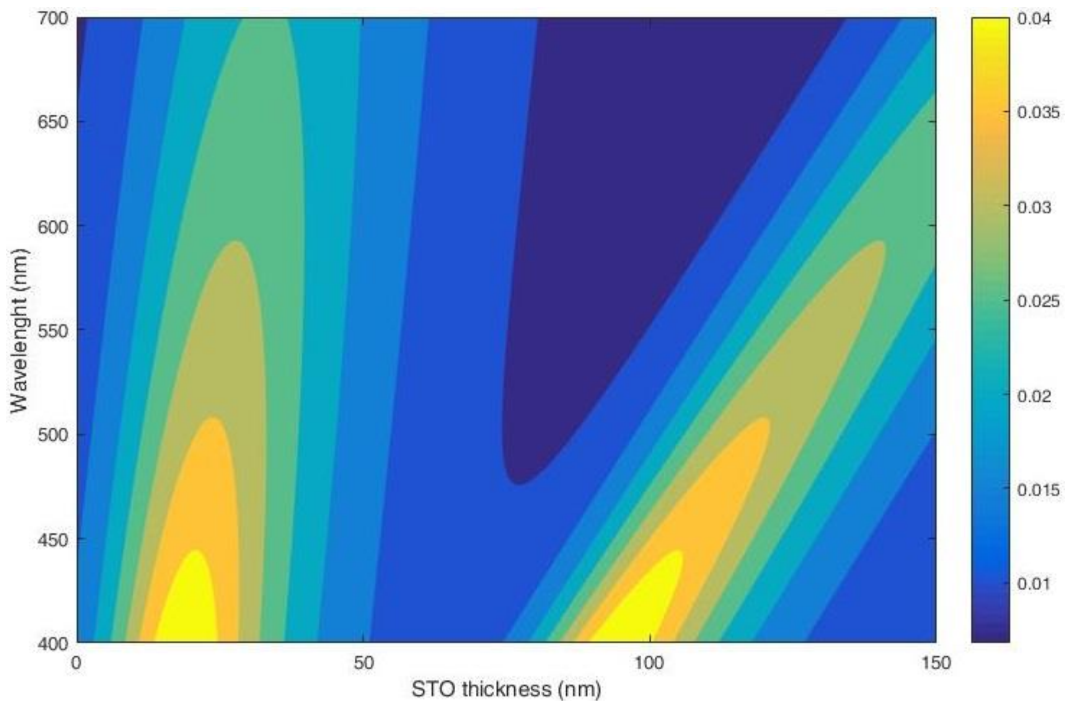

Figure 1.11 Color plot of the optical contrast of graphene on STO substrates as a function of wavelength and STO thin film thickness. The color scale on right shows the theoretical contrast.

contrast of graphene is calculated, as a function of STO thin film thickness and the incident light wavelength. Refractive indices of STO and LSMO were calculated from the literature [36-39]. The theoretical contrast for graphene on this substrate as a function of STO thin film thickness and incident light wavelength is shown in Figure 1.11. The maximum contrast of graphene on this STO substrate ∼3%, which is lower than that on SiO_2/Si substrate, making graphene much more difficult to find on the former substrate. While optical microscopy provides a fast technique to identify graphene, it has to be calibrated against other methods, which provide a direct signature of having a certain number of layers of graphene. Which can be done in various ways, like using AFM [5][7], STM [40] or Raman spectroscopy [41-43] after selecting particular areas of graphene using optical microscopy.

1.5 Graphene production

After successfully demonstrating a game changing method - "scotch tape method", the easiest way to obtain graphene, by A. K. Geim and K. S. Novoselov [5], many other production processes have been exploited. All these methods have their own strengths and limitations; as different techniques give materials with some widespread properties. However, there is always trade-off

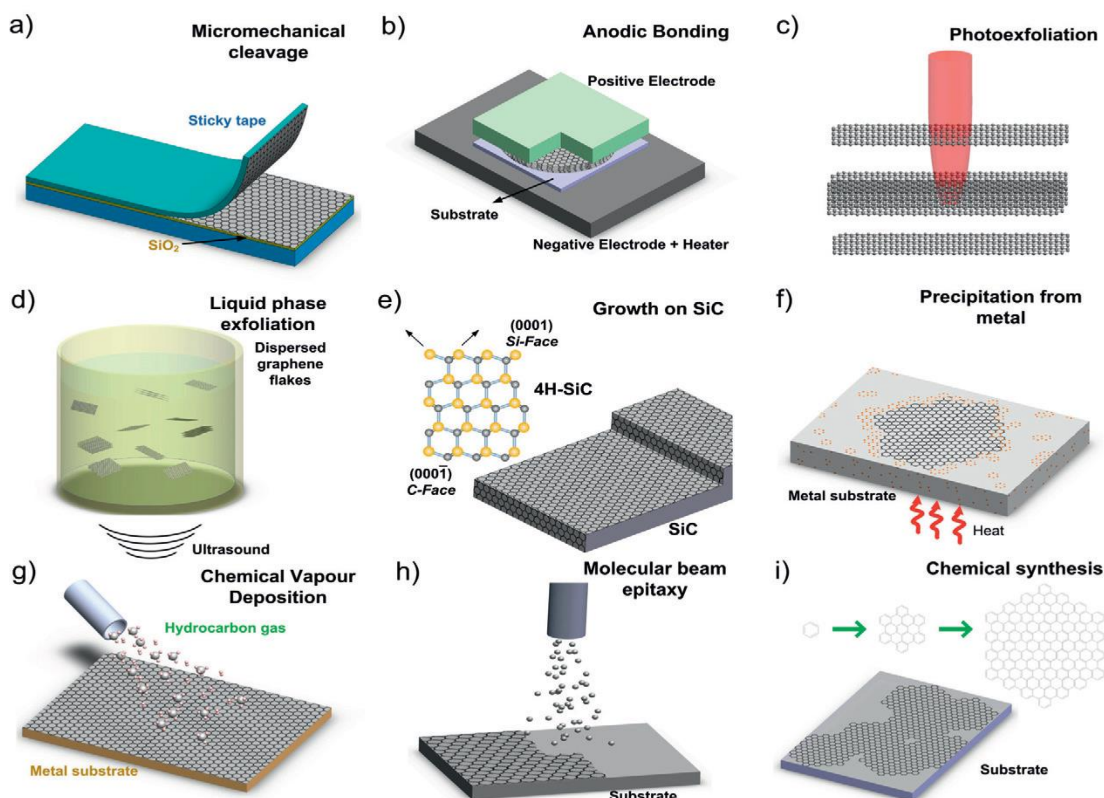

Figure 1.12 Schematic illustration of the main graphene production techniques. (a) Micromechanical cleavage (b) Anodic bonding (c) Photoexfoliation (d) Liquid-phase exfoliation (e) Growth on SiC (f) Segregation/precipitation from carbon containing metal substrate (g) Chemical vapor deposition (h) Molecular Beam epitaxy (i) Chemical synthesis using benzene as building block. [44]

between large-scale cost-effective production methods and ease of fabrication and acceptable materials quality, and base on these two criterions the choice of the fabrication technique can be done. Some of the most widely used or proposed techniques are summarized in Figure 1.12.

1.5.1 Micromechanical cleavage

Graphene was initially produced by mechanical exfoliation of Highly Oriented Pyrolytic Graphite (HOPG) using sticky tape to extract thin layers of graphene and then depositing them on a silicon substrate [5]. HOPG is used for this method, as it gives large flakes with little contamination. The graphite crystal is cleaved several times using the tape, then pressed against the desired substrate. And finally, the tape is carefully removed. This procedure results in a countless graphite flakes with varying thickness and lateral dimensions, with only a small portion being monolayer. Although the size of flakes and the production throughput is limited, this method is still dominant technique for scientific purposes, as it produces the highest quality graphene in terms of structural integrity and carrier mobility.

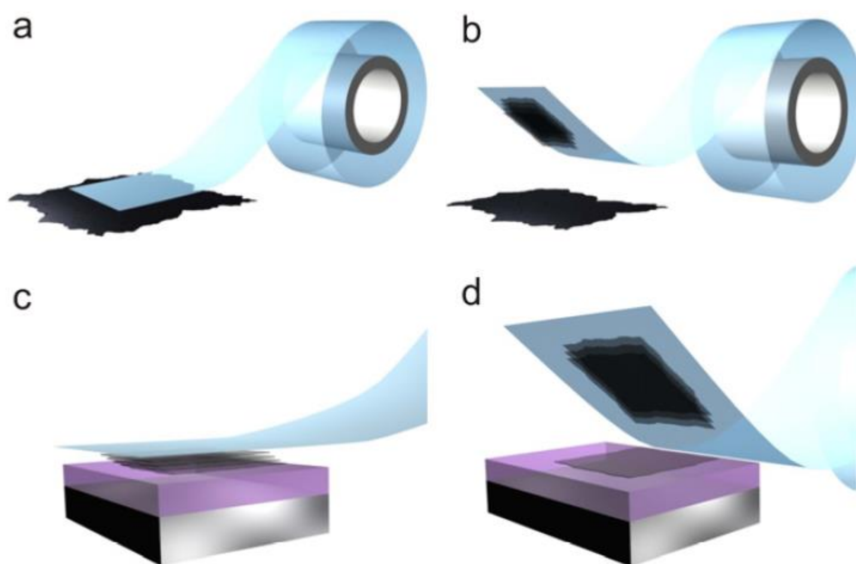

Figure 1.13 Micromechanical cleavage of 2D crystals. (a) (b) Adhesive tape is pressed against a 2D crystal so that the top few layers are attached to the tape. (c) The tape with crystals of layered material is pressed against a surface of choice. (d) Upon peeling off, the bottom layer is left on the substrate. [45]

1.5.2 Liquid-phase exfoliation

Graphene can be obtained by exfoliation of graphite in liquid environments using ultrasounds to extract individual layers, Figure 1.12 (d). This process generally involves three steps: (1) dispersion of graphite in a solvent, which can be organic or water base solvent; (2) exfoliation; and (3) purification, this step is necessary to separate exfoliated from un-exfoliated flakes, and is usually done through ultracentrifugation [44] [46] [47]. The quality of produced graphene flakes and low complexity of production, makes such graphene a good candidate for bulk application; like in composite materials or as coating [15] [16]. However, its use in electronic applications is still not

practical, due to having very small size of the flakes and the low control over the process for getting individual graphene flacks.

1.5.3 Epitaxial growth

Growth of graphene on SiC is usually referred to as “epitaxial growth”, even though there is a very large lattice mismatch between SiC (3.073 Å) and graphene (2.46 Å). The carbon atoms rearrange themselves in a hexagonal structure when Si atoms sublimates from the SiC substrate, which is different than deposition on the SiC surface, as would happen in a traditional epitaxial growth process [44]. Silicon carbide (SiC) sublimation, Figure 1.12 (e), which involves thermal decomposition of single-crystal SiC(0001) at high temperature (∼1600 °C) in an inert atmosphere, results into sublimation of Si and leaving behind a carbon rich film on the faces of the SiC crystal [48][49]. Only shortfall of this method right now is continuity and uniformity of the grown film, which makes graphene quality not as good as that of exfoliated graphene. On the other hand, a considerable advantage of this method is that the graphene film is directly grown on insulating SiC substrates, which can be directly used for device fabrication means no need to do transfer process.

1.5.4 Chemical vapour deposition

Chemical vapour deposition (CVD) is a well-known process for deposition of a thin crystalline film on any substrate, which is based on decomposition of precursor gases on a substrate. Substrate is exposed to one or several precursor gases which contains reactive elements. Epitaxial growth of graphene by CVD, generally has carbon-containing gas for deposition of carbon onto a lattice-matched substrate and some carrier gas like Ar and H_2. The carbon-containing gas decomposes at the high temperature (∼1000 °C), and thus free carbon atoms deposit on the surface and diffuse to form chemical bonds with each other [44][50-53]. The sp^2 bonds are the most stable and thermodynamically favourable bonding for carbon, but the temperature required for formation of such bond is much higher than the process temperature. So to make process more efficient, a metal catalyst is use as substrate, which lowers the energy barrier for creating such bonds. As for thin film deposition, higher temperature and low deposition rate is favourable condition for high quality crystal growth. So in graphene CVD process preferred condition are, the process temperature as close as possible to melting point of the metal catalyst and the partial pressure of the carbon-containing gas as low as possible.

One of the main aspect need to consider for this process is the right choice of catalyst metal substrate. Although the amount of carbon that can be dissolved in most metals is up to a few atomic percent, but to eliminate the alloy formation and carbon precipitation, it is preferred to use a non-carbide forming metals, like Ir, Cu, Ni, Pt, etc. Metal like Ir, which has very low carbon solubility, low pressure CVD on Ir(111) single crystals using an ethylene precursor, yields a good graphene film [44][52]. But Ir’s chemical inertness makes it difficult to transfer graphene to other substrates and also Ir is very expensive metal. On the other hand, Ni and Cu is less expensive, but has somewhat high solubility for carbon. Compare to Ni, it was found that thermal catalytic

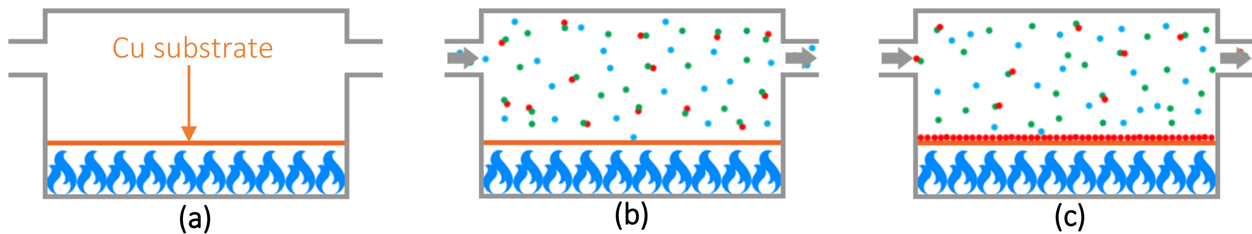

Figure 1.14 Chemical vapour deposition for graphene. (a) A copper substrate is heated at high temperature (~1000°C) and at low pressure in a furnace, to anneal the metal substrate. (b) Argon, methane and hydrogen gages flow through the furnace. (c) Carbon atoms from the methane decomposed on the copper and crystallize as a continuous graphene sheet.

decomposition of methane on a Cu foil, results in a self-limited process, which yielding around 95% of the substrate surface covered by single layer graphene [50]. Till now the highest quality and large area CVD-grown graphene is produced on copper catalysts [55]. And it is easy to transfer graphene from the Ni and Cu substrate. Due to the simplicity of the growth process and ability to have large area graphene, this technique arises as the most promising method to have graphene for electronic applications. However, CVD-grown graphene does not have as high quality as that obtained by micromechanical cleavage, so far for CVD graphene transferred to SiO_2 substrate mobility values of more than 20,000 $cm^2V^{-1}s^{-1}$ at room temperature is reported [55][56].

1.6 High-κ materials

Based on electronic properties, materials can be broadly classified in three different types: conductors, semiconductors, and insulators. An electronic conductor is a material in which electrons can move freely from one atom or molecule to another, thereby allowing charge carriers to conduct current. While a dielectric material is an electrical insulator in which the electrons or better charge carriers can only move within, or rather between atoms and molecules, unless the charge carrier jump a large band gap and moved to conduction band. Due to this bound nature of electron in this material, electrons stretch and rotate around atoms and form dipole moments, causing the dielectric material to become polarized under an applied electric field [57]. The extent to which a material can be polarized is a physical property of that material, but quantitatively it can be represented as its dielectric constant (κ).

Dielectric material plays one of the most important role in transistor technology, and particularly very crucial in field effect transistors (FET). It is used as a sandwich layer between the metal gate electrode and the semiconductor channel. At present dominant dielectric material used in semiconductor industry is SiO_2, and generally because of this kind of topology of system and material used, it is commonly referred as complementary metal-oxide semiconductor (CMOS) technologies. The role of dielectric material, is to form a capacitor between the metal gate electrode and the semiconductor channel. Which modulates the distribution of electrical charges at that interface, when a voltage is applied to the gate electrode, thus changes the conductivity of semiconductor channel [58].

From basic capacitor equation $Q = CV$, where Q is the accumulated charge, V is the applied voltage and C is the capacitance of the device. The capacitance can be derived as $C = \kappa\varepsilon_0 A/t$, where A is the capacitor area, t is the thickness of the capacitor insulator (dielectric material), ε_0 is the permittivity of vacuum and κ is the relative dielectric constant [58]. So an increase in C will result in a larger Q and ultimately result in a larger charge carrier density in the semiconductor channel even though other parameters are held constant. Here C can be improved by increasing area, reducing the dielectric thickness or by having higher dielectric constant material. For the past few decades, the scaling of Si technology has increased C by decreasing t. But due to quantum mechanical tunnelling effect further reduction in the gate-oxide thickness is not advisable. Since then focus has been changed to increase C, by increasing κ; means new gate dielectric materials. And generally the term high–κ material is used for the materials which do have dielectric constant higher than SiO_2.

However, it is also important to note that high-κ materials have their own drawbacks. Firstly, dielectric materials with high-κ have larger atoms such as Hf and Ti compared to Si, which generally makes the lattice constant different than that of the semiconductor material underneath (which is Si in most of the CMOS technology). These materials also have smaller band gaps [59], which means there is trade-off between dielectric constant and its thickness. As smaller band gap of gate-oxide material would increase the probability of charge carrier tunnelling, so this will put some limits on decreasing the thickness of oxide. Addition to this it is observed that the high-κ materials also degrade carrier mobility in the channel region, at least for Si metal-oxide-semiconductor FET (MOSFET) [60]. But as here the use of high-κ material is for graphene base transistor, so limitation and advantages of one or the other material is different compare to Si transistors.

1.6.1 Possible high-κ materials for GFETs

Many kind of dielectric materials with high dielectric constant are available, some of them are having very high dielectric constant but do lack enough band gap for electronic application [59]. The following is a brief description of some of the possible materials being considered.

Firstly, the most widely used dielectric material in Si CMOS industry is oxides. Considering the same scaling requirement as of Si CMOS devices, for graphene FETs also, it is better to start considering other gate dielectric materials. Other than SiO_2 most impressive and easy to implement oxide in GFETs is alumina (Al_2O_3) [61], it has somewhat higher dielectric constant ($\kappa \sim 9$) as well as good band gap ($E_G \sim 8.8$ eV) [59]. But main feature is, ease with which it can be used in GFETs. One another extensively studied oxide, particularly by a company like Intel, is Hafnium based high-κ materials. Intel has first introduced Hf based high-κ dielectrics for their 45 nm technology CMOS chips, which began manufacturing in 2007 [63], and currently using it in 32 nm technology [64]. HfO2 has a relatively high dielectric constant ($\kappa \sim 25$) and a large band gap ($E_G \sim 5.8$ eV) [62]. So for Si CMOS it is considered as next dielectric material for gate insulator.

When it comes to ultrahigh-κ materials, they do have relative dielectric constant as high as 50 to 100 times higher than SiO_2. But at the same time it is also required to consider the band of these materials, to actually gain advantage of having such high dielectric constant. One of the candid material is TiO_2 [65] having dielectric constant (κ) of about 80 with band gap (E_G) around 3.5 eV [59]. But due to low band gap its application as gate dielectric material is not much convincing. On the other hand, the one which actually can be referred as ultrahigh-κ material is Strontium Titanate - $SrTiO_3$ (STO). Its dielectric constant is around 300 [66] and at the same time have band gap of about 3.2 eV [36] at room temperature. So compare to TiO_2, it has very high dielectric constant, so it is worth to give try to implement it in GFETs.

Second class of material which is generally considered for graphene is organic and polymer base dielectrics. Owing to flexibility, good electrical conductivity and transparency – graphene is one of the best suitable material for organic field effect transistors, in which semiconducting material is itself an organic or polymer base material. But most organic and polymer base materials do have dielectric constant even lower than SiO_2 or in the range of it. So they are out of the scope of this work, which is related to ultrahigh-κ materials, while these materials can be consider as low-κ materials.

Possible and already in use dielectric materials for GFETs are listed in table 1.1 below. From which it is clear that as the dielectric constant increases, the band gap decreases.

Table 1.1 Dielectric constant and band gap of various oxides. [36] [59] [66]

Dielectric material	Dielectric constant (κ)	Band gap [eV]
SiO_2	3.9	9
Al_2O_3	9	8.8
HfO_2	25	5.8
TiO_2	80	3.5
$SrTiO_3$	300	3.2

2 Graphene transistors

2.1 Physics of field-effect transistors

2.2 Radiofrequency application of FETs

2.3 Graphene properties relevant to transistors

2.4 State of the art of graphene transistors

2.5 Importance of gate oxide in GFETs

2 Graphene transistors

State of the art graphene transistors are mainly realised as the field-effect transistors (FETs), because this is the most successful device concept in electronics. FET is the back-bone of modern information and communication technology. Semiconductor electronics can be divided broadly in two principal divisions; digital logic devices and radiofrequency (RF) devices. Till today Si MOSFETs are the dominant technology for digital logic devices. For decades, semiconductor mainstream electronics (processors, memories, etc.) are continuously making MOSFETs smaller and smaller to have higher performance for digital logic devices, which results in almost twofold increase in the number of transistor every 18 months, leading to significant improvements in performance and decreases in price per transistor [67]. Today, Si MOSFETs with 14nm gates are already in mass production, and according to the International Technology Roadmap for Semiconductors (ITRS 2.0), by the year 2020 there will be 10nm MOSFETs [68].

2.1 Physics of field-effect transistors

A FET is a three port device, consisting of a channel region connected by source and drain electrodes, and a gate electrode separated by a barrier from the channel (Figure 2.1 (a)). The conventional FET works by controlling the channel conductivity, and thus the drain current, by a voltage V_{GS}, applied between the gate and source. Applying a gate potential makes the gate-oxide structure to behave like a capacitor, which attracts carriers from the bulk semiconductor toward the channel. These charge carriers, electrons and holes in channel are in an electric field, generated through the application of a voltage between source and drain (V_{DS}). Due to this electric field, an electromotive force is generated on them, which force them to move along the channel [58].

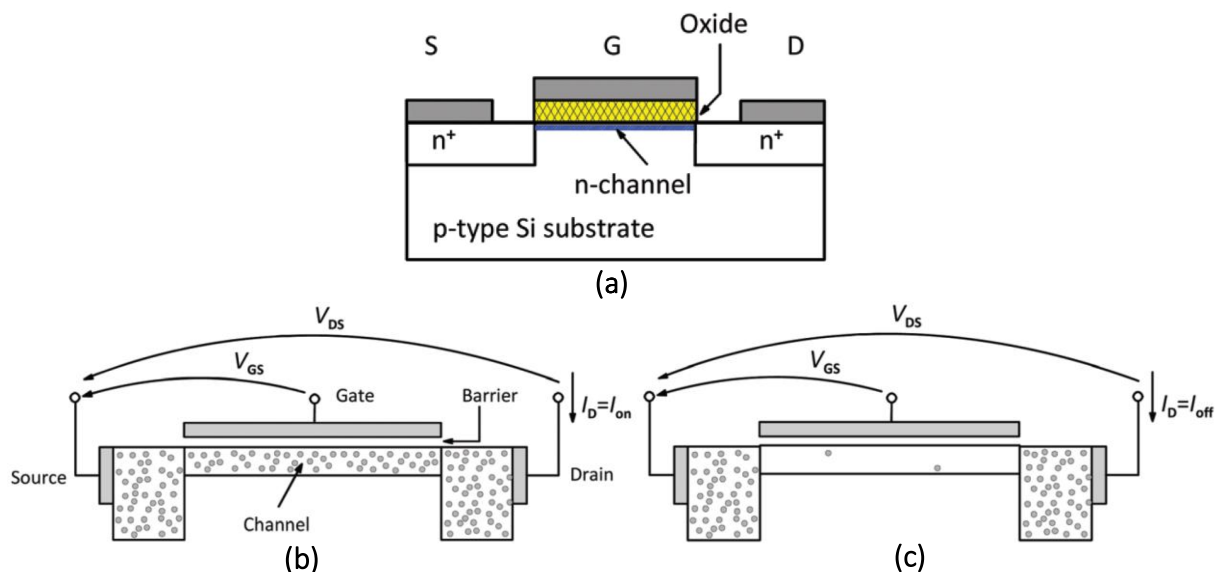

Figure 2.1 Basic FET structure. (a) Conventional Si n-channel MOSFET. Generic structure of a FET (b) in the on-state and (c) in the off-state. [69]

In digital logic, the FET is supposed to switch between on and off. In Si MOSFET it is done by different doping of the bulk and the source-drain regions, which makes p-n junctions at the interface. In FET to make ohmic contact between metal electrodes and source-drain region, generally these regions are doped heavily. In on-state (Figure 2.1 (b)), the channel has a large charge carriers and low resistance, which makes a large on-current (I_{on}). In off-state (Figure 2.1 (c)), there should not be current flowing between drain and source, this happens when the applied gate voltage (V_{GS}) is less than a well-defined threshold voltage (V_{th}), which restricts the current flow due to presence of p-n junctions at the interface, thus the off-current (I_{off}) becomes very small. One of the important figure of merit (FOM) of FETs for digital logic application is on-off ratio, which is the ratio of I_{on} and I_{off}. FET with high on-off ratio is considered good for digital applications [69].

While for RF application, FET does not require to be switched off. Infect, in most RF amplifier application of FET, it is always in on-state. Generally small signal is applied as input to the gate, which appears to be amplified at the output between source-drain. The extent to which the input signal is amplified is called gain. The small-signal current gain, is defined as the RF output current of the transistor divided by the RF input current. Gains are frequency dependent and decrease with increasing frequency. Two important FOMs of RF application of transistors, are the characteristic frequencies f_T and f_{max}. f_T is the cut-off frequency, the frequency at which the small signal current gain of the transistor reduced to unity. And f_{max} is the maximum frequency of oscillation, the frequency where the unilateral power gain becomes unity [69].

Another parameter used in FET description is the gate-capacitance per unit area of the gate-oxide structure, which can be defined as:

$$C_g = \frac{\kappa}{t} \tag{2.1}$$

where κ is the dielectric constant of gate-oxide and t is its thickness. It is a parameter which shows the ability of the gate to modulate the charges in the channel [58]. Higher the value of gate-capacitance, lower the V_{GS} is required to reach certain I_D, which means reduction in on-off switching time.

2.2 Radiofrequency application of FETs

Analog/RF electronic circuits are relatively simple compared to digital logic circuits, and are less integrated. So it is more easy to experiment new materials and devices with RF technology. In analog/RF high-speed applications, FETs should respond quickly to a variation in the gate voltage; and as mention previously this can be done with high gate capacitance and with high mobility carriers in short channel. In RF application, DC voltages V_{GS} is applied to the terminals of a FET, to make FET work in on-state, and a small RF signal to be amplified is applied as superimposed over it. By the small gate voltage variation $\pm\Delta V_{GS}$, the amount of carriers in the channel, and consequently, the drain current (I_D) is changed. The amplification characteristics of transistors are described in terms of the intrinsic gain, the current gain, and the unilateral power gain [70].

The frequency performance of FET can be discussed with their small-signal equivalent circuit, as shown in figure 2.2. In which intrinsic FET it the gate stack of transistor and the channel underneath.

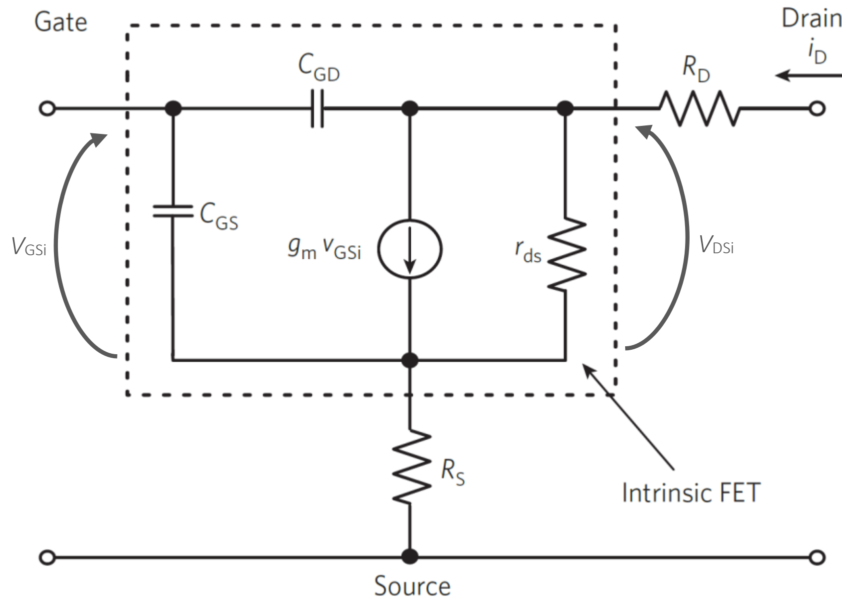

Figure 2.2 Small-signal equivalent FET circuit. The intrinsic transconductance (g_m), is related to the internal small-signal gate–source (V_{GSi}) and drain–source voltages (V_{DSi}), whereas the terminal transconductance (g_{mt}), is related to the applied gate–source (V_{GS}) and drain–source voltages (V_{DS}). [22]

In the equivalent circuit the intrinsic transconductance (g_m), the slope of the transfer characteristics of FET, can define as [22],

$$g_m = \left.\frac{\mathrm{d}I_\mathrm{D}}{\mathrm{d}V_\mathrm{GSi}}\right|_{V_\mathrm{DSi}=\mathrm{const}} \tag{2.2}$$

while the drain conductance (g_{ds}), the slope of the output characteristics of FET, can be define as [22],

$$g_{ds} = \frac{1}{r_{ds}} = \left.\frac{\mathrm{d}I_\mathrm{D}}{\mathrm{d}V_\mathrm{DSi}}\right|_{V_\mathrm{GSi}=\mathrm{const}} \tag{2.3}$$

R_D and R_S are source and drain series resistance respectively. The cut-off frequency (f_T), is the highest frequency at which the transistor should be used for RF application. From this the characteristic frequency of the transistor, cut-off frequency can be written as [22] [70],

$$f_T \approx \frac{g_m}{2\pi} \frac{1}{(C_\mathrm{GS} + C_\mathrm{GD})[1 + g_{ds}(R_\mathrm{s} + R_\mathrm{D})] + C_\mathrm{GD} g_m (R_\mathrm{s} + R_\mathrm{D})} \tag{2.4}$$

Another important FOM for FET is intrinsic gain (G_{int}), can be defined as, $G_{int} = g_m/g_{ds}$ [22], for low frequency this help to get frequency-dependent voltage gain (A_V), as it becomes more or less similar to each other [69].

From the equation 2.4, it is clear that to maximize the f_T, g_m should be as large as possible while all other quantities as small as possible. But value of these properties varies with applied voltages, V_{GS} and V_{DS}. Particularly drain bias affects the FET performance more compare to gate bias [70]. This behavior becomes clear when considering equation 2.4 together with Figure 2.3 (b). The small g_m and the large g_{ds} at low V_{DS} automatically lead to small gains and thus to low f_T and f_{max}. So FET must have to be used in saturation region to fully exploit its speedy operation. Roughly a high frequency performances increment can be obtained by scaling the transistors, but the continued miniaturization of FET, has adverse effects on its performance. Some of these can be partially mitigated by using high mobility channel material, or having very thin channel. For this reason, graphene can be used in order to overcome some problems reaching higher frequency of operation, as it has high mobility and it is the thinnest material possible.

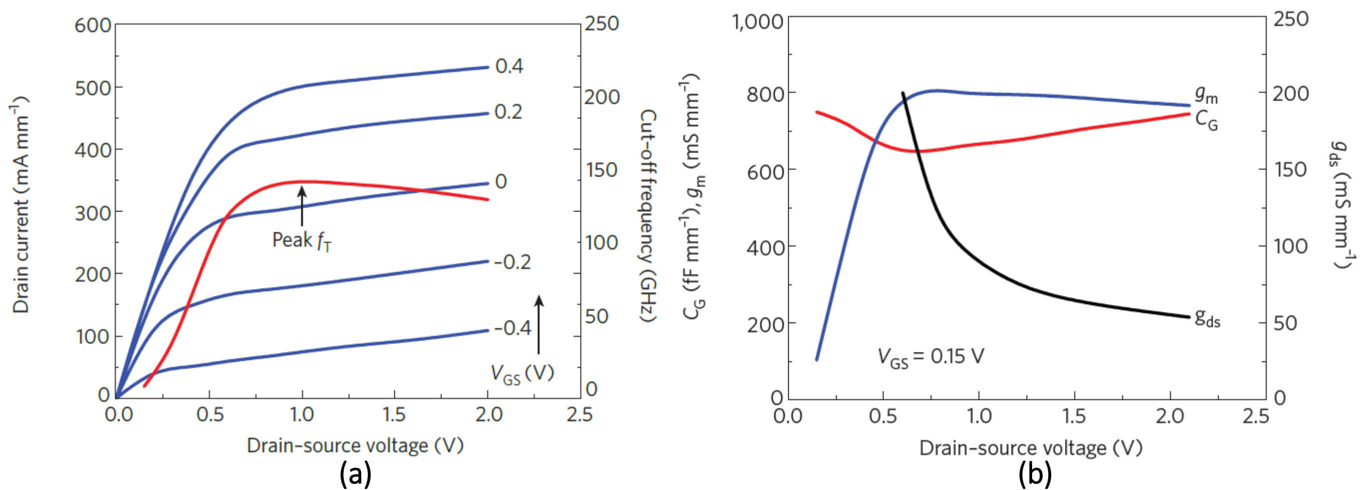

Figure 2.3 (a) Output characteristics (blue lines) of a FET at differ values of V_{GS} together with its f_T (red line). The cut-off frequency peaks at V_{DS} = 1 V and V_{GS} = 0.15 V. (b) Elements of the equivalent circuit as a function of V_{DS}; the overall gate capacitance C_G is the sum of C_{GS} and C_{GD}. [22]

2.3 Graphene properties relevant to transistors

The ideal semiconductor properties for transistors would be (1) sufficiently wide bandgap; (2) good charge carrier mobility; (3) high enough thermal conductivity; (4) low contact resistance; (5) large scale producible, and compatible with Si CMOS technology; and (6) interfaces to dielectrics with low defect density [69] [70]. Unfortunately, all these properties don't exist in a single material, there is always trade-off between different properties. Now question is how good graphene is in terms of these desirable properties for transistor material.

Large areal graphene is gapless material, means behave like semimetal [2] [17]; so first requirement is already cannot be fulfilled. But there are different ways to open a gap in graphene. One of the way is to make graphene nanoribbons (GNRs) [21], but it is extremely difficult to make GNRs with required width of few nanometres and it also suffers from edge damaging, which influence the carrier transport properties. The second way by which gap can be open is to use bilayer graphene [71]. Although there is a limit on the maximum possibility to open the band-gap through this method. There are other ways also to have band gap in the graphene. However

gapless graphene has very good carrier mobility as mention in previous section 1.3, mobility ranging from 10,000 $cm^2V^{-1}s^{-1}$ to 100,000 $cm^2V^{-1}s^{-1}$ has been observed in graphene [27-30]. Which makes graphene good material for transistor base on the second requirement mention above.

Graphene is the best conductor of heat at room temperature with heat conductivity of ∼4.84 ± (0.44) $\times 10^3$ to 5.30 ± (0.48) $\times 10^3$ W/mK [11], compared to 4 $\times 10^2$ W/mK for copper. In semiconductor devices, particularly in CMOS technology, a high thermal conductivity of the channel material is certainly desirable for better heat dissipation. The resistance between metal contacts and graphene channel should be as low as possible for the optimum operation of transistors. Contact resistances in the range of 100–1000 Ωμm have been demonstrated [72], which is not the best for transistor application but further progress can be done to reduce the contact resistance [69]. Regarding large scale production of graphene, as described in the section 1.5, it is pretty easy to have large area graphene over any kind of substrate now a day.

2.4 State of the art of graphene transistors

GFETs with gapless large area graphene channels cannot be switched off and thus have very low on–off ratios of only 2–10. Thus, large area graphene is not a suitable as channel material for digital logic FETs. So far most of the work on GFETs is done for RF applications. Soon after first observation of a field effect in graphene by Novoselov et al. [5], its application as channel material for RF application has been investigated. The first GFET for RF application with f_T about 14.7 GHz was made using exfoliated graphene having 500 nm gate channel length and HfO_2 as top gate material in late 2008 [73]. Since then many other groups around the world have done significant work for the improvement of RF performance of GFETs, which is well summarised by F. Schwierz [70]. Till now the best reported f_T for GFETs is 427 GHz [74]. Figure 2.4 shows the best reported cut-off frequency and maximum frequency for various MOSFETs.

From Figure 2.4 (a) it is clear that for conventional MOSFETs with channel length higher than 0.2 μm, the f_T has an L^{-1} dependence, where L is the gate channel length. Furthermore, f_T increases with the channel mobility [22] [70]. Channel mobilities of Si MOSFETs is few 100 $cm^2V^{-1}s^{-1}$, for GaAs pHEMTs it is about 6000 $cm^2V^{-1}s^{-1}$, and for InP HEMTs and GaAs mHEMTs it is above 10,000 $cm^2V^{-1}s^{-1}$ [70]. On the other side, when the gate length is about 100 nm or below, GFETs do compete extremely well with conventional HEMTs, which are the fastest RF FETs at all. Although GFETs' impressing f_T performance, they behave rather poor in terms of the maximum frequency of oscillation f_{max}, as can be seen in the Figure 2.4 (b). One of the reason for poor f_{max} performance of GFETs is the missing gap in large area graphene. Another noticeable difference of GFETs compare to other competing FET, which can be easily recognised from Figure 2.4 (b) is, f_{max} for GFETs does not show any distinct gate length dependence. So far the best reported f_{max} for GFETs is 105 GHz with 100 nm gate length [75]. Just for a note all the mentioned values above and in the Figure 2.4 are de-embedded data, so actual measured data may be much different than reported one.

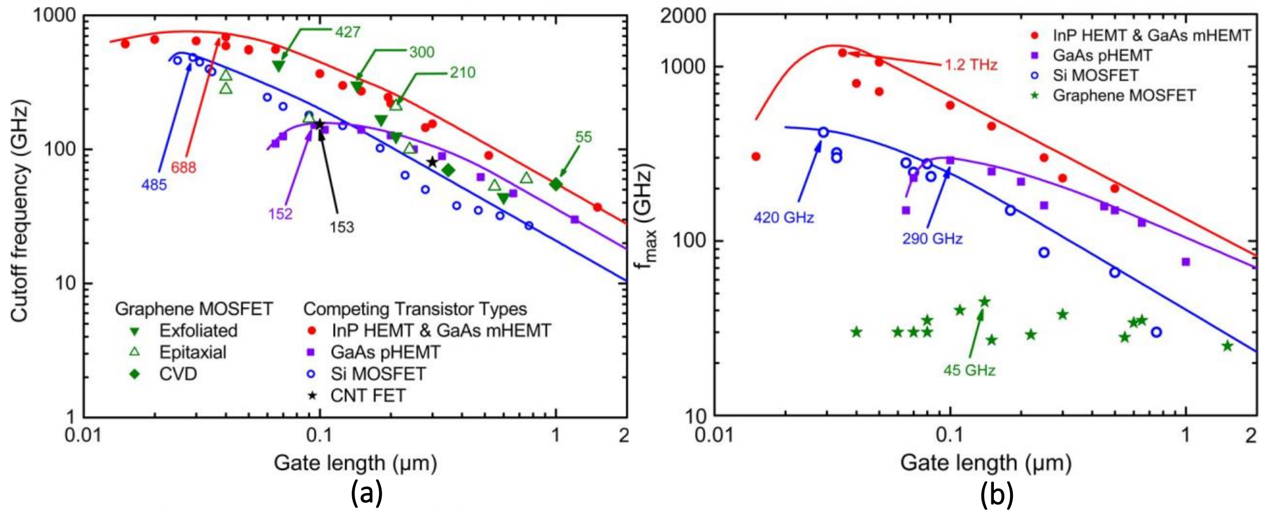

Figure 2.4 (a) Cutoff frequency (f_T) of various MOSFETs versus gate length (L); the symbols are experimental data points and the lines are for reference. The highest f_T 668GHz among all reported values, is for GaAs metamorphic HEMT (mHEMT) with a 40 nm gate, and f_T of 644 GHz for a 30 nm InP HEMT. For a Si MOSFET the highest f_T is 485 GHz with a 29 nm gate. While for a GaAs pseudomorphic HEMT (pHEMT) the highest f_T is 152 GHz with a 100 nm gate. On the other hand, the fastest nanotube device (CNT FET) has fT about 153 GHz with a 100 nm gate, and the fastest reported graphene MOSFET has fT around 427 GHz with 67 nm gate. (b) Maximum frequency of oscillation (f_{max}) of various MOSFETs versus gate length (L). The highest f_{max} data reported for graphene MOSFETs is 45 GHz only, compared to several hundreds of gigahertz for the competing FET types and a record f_{max} about 1.2 THz for an InP HEMT with 35 nm gate length. [70]

However, unlike Si MOSFETs, for GFETs the gate resistance is not the dominant effect causing the poor f_{max}. Instead, the weak and poor saturation causing large drain conductance g_{ds}, with too high source drain series resistance, may be the reason of poor f_{max} of GFETs [70]. As due to larger g_{ds} the intrinsic gain $G_{int} = g_m/g_{ds}$ would become significantly lower, which is one of the possible effect of poor GFETs performance. As the g_{ds} value depends mainly on the output characteristics of FETs, mainly small g_{ds} can only be achieved if the transistor works in saturation region. Unlike conventional FETs, GFETs behaves much differently while considering current saturation. It is better to first understand the physics of current saturation in GFETs as describe by Meric et al. [76].

The output characteristic for GFETs generally has a linear shape without any saturation or have some unusual form of saturation like behaviour, that is saturation regime in-between two linear regimes, as can be seen in Figure 2.5 (a). While for a convention FETs, one can easily find a well define saturation regime, this is the condition in which most FETs works. When FET operates in the saturation regime the carrier density in channel continuously decreases towards the drain and forms pinch-off region near drain. While in graphene due to its ambipolar nature, this kind of behaviour is hard to observe and this results in unusual output characteristic of GFETs. In a GFET,

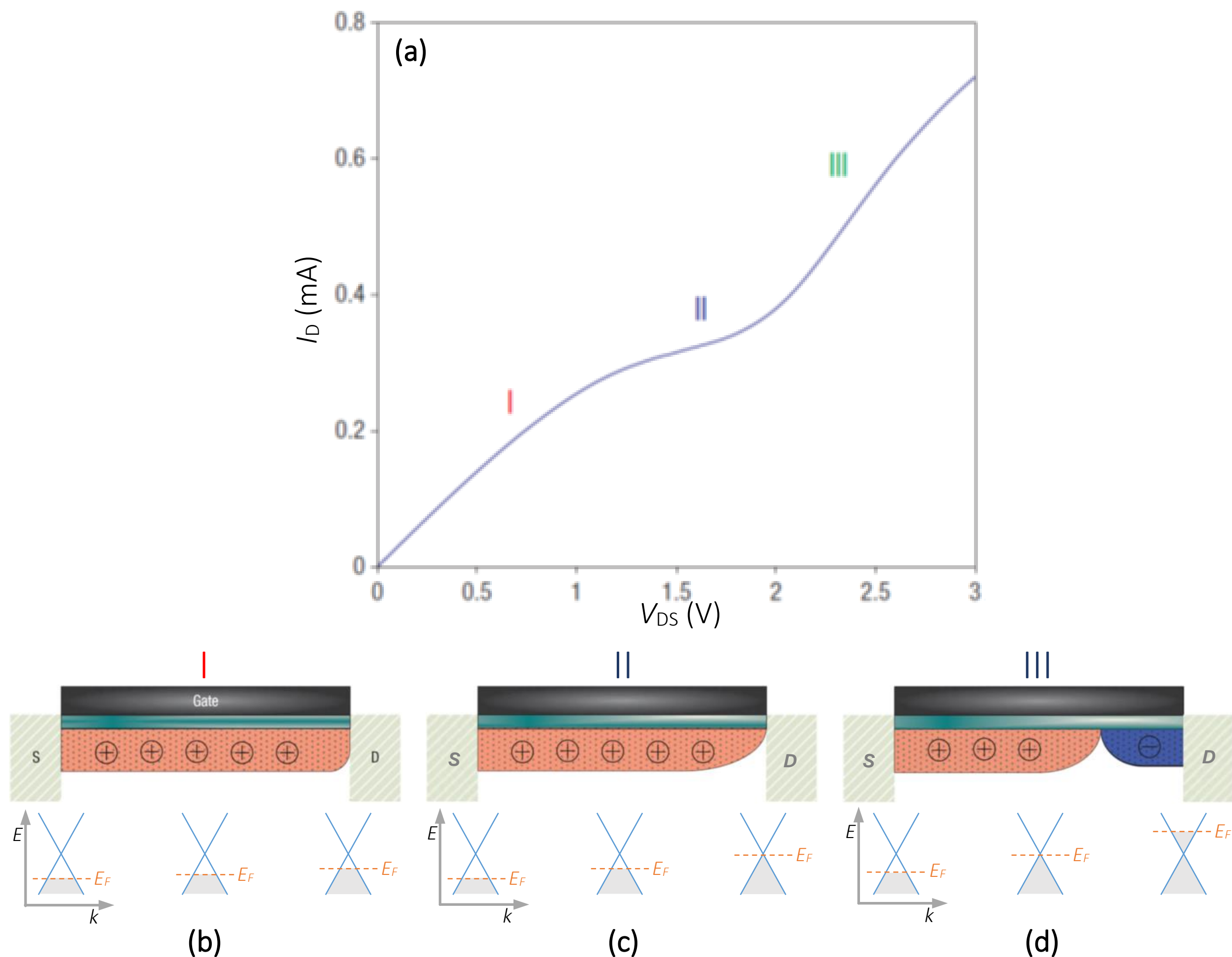

Figure 2.5 Direct-current behavior of GFET (a) Schematic output characteristics of the GFET and indicating three operation regimes of it. (b), (c) and (d) Schematic demonstration of the carrier concentration under the top-gated region and conical shaped band structure with fermi energy level at different operation regimes of GFET. (b) V_{DS} is positive but still lower than V_{th} (the voltage required to have Dirac condition), (c) V_{DS} equal to V_{th}. (d) V_{DS} higher than V_{th}. [76]

the carrier density decreases initially when moving towards drain in the channel. But still there is no pinch-off effect, as can be seen in Figure 2.5 (b). In this situation when the V_{DS} is still lower than V_{th} (the voltage required to have Dirac condition), transistor operates in linear regime – I (Figure 2.5 (a)), and current is entirely carried by holes throughout the length of the channel. With further increase in V_{DS}, the drain current starts to saturate until the inflection point reached, when V_{DS} becomes equal to V_{th}, at this point, the potential conditions at the drain correspond to the Dirac point. Due to this, there is a pinch-off region at the drain (Figure 2.5(c)), that results in a sort of saturation behaviour (regime II in Figure 2.5 (a)). After the onset of current saturation, the slope of the output curves again starts to increase; this is sometimes known as the second linear regime (regime III in Figure 2.5 (a)). In this bias range the carriers in the channel on the source side are holes, and those on the drain side are electrons. In this ambipolar regime, the pinch-off point becomes a place of recombination for holes from the source and electrons from the drain, and as there is no bandgap, no energy is released in this recombination. At sufficiently large values of V_{DS},

the output characteristics shows a zero or even negative transconductance, which is a highly undesirable situation, as it means that the gate is no more effectively controlling the current flowing through the channel. It should be noted that the reason for this behaviour is the missing bandgap of the graphene channel. Moreover, the series resistances of source and drain also have an effect on the saturation behaviour [70].

From this discussion it is clear that, to achieve competitive power gain and f_{max} performance for GFETs, it is required to have current saturation and if a channel with a bandgap is used than performance can be further improved. On the other hand, very high mobility of graphene also contributes to achieve the high transconductance, even if it is hard to have a saturation current in GFETs. Due to ambipolar nature of graphene, as mention in the previous section 1.3, transfer curve for GFETs has V-shape, which makes the slope of the curve lowest at the Dirac point. Generally, the maximum slope of the curve is somewhere near the Dirac point, which can be easily found, and for best performance of the transistor, it should be operated at that point. As the slope of the transfer curve is the transconductance of the device, and maximum f_T and f_{max} can achieved when the transistor works with maximum g_m, as mention earlier.

Along with the development in the GFETs, several groups across the globe have also demonstrated different kinds of integrated circuits (e.g., amplifiers, mixers, frequency multipliers, and oscillators) using GFETs [84]. Starting with just two GFETs for logic inverters in 2010 [79], various complex circuits operating in GHz range were successfully demonstrated [80-85]. Last year at L-NESS laboratory in Como, where this project was done, graphene ring oscillators comprised of 4 inverter stages and with oscillation frequency 4.3 GHz, which is the highest oscillation frequency obtained in any strictly low-dimensional material to date, had been measured [86].

2.5 Importance of gate oxide in GFETs

As already mentioned earlier in this chapter, the two major figure of merits for the RF performances of a transistor are the cut off frequency and the maximum oscillation frequency. There are many parameters which influence the high frequency performance of any FET based device, among those one of the important factor which need to consider is the gate stack. The ability of faster switching of the transistor from one state to another is mainly depends on the gate capacitance per unit area defined previously as equation 2.1. This is basically the capability of the gate to modulate the carrier concentration along the channel. And as mention in section 1.6, the choice of the dielectric layer becomes a crucial aspect in the fabrication of high frequency GFETs, as small gate oxide thicknesses may suffer from large leakage current through the gate. Instead using high-κ materials, allows to maintain high values of C_g while using higher thickness. Thus using this kind of gate oxide for GFETs gate stacks seems to be the most promising way to get high frequency performances.

However, to have a uniform layer of high-κ material over graphene is quite difficult. Most of the methods for deposition of high-κ materials operates at very high temperature, so that puts some limit on the use of this kind of materials in GFETs. And one of the negative effect of having high-κ

gate oxide is reduction in carrier mobility [60], due to generation of defects in the graphene below. But there are some ways to have a good oxide layer, like formation of a very thin layer of AlO_x (around 4 nm) at the graphene interface, due to oxidation of aluminium [79]. Another method, recently in much focus for GFETs is, T-shaped gates [75]. Due to its unique architecture, it has low gate resistance and low parasitic capacitance, which improves the f_T and f_{max} for the GFETs (base on the equation 2.4). other than the gate stack, if only gate oxide material is considered assuming no influence of other parameters, then by rearranging the equation of the field-effect mobility [22], equation for transconductance g_m can be written as,

$$g_m = \frac{\mathrm{W}}{\mathrm{L}} \frac{\kappa\, \mu_{FE}}{t} V_{\mathrm{DS}} \tag{2.5}$$

where W is the channel width and μ_{FE} is the field-effect mobility of the channel material. So from this equation keeping all other parameters constant except κ and t, it is clear that to maximise the g_m, higher value of κ, and lower value of t is required. In this report we have made GFETs using STO having κ around 230 and with thickness of 160 nm, which makes the dielectric constant to oxide thickness ratio around 1.44, somewhat similar to native AlO_x as gate oxide in GFETs (considering that the carrier mobilities are same for both cases). Still further reduction of thickness for STO can be done to push the performance of the device, but also need to considered that the band gap for STO is much lower compared to SiO_2 and Al_2O_3. So it is not possible to have few nm gate oxide thickness for STO, as in that case there will be huge leakage current through gate.

3 Device fabrication

3.1 Fabrication processes

Electron beam lithography (EBL)

Reactive ion etching (RIE)

Electron beam evaporation

3.2 Substrates

3.2.1 SiO_2/Si substrate

3.2.2 STO substrate

3.3 Graphene transfer

3.4 Device fabrication

3 Device fabrication

In this chapter an overview of the substrates and different processes required for the fabrication of the samples is given. Section 3.1 presents an overview of different fabrication techniques used for preparation of samples. Section 3.2 includes details regarding SiO_2/Si substrate and STO substrate. Graphene transfer method and evaluation of quality of transferred graphene is explained in section 3.3. And at last, a step by step procedure for the device fabrication is given in section 3.4.

In this work, we prepared field effect transistors using graphene as channel material. It had a very simple structure, in which we had some conductive substrate covered with oxide on top (dielectric material, acting as gate oxide); over which CVD grown graphene was transferred and then electrodes were made over it. This kind of structure is commonly known as back gated devices. As the main aim was to characterise compatibly and effect of oxide materials in the GFETs, and then using GFETs having same gate length some complementary inverters were made to measure voltage gain for graphene inverters.

3.1 Fabrication processes

Most of the techniques used for fabrication of devices are standard processes used in microelectronics industries. For example, electron beam lithography (EBL) can be used for patterning the devices structures, plasma assisted reactive ion etching for removing unwanted graphene and electron beam evaporator for depositing metal as electrodes in the devices. All of these processes used for fabrication of devices are briefly introduced here in this section.

3.1.1 Electron beam lithography (EBL)

Lithography is one of the essential process in microelectronic device fabrication. Generally, for research purpose electron beam lithography is widely used compare to optical lithography, due to its flexibility and ease with which very low feature size structure can be obtained. Here by flexibility, it means, using EBL system any kind of shape and size variation can be easily adopted. And as the wavelength for electron is very small (∼7 pm at 30 keV), very high resolution can be obtained with this system. For EBL there are some specially made dedicated systems are available, but for this work a scanning electron microscope (SEM) attached with pattern generator and beam blanker; then the entire system can serve as EBL, is used.

In EBL a beam of highly focused electron is scanned over a surface to make some patterns on the resist. For that a design file is required according to which the beam moves and generates the pattern. In this work we had used Raith ELPHY Quantum GDSII Editor to generate the CAD file, which is used to give inputs to the EBL system about the locations and shapes to be written on the substrate. Depending on the resist used the pattern can be made, for example the positive resist will become more soluble after exposure while negative resist will become less soluble after exposer, so accordingly a design file can be generated. We had used Poly methyl methacrylate -

PMMA as resist material, with different density and molecular weight for different purpose, which will be clear later in this chapter.

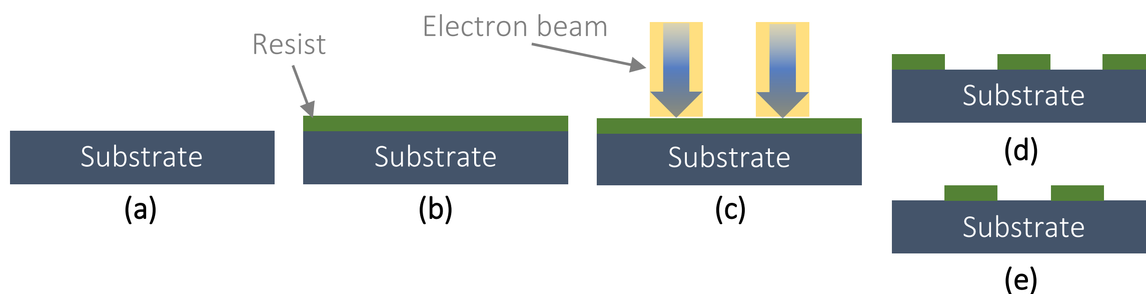

Figure 3.1 Schematic diagram for EBL steps. (a) Substrate cleaning. (b) Spin coating of resist on the substrate. (c) Electron beam exposure. (d) and (e) development step, based on the resist type mask will be developed. (d) Positive resist, exposed part of resist dissolved in developer solution. (e) Negative resist, unexposed part of resist dissolved in developer solution.

Same as lithography, first the substrate needs clean with bath in acetone followed by a rinse with isopropanol, to make sure there is no foreign particles and dirt on the substrate and to remove protective layer from it. After cleaning, substrate is ready to coat with resist, for which spin coating is the best way to do. In spin coating, material which need to be deposited is in liquid form, so based on its viscosity when the sample is rotated at high speed this will form a very thin and homogeneous layer of material over the surface. In our case after several test run, we had fixed the parameters for the spin coating for all kind of PMMA resist used, at 6500 rpm for 30 sec. As the material is having solvents to make it fluidic, it requires to be removed, this can be done by baking, for PMMA we used to follow baking at 160 °C for 5 min. Thus at the end there will be dense polymer film on the top of substrate ready for exposure. Once EBL is done the exposed area can be removed (as here PMMA is used which is positive resist so the area which is exposed will become more soluble) using a chemical solution, generally refers as developer. For PMMA a solution of 4-methyl-2-pentanone and isopropanol in a proportion of 1:3 was used. For development of the sample, it is put in the developer solution for 90 sec and then in isopropanol for 60 sec to remove excess developer solution from the sample, followed by a rinse with isopropanol and drying with dry nitrogen gun. After this there will be a patterned mask on the surface, ready to use for the subsequent process.

3.1.2 Reactive ion etching (RIE)

Reactive ion etching was used to etch the graphene. Compare to CMOS technology, for graphene etching is pretty simple. It can be done using low pressure oxygen plasma etching. As it is performed using gases it falls under the dry etching processes. In this plasma is created between two parallel plates, which makes the etching highly anisotropic. And on the other end, oxygen ions are very reactive with graphene compare to the PMMA resist used as mask. So combining these two features, it is easy to obtain well-defined regions of graphene by this method. After several test performed the process parameter concluded for best results for graphene etching was,

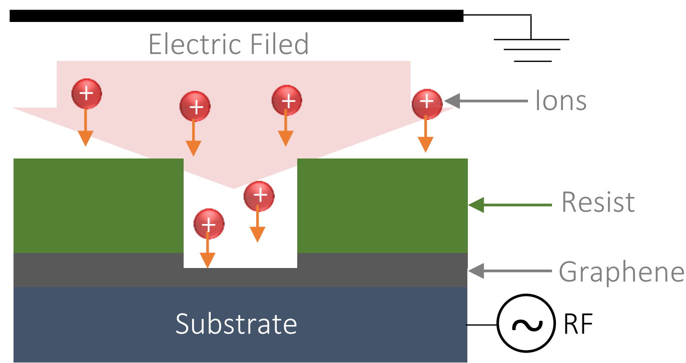

Figure 3.2 RIE schematic process. Under a radio frequency electric field, the plasma forms between the two electrodes, which accelerates the ions towards the substrates and those heavy ions etch the uncover part of sample.

plasma generation using RF excitation of 13.56 MHz frequency with 50 W power. And the oxygen flux of 500 sccm with the chamber pressure of 100 mTorr. RIE was done for 25 sec at the above mention parameters for graphene.

3.1.3 Electron beam evaporation

It is necessary to have some electrical connect with the device to perform measurements, and base on the device architecture some of its structure need to be deposited at different stages of fabrication. In this work electron beam evaporation is used to deposit metals to make marking grids and to make electrodes for the devices. In electron beam evaporation, from its name, it is clear that electron beam is used for evaporation of material. Here electrons are generated by heating the tungsten filament (thermionic emission), which is located under the crucibles. The beam is directed to the evaporation material in crucible using magnetic field. When these high

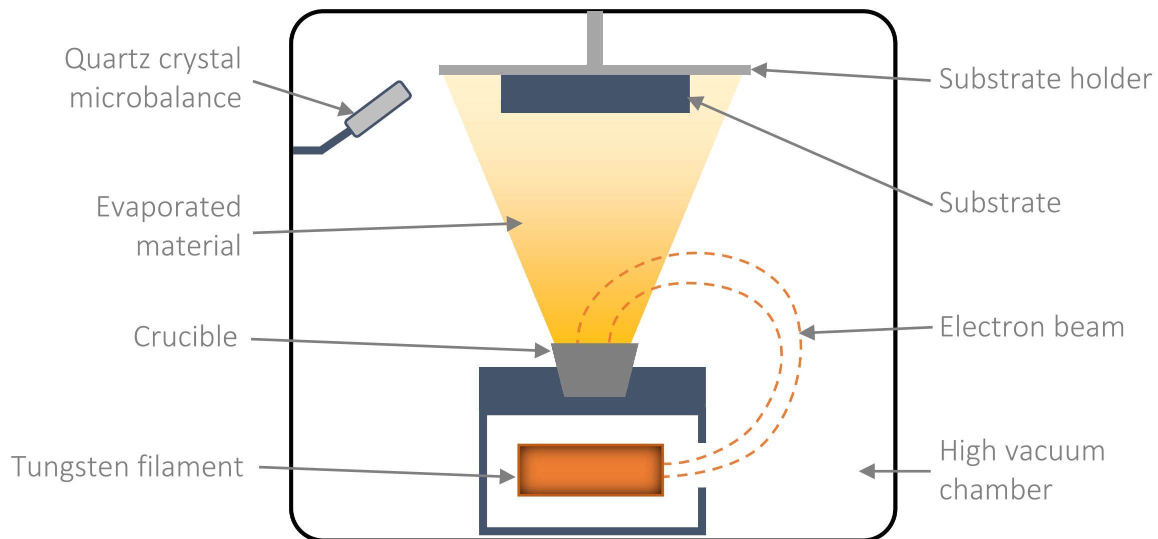

Figure 3.3 Scheme of an electron beam evaporation system. The substrate is hold in holder in face down position over the crucible. Material evaporates due to heating cause by electron beam focused on it, deposition rate is measured by the quartz crystal microbalance.

energy electrons strike the metal, they lose their kinetic energy, causing the heating of the target material.

In order to have a good homogeneous film, scattering of electrons as well as evaporated material should be as low as possible. This is directly related to the chamber pressure; lower the chamber pressure, higher is the mean free path for particle, so it is required to have very low pressure for good deposition of material. In addition to pressure the deposition rate is also important. To have a good metal film it is better to go with minimum deposition rate. Rate of deposition of material, in the system used for this work, is measured using quartz crystal microbalance, which works based on the change in frequency depending on the mass per unit area being deposited. Evaporation rate of the material can be controlled by the power of the beam, i.e. the kinetic energy of the electrons, and its spot size, which allows to spread the energy on a smaller or a larger area.

3.2 Substrates

As graphene is just a monolayer of carbon atoms, it is not possible that device can be made on standalone graphene sheet. So to have some feasible device using graphene, it is required that it should be deposited over some substrate. As such it has been noticed that the substrate underneath has very great impact on the overall performance of graphene devices [87], so it required that the substrate use as support or even as a part of device, is carefully selected and prepared. Most of the research groups use the SiO_2/Si substrate with 300 nm or 90 nm thick SiO_2 oxide on top, because it produces optimal contrast with graphene, as mentioned in section 1.4. In this work we have used SiO_2/Si substrate with 300 nm thick SiO_2 on top, for reference device fabrication. While the main substrate of interest and under investigation had STO as the top oxide layer.

3.2.1 SiO_2/Si substrate

Highly doped silicon wafer with 300 nm thick layer of SiO_2 is used for this work. Highly doped Si is required to have a good conducting material to be used as back gate electrode. SiO_2 is generally formed by thermal oxidation, which results in oxide layer on both sides of the wafer, but as in our case we need to use this substrate as back gate, a good conducting back side is required. To do so the oxide layer from the back can be etched away using hydrogen fluoride acid solution. After that to have a good conductive back contact and to stop Si to oxidise in atmosphere, silver was deposited on back surface through electron beam evaporation. In order to have good bonding between the etched silicon surface and the silver back gate, two thin adhesion layers of chromium and antimony can be deposited. Once the deposition of metal is done, the wafer can be cut in a required size of chips using any wafer dicing method. This is the standard method followed in Si wafer production and we received the substrates at this stage, with some protective coating, to ensure no damage during handling the chips.

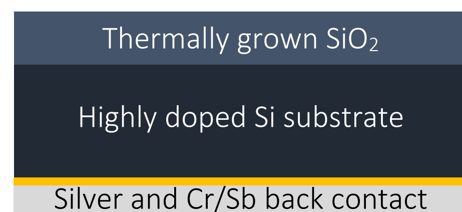

Figure 3.4 Illustrative SiO_2/Si substrate structure

In order to facilitate the alignments for the subsequent devices fabrication steps particularly for EBL, some reference points are required on the substrate. This can be done by making a grid, having cross shape markers separated by a distance of 80 μm in both horizontal and vertical directions. For this, first PMMA was coated on the surface and then exposed to an electron beam which makes the required shape on the resist. After this, the sample was developed using developer solution, thus the pattern was created over the substrate and this resist film now acts as a mask for deposition of metal. For this, we deposited 20 nm of titanium followed by 50 nm of gold, using electron beam evaporator. At the end of metal deposition an acetone bath was required for complete removal of resist and excess metal deposited (generally referred to as lift-off). By this way the obtained grid can be used for precisely positioning of the structures during the fabrication steps.

3.2.2 STO substrate

The main work for this thesis is to evaluate high-κ materials as gate insulator for GFETs, so this was the main substrate which was used to make such devices. STO itself is an insulating material, so it is not possible to have devices as can be prepared on SiO_2/Si substrate. To make such thing possible it is necessary to realise electrical contact as the back gate, so it is required to deposit some conductive material below STO (gate insulating layer). In our case this was done by using lanthanum strontium manganite (LSMO), which can be conductive when used in correct composition. For this application the composition used was $La_{0.67}Sr_{0.33}MnO_3$, one which makes the material a metallic and ferromagnetic with the highest transition temperature [88]. The reason for using LSMO as conductive material rather than any metal is due to its close lattice match with STO. This makes it easy to grow a crystalline material, which is must for GFETs to reduce the loss of mobility, as the grain boundaries acts as scattering centres for the charge carriers. Now both LSMO and STO have different lattice parameters compared to Si, so Si substrate cannot be used for the sample preparation. Generally, for LSMO thin films, STO is used as a substrate, so here in this work also STO substrates were used to grow LSMO and STO top layer.

STO substrates for the device fabrication were prepared at the Polifab lab by M. Asa. STO (100) substrates were used for the growth of LSMO and final STO layers. Both layers were grown with pulsed laser deposition (PLD) method. The substrate temperature during growth was 730 °C and the chamber was having 0.29 mbar of oxygen pressure. The laser beam was produced by a quadrupled Nd:YAG laser (266 nm). Before starting deposition substrate was pre-annealed for 30 min at 730 °C and 0.29 mbar of oxygen pressure, so that it will reach to the optimal condition for deposition. LSMO layer was deposited at 78 mW (34 mJ/pulse) of laser power with deposition rate of 1.10 nm/min (with final thickness about 50 nm). While for the STO top layer, the laser power was 50 mW (25 mJ/pulse) and deposition rate of 1.68 nm/min (with final thickness about 150 nm). After deposition sample was annealed at 400 °C temperature and about 500 mbar

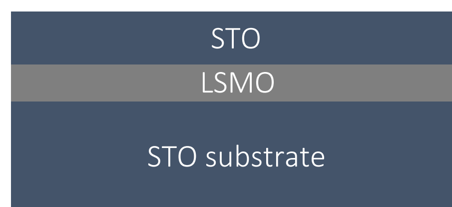

Figure 3.5 Illustrative STO sample structure

oxygen pressure for 30 min. This was followed by controlled cooling of sample, cooled to room temperature in 30 min in PLD chamber at 500 mbar oxygen pressure. Process parameters were optimised for best recipe to get perfect crystalline material growth. The growth rates of the materials have been calibrated prior to the growth of the materials since RHEED oscillations cannot be used due to high oxygen pressure required for this process. Once the samples were grown, various tests were conducted to confirm the crystalline growth and to measure the thickness of both layers.

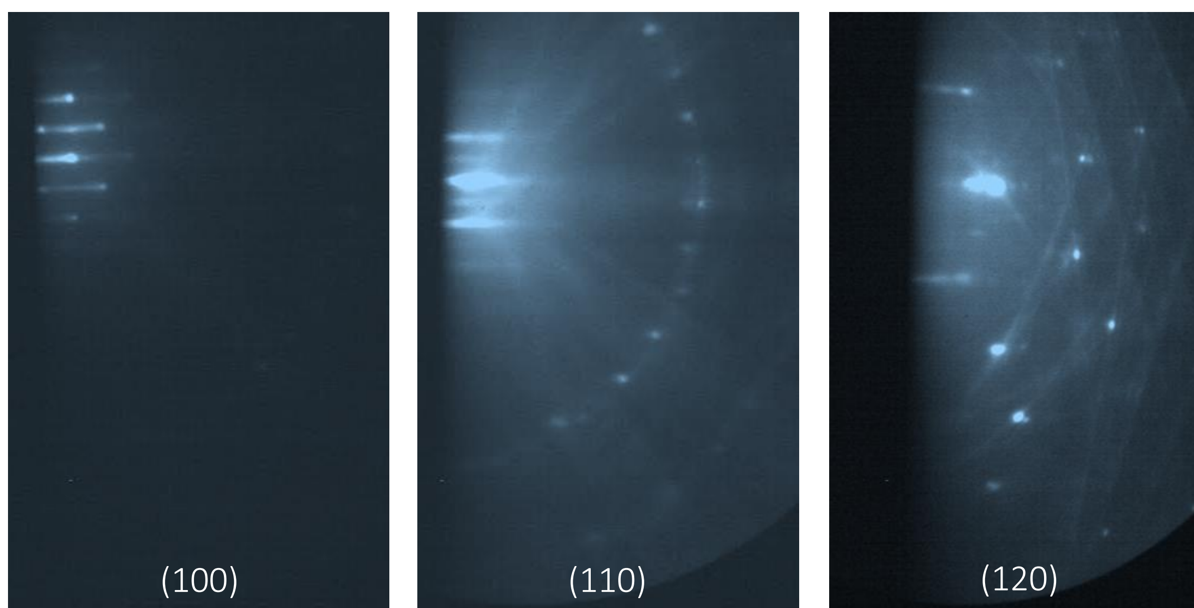

Figure 3.6 RHEED patterns after the STO and LSMO layers grown on the STO (100) substrate. (Image taken by M. Asa at Polifab, Politecnico di Milano)

To confirm crystalline growth, RHEED analysis was performed of the prepared samples by M. Asa at Polifab lab, which can be seen in Figure 3.6. The main specular spot is very intense compared to the other side spots, which is the typical signature of TiO_2 terminated STO [89]. There are clear two dimensional spots, but also some 2D streaks are present. The latter may attribute to the scattering of the RHEED beam from the steps at the surface or due to surface roughness. But it is clear that the grown layers had crystalline structures.

X-ray diffraction (XRD) analysis was performed with the help from D. Chrastina, at L-NESS, in order to further check the crystallinity of the samples. Measurements were performed using PANalytical X'Pert PRO high-resolution diffractometer, with a hybrid monochromator featuring a parabolic mirror and two-bounce channel-cut Ge crystals in front of the x-ray tube, which was configured in the line focus geometry. The measurements were done in Triple axis mode, as there were three crystals in the beam path (monochromator, sample, and analyser) and all in the Bragg condition

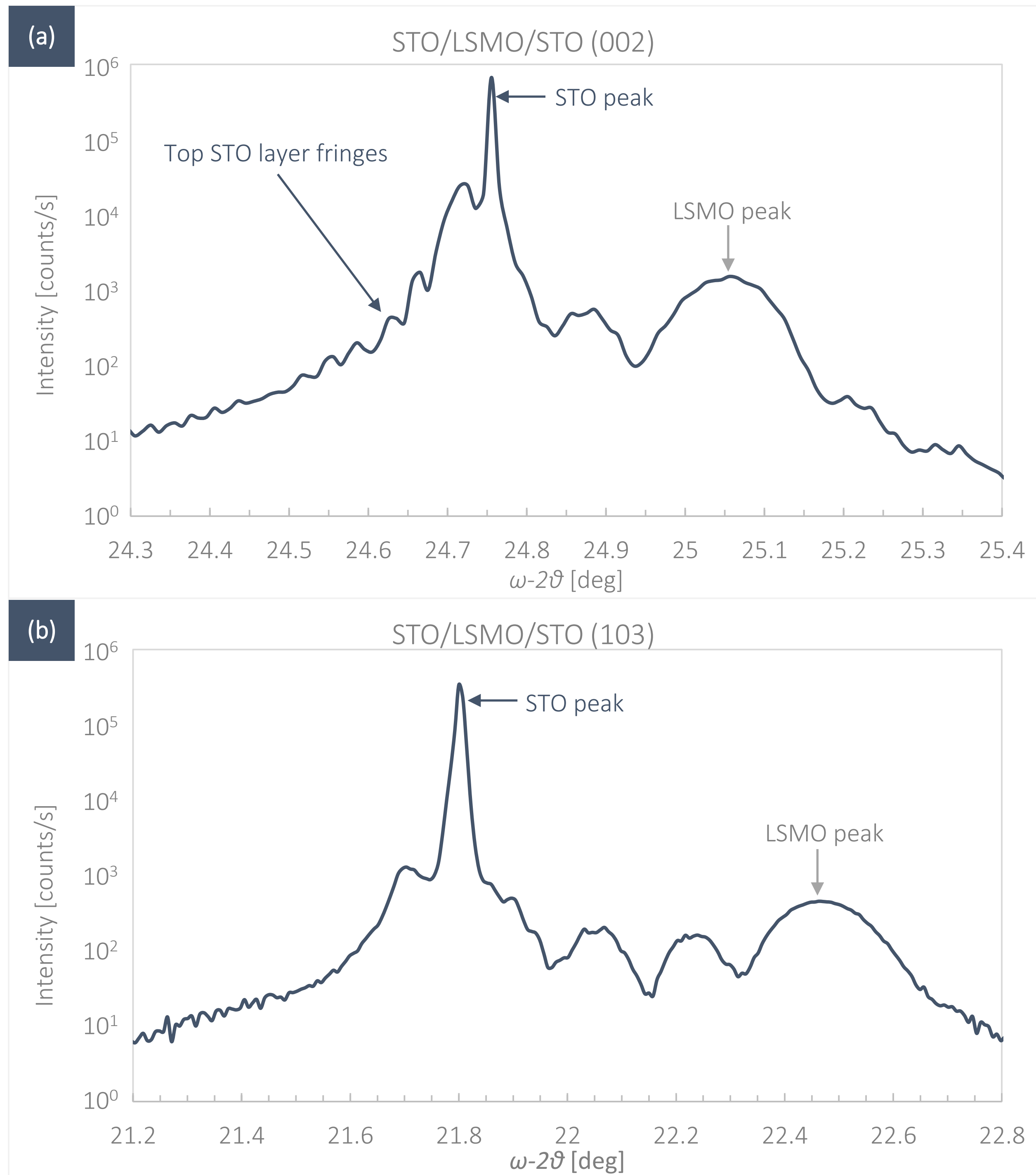

Figure 3.7 XRD ω-2ϑ scan for an STO sample. (a) ω-2ϑ scan for (002) plane of STO, symmetric reflection. (b) ω-2ϑ scan for (103) plane of STO, asymmetric reflection. In both the cases the maximum intensity peak corresponds to the STO substrate, while the other peak on right is related to LSMO. And the fringes (showing over the peaks of LSMO) are related to the top STO layer (Measurement was done with help from D. Chrastina, L-NESS).

in order to detect the signals. This particular kind of operation mode is used for high-resolution measurements, in which a three-bounce monochromator (as an analyser crystal) is placed in front

of the Xe proportional x-ray detector. In this XRD measurements both symmetric (002) and asymmetric (103) reflections were measured to better understand the crystalline growth of the material. For this the Cu $K\alpha_1$ x-ray line, having wavelength (λ) of 0.1540562 nm, was used. Figure 3.7, shows the *ω-2ϑ* scans for (002) and (103) planes of an STO substrate. Here *ω* is the incident angle and *2ϑ* is the scattering angle. The maximum intensity peak at the center of scan is related to the STO substrate, while the other peak at right (with maximum intensity) is related to LSMO. Both these peaks are related to Bragg condition, and because of that only they have highest intensity among all other peaks. Fringes over the peaks of LSMO is related to top STO layer. From the distance between peaks of STO top layer and of LSMO, using Bragg's law, the thickness of the layers can be found. Particularity for (002) scan the perpendicular component of the scattering vector (which is also known as out of plane component - $q_\perp$), should be used to calculate the thickness of the layers. Form the results obtained from the measurements, the thicknesses of the layers were calculated, which turns out to be 160nm for top STO layer, while 38.86 nm for LSMO layer, which is more or less the same as observed under SEM. But still this can be just used as an indicative method for thickness measurement, as it was hard to exactly locate the peaks.

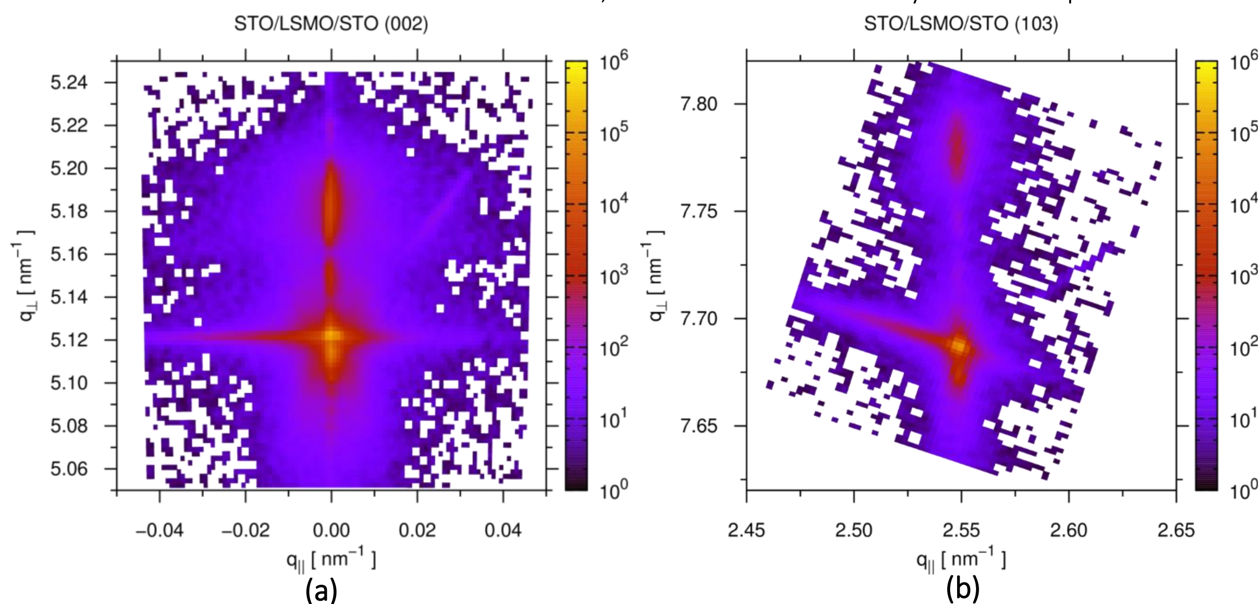

Figure 3.8 Reciprocal space maps (RSMs) of (002) and (103) reflection peaks. In both images the bottom dark region is related to the peak of STO, while the top dark region is related to LSMO. The side color-bar shows the intensity [counts/s] measured at each point (Measurement was done with help from D. Chrastina, L-NESS).

As such the reciprocal space maps (RSMs) are useful to get the lattice parameters and the atomic positions, but it can also be used to check the distortion or defects in the grown layers. Figure 3.8 shows the two RSMs done for the STO substrates, one for (002) plane for the symmetric reflection and the other for (103) plane for the asymmetric reflection. In both cases, in plane scattering vector ($q_{||}$) remains same for STO and LSMO, which means that the grown layers do have lattice match and are not distorted in the plane, confirming a good crystalline growth.

Moreover, to confirm the thickness and homogeneity of material a cross-section SEM images were also taken which is shown in Figure 3.9. From this figure it can be concluded that thickness is similar over entire surface of sample, i.e., layers being deposited have homogeneity in the thickness. Also the AFM characterisation was done to check the surface roughness of the grown materials, which is shown in Figure 3.10. The average surface roughness (root mean square - RMS) measured was in the range of 0.3 nm to 0.5 nm.

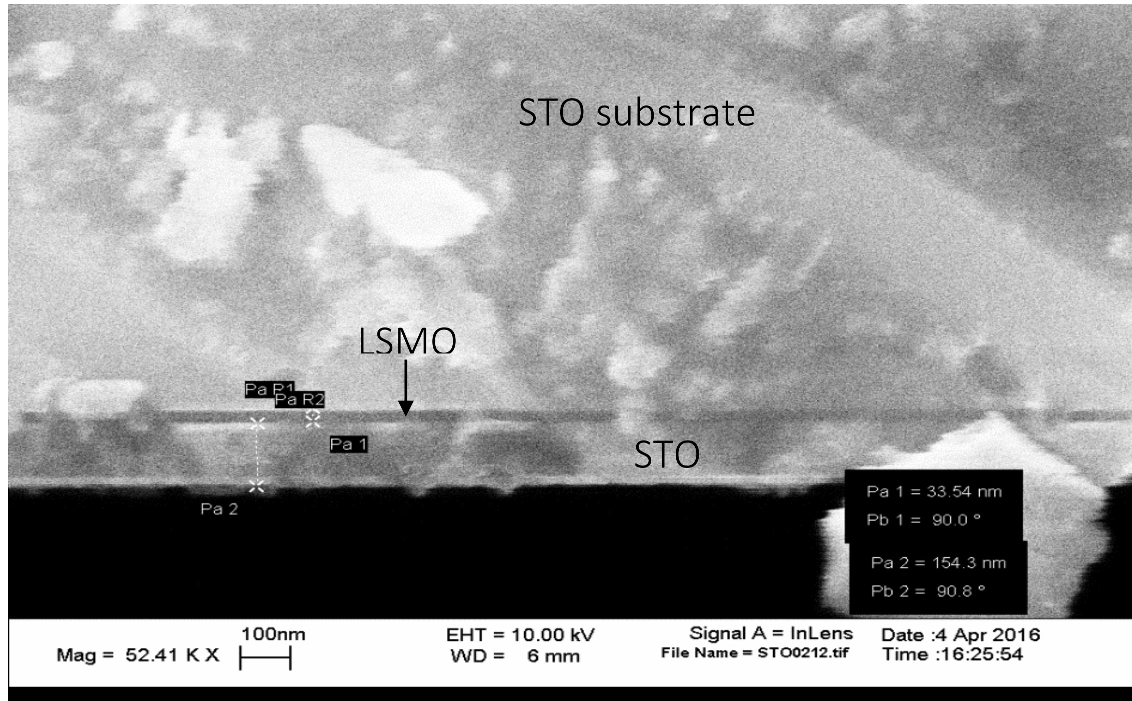

Figure 3.9 SEM Cross-section image showing thickness of STO and LSMO layers grown on the STO (100) substrate. (Image taken by M. Asa at Polifab, Politecnico di Milano)

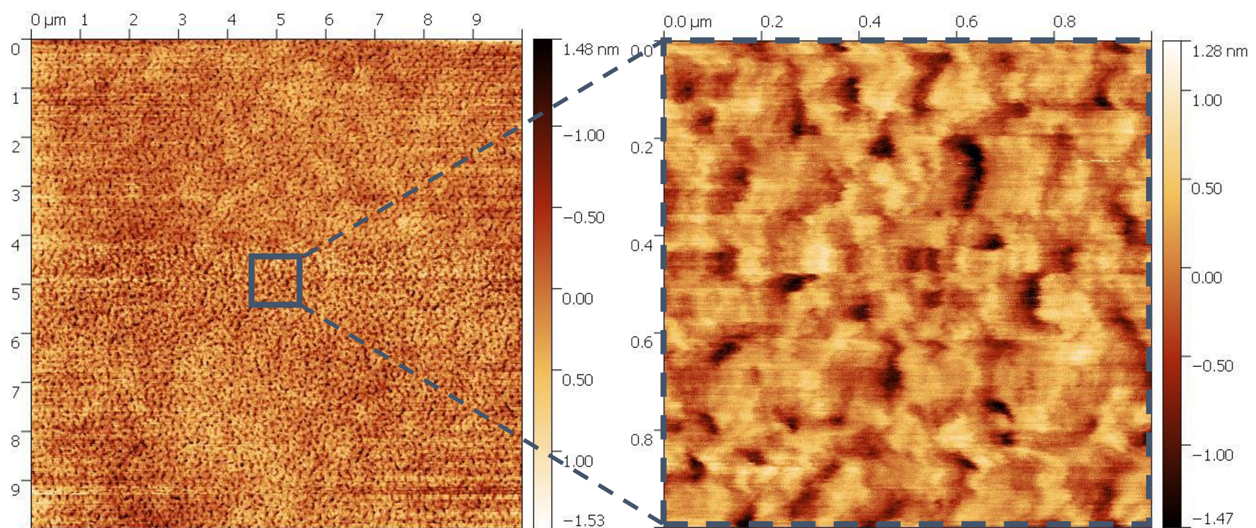

Figure 3.10 AFM images after STO and LSMO layers grown on the STO (100) substrate. The average roughness (RSM) value measure was in the range of 0.3 nm to 0.5 nm. (Image taken by M. Asa at Polifab, Politecnico di Milano)

3.3 Graphene transfer

In this section CVD grown graphene transfer procedure is described. This method has been optimized by M. Fiocco at L-NESS, form the first ever demonstration of such kind of process [51]. We got our monolayer CVD graphene on Cu foil (60 mm X 40 mm and 25 µm thick) from Graphenea.

As it was CVD grown graphene, we had graphene on both sides of the foil, so it was needed to remove graphene from one side. Generally, it is mentioned by the supplier which side has good graphene. As if graphene from one sides of foil is not removed then after Cu is etched, graphene from either side may stick to each other and will not have monolayer of graphene. To remove graphene from one side, it is required that the side with good graphene should be coated with something to prevent it from damage. Generally, this is done by coating it with PMMA, which also act as support for graphene throughout the process of transfer.

First the Cu foil with good side of graphene on top was placed on the Si substrate (which will act as support for the Cu foil for coating process). Then to make sure that it will stay on the substrate during spin coating, it was taped by scotch tape. After that, the substrate was placed in the spin coater and covered with 2 layers of PMMA (950k MW - diluted in 15% chlorobenzene solvent). Coating was done at 6500 rpm for 30 sec and will have approximately thickness of 100 nm of coating. Each layer of PMMA coating was followed by a baking on a hot plate at 160 °C for 5 min.

To remove graphene from the other side, it is required to flip the sheet. So now removing the tape and placing the foil other way so that the uncoated side is now on the top and again to make sure that the Cu foil remains on its place, it was taped by the scotch tape. By O_2 plasma in a barrel reactor or a RIE, the graphene from the Cu foil can be removed. The etching was done by oxygen gas assisted by plasma. Parameters set for the RIE were 150 ml/min of oxygen flow and 100 W of power for plasma for 4 min. To be sure that there were no impurities present on the back side of the foil (oxygen plasma itself might not remove completely backside graphene and residues) the foil was washed with the solution of hydrochloric acid (HCl), hydrogen peroxide (H_2O_2) and water in the ratio of 1:1:10 respectively. Each graphene on Cu flake was first left on top of the solution for 30 secs and then dipped in the solution and then put in deionized water for 2 min. After a couple of immersions, the sample was dipped into deionized water to remove residues from the solution.

After cleaning, the foil can be placed in the Cu etchant solution to etch Cu. For Cu etching ferric chloride ($FeCl_3$) solution was used. Solution was prepared from diluting powder of $FeCl_3$ in water and making concentration of 0.25M $FeCL_3$. As it was made from powdered $FeCl_3$ and can be reused many times, it may contain some particles which should be removed to have residue free transferred graphene. This was done by filtering the solution by 1-5 µm pore size paper filter or by 0.2 - 1 µm pore size filters using pump. Once the solution is filtered, process for Cu etching can

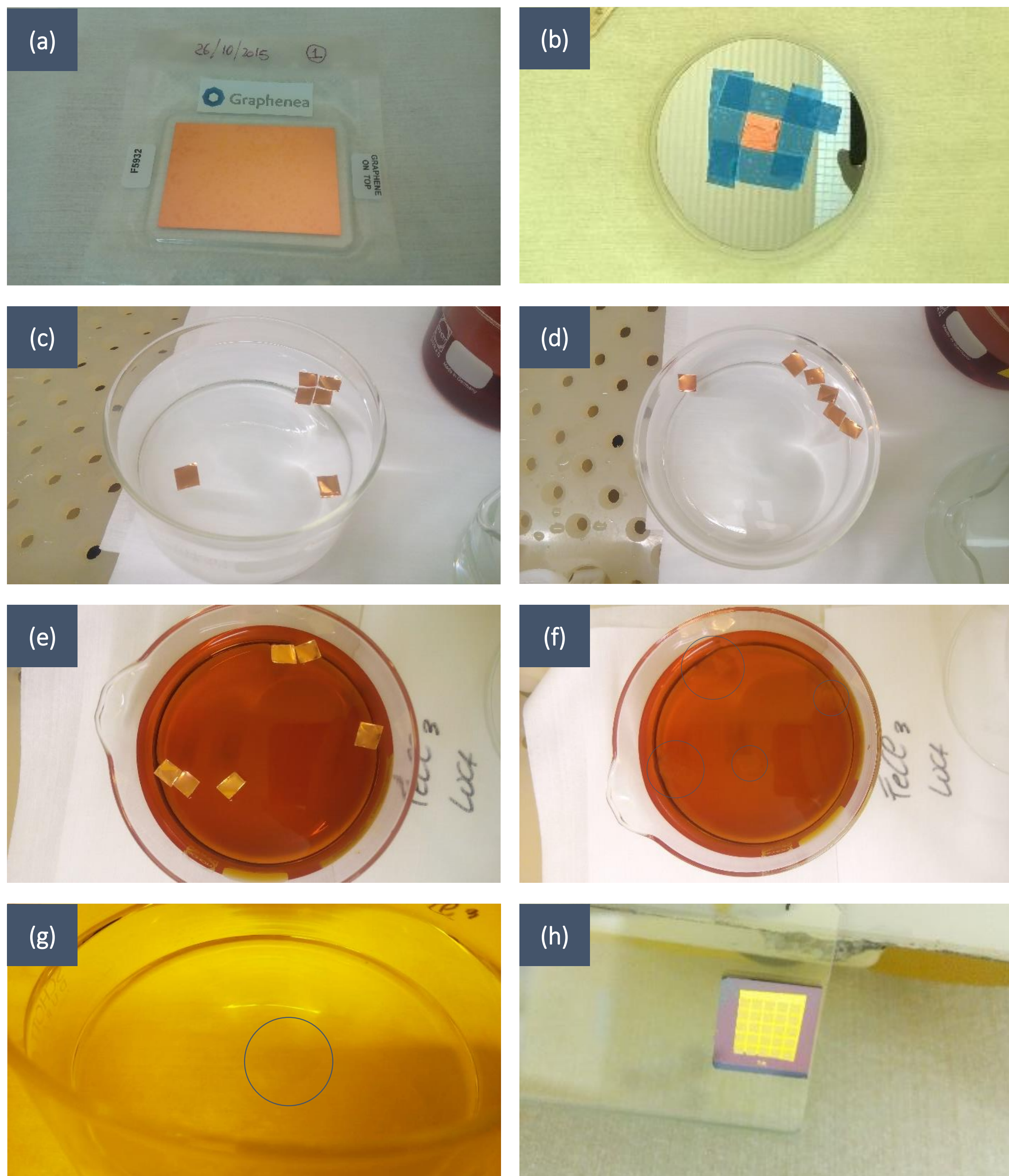

Figure 3.11 Graphene transfer steps. (a) As received CVD graphene on Cu. (b) Graphene on Cu foil placed on Si wafer using scotch tape for PMMA coating and RIE. (c) Cleaning of foils in acid solution. (d) Washing of foils in deionized water. (e) Graphene on Cu foil, after cleaning placed in $FeCl_3$ for Cu etching. (f) After Cu foil is etched away (it is hard to recognize graphene, for ease to eyes it has been circled where those flakes are. (g) Graphene with PMMA on top, placed in deionized water for etchant removal (in this case it is even more difficult to see the flakes, which is marked by circle to recognize it). (h) Graphene transferred to the final substrate, and put at some inclination for drying.

such that it floats on it having graphene and PMMA on the top and Cu in contact with the solution. Generally, within 1 hour Cu be will etched away completely as its thickness was not large. However, to be sure it was kept for 2-3 hours in the solution. Longer etching times should be avoided because $FeCl_3$ can damage graphene.

After this step, transparent film of graphene and PMMA floats over the solution. This film was then removed from the solution with help of a dummy sample, which was just a Si substrate of somewhat larger size. The film was then transferred to deionized water for 15 min and again moved to other deionised water for 15 min to ensure that there is no etching solution left with graphene. Once clean in water, the film was placed in the solution of HCl, H_2O_2 and water in the ratio of 1:1:10 respectively, for final cleaning. We noticed that placing the film for 3-5 min in the solution will yield good quality of graphene film, free from the impurities of the iron and copper. Once this is done it was placed in the deionised water overnight to make it completely free from any kind of etching solution.

Fishing was the last step for transferring graphene on the final substrate. Very gently and carefully substrate was moved below the film and then lifted so that the film sticks to it. Now it was placed somewhat inclined overnight to dry as it is not advisable to dry it by nitrogen gun as the film may flow away with gas. Placing it at inclination makes the water to flow away by gravitational force, causing least possible stress over graphene sheet. After natural drying it was placed on the hot plate at 160 ^{o}C for 5min. This will help graphene to stick to the substrate as heating will soften the PMMA and due to its weight it will force graphene on the substrate resulting in better bonding.

As the graphene sheet is transferred to the final substrate, PMMA support is no more required. To remove the protective PMMA coating from the top, sample was placed in NEP for 4 hours. After that it was placed in isopropanol to remove residues of NEP and PMMA. If Acetone alone is used than it may possible that due to evaporation of acetone some PMMA residues may stick to graphene and will not yield good quality of graphene transfer. Once cleaned with isopropanol it was dried with help of nitrogen gas.

After transferring graphene on the substrate, it is required to check its quality for final application. This can be done in various ways, like as mentioned earlier in the section 1.4, optical observation gives a quick idea about the quality of graphene. But as for the STO substrates the optical contrast is very poor for graphene so it is better to also perform some other tests to verify the quality of graphene. AFM or STM scan can be done, but they are too much time consuming. Alternatively, Raman spectroscopy is a non-destructive, fast and reliable tool to assess the quality of graphene, and even can be used to distinguish monolayer from multilayer graphene.

Very good and extensive study of Raman spectroscopy for graphene has been reported in many articles [41-43]. Micro-Raman spectroscopy measurements for fabricated samples were performed using Renishaw Invia Raman spectrometer, with excitation line 514.5 nm produced by

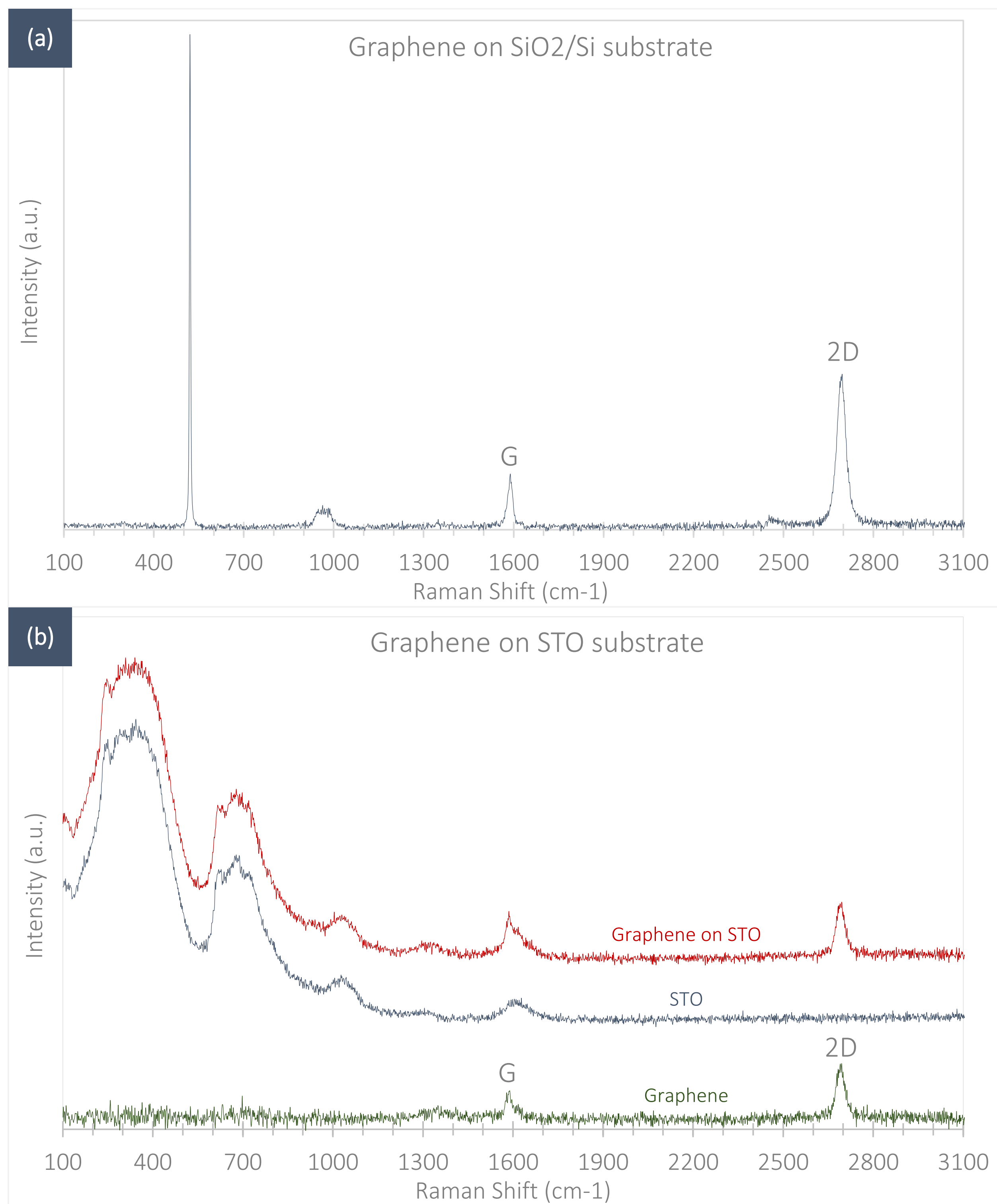

Figure 3.12 Raman spectrum of CVD grown graphene transferred to different substrates. (a) Raman spectrum of graphene on SiO_2/Si substrate. (b) Raman spectrum of graphene on STO substrate. In both cases the 2D peak has more or less twice the intensity than the G peak, which indicates the presence of good quality monolayer graphene. There is no D peak so transferred graphene does not have noticeable distortion or defects (Measurement was done with help from V. Russo, Nanolab).

from Dr. V. Russo at NanoLab. Measurements were done in two steps; first for the graphene transferred on SiO_2/Si substrate and then for graphene on STO substrate. These two different tests were performed to compare the transferred graphene on different substrates. Figure 3.12 shows the Raman spectra of CVD grown graphene transferred on different substrates using the process described above. As it can be seen for both the cases there is a very high intensity of 2D peak compared to G peak, which is an indication of monolayer graphene. No presence of D peak, which generally appears around 1350 cm^{-1} of Raman shift, means the transferred graphene is free from distortion and defects. The G peak was at ~1586 cm^{-1} and 2D peak at ~2695 cm^{-1}, which are the most observed values for a good quality graphene on any substrate. In case of graphene on STO, strangely the STO substrate also shown a peak in the range of G peak of graphene, so to distinguee the G peak of graphene from the STO peak, normalised Raman spectrum of STO substrate is subtracted from the Raman spectrum of graphene on STO substrate, as shown in Figure 3.12 (b).

3.4 Device fabrication

In this work different samples with different gate channel lengths were fabricated for better understanding of effectiveness of the gate oxide on GFETs performance. All devices were fabricated following the same procedures. Starting with the substrate cleaning, by acetone bath for 2-3 hours and then rinsed with isopropanol. This step is required to make sure that there is no dirt on the surface, which may affect the device performance and can not be removed once the graphene sheet is transferred over it. Once cleaning is done, alignment markers were prepared, which are useful for the subsequent processes. After this graphene was transferred over it, and then the supporting PMMA layer for transfer was removed using NEP (organic solvent) followed by isopropanol rinse.

Once graphene is transferred, most of the device fabrication steps are related to standard lithography steps. So for that a CAD file is required, which contains all the designs required for the EBL systems. As the devices were made in sequential steps, design file was created for each steps accordingly. All the devices fabricated for this work had the same design channel width of 5 µm and the entire graphene channel had the length of 200 µm. For electrodes the width selected was 2 µm and were placed at 1 µm or 2 µm apart from each other, to have different gate channel lengths. As the measurement setup had 12 micro probes, there were 12 electrodes placed over the graphene channel. Here graphene channel and the electrodes were fabricated in different steps. For EBL, when working with different sizes of a device, different writing fields, different sizes of the spot and different doses for the electron beam need to be defined to have better control over the exposure. For example, for contacts 100 µm X 100 µm writing field should be used as they have small feature size, while for making electrode connection and pads for probe landing, bigger writing filed of 1000 µm X 1000 µm can be used to speed up the process and as they do not have very small feature size. When using different writing fields, it is possibility that the two exposures may be slightly misaligned, which can be compensated by making slight overlap between two designs for exposure.

As we had used CVD grown graphene, it is likely possible to have some defects and contamination from the growth process itself or during transfer process. To make sure that the best quality graphene available is used, a quick look under optical microscope is done. By this some regions which did not have any residues or defects were selected. As mentioned in section 1.4, for graphene on STO substrate, the optical contrast is not so good, so it is hard to say confidently that the selected area is good. But still by this method some regions with big defects or residues can easily be recognised, and by this way we can make sure that the devices fabricated are not over such regions.

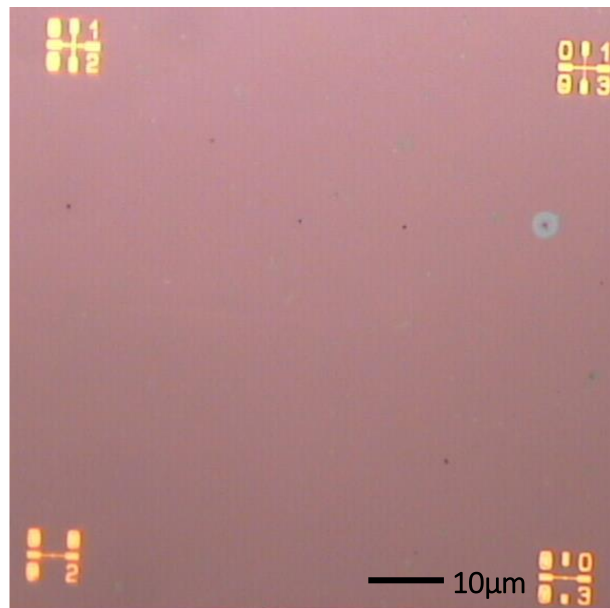

Figure 3.13 Optical microscope image of graphene on STO substrate. As the transferred graphene was of good quality, only some very small residues were present on it. But there was not any area without graphene. As such the size of fabricated devices is very small, it is easy to make sure that the devices are not fabricated over tiny residue particles.

Now as we had selected the best regions to make graphene and design files were also made, so actual device fabrication process can be done. The devices made have back gated configuration, means gate electrode at the bottom of the channel material and source and drain contacts on the top of the channel. So the first thing is to make graphene channel from the sheet of graphene, which is covering almost entire sample, and this also makes sure that the electrodes do not get shorted through graphene with each other. This is done with help of RIE. For that first graphene was coated with 3 layers of PMMA (950k MW - diluted in 15% chlorobenzene solvent) by spin coating method, which is performed at 6500 rpm for 30 sec followed by hot plate baking at 160 °C for 5 min after each layer of coating. After PMMA coating, EBL was done to define the channel of graphene. Here as the PMMA is used as resist, which is a positive resist, the area which is required to be removed needs to be exposed, and in our case it is the entire region except the channel. So in EBL entire region 1000 µm X 1000 µm except the channel region was exposed. After e-beam exposure the sample was developed in developer solution for 90 sec and washed in isopropanol for 60 sec. By this the PMMA forms a mask over graphene, which will act as protecting

mask during the RIE. RIE was done as described in section 3.1.2. After RIE, the sample was placed in NEP for 3-4 hours for removal of residual PMMA over the channel.

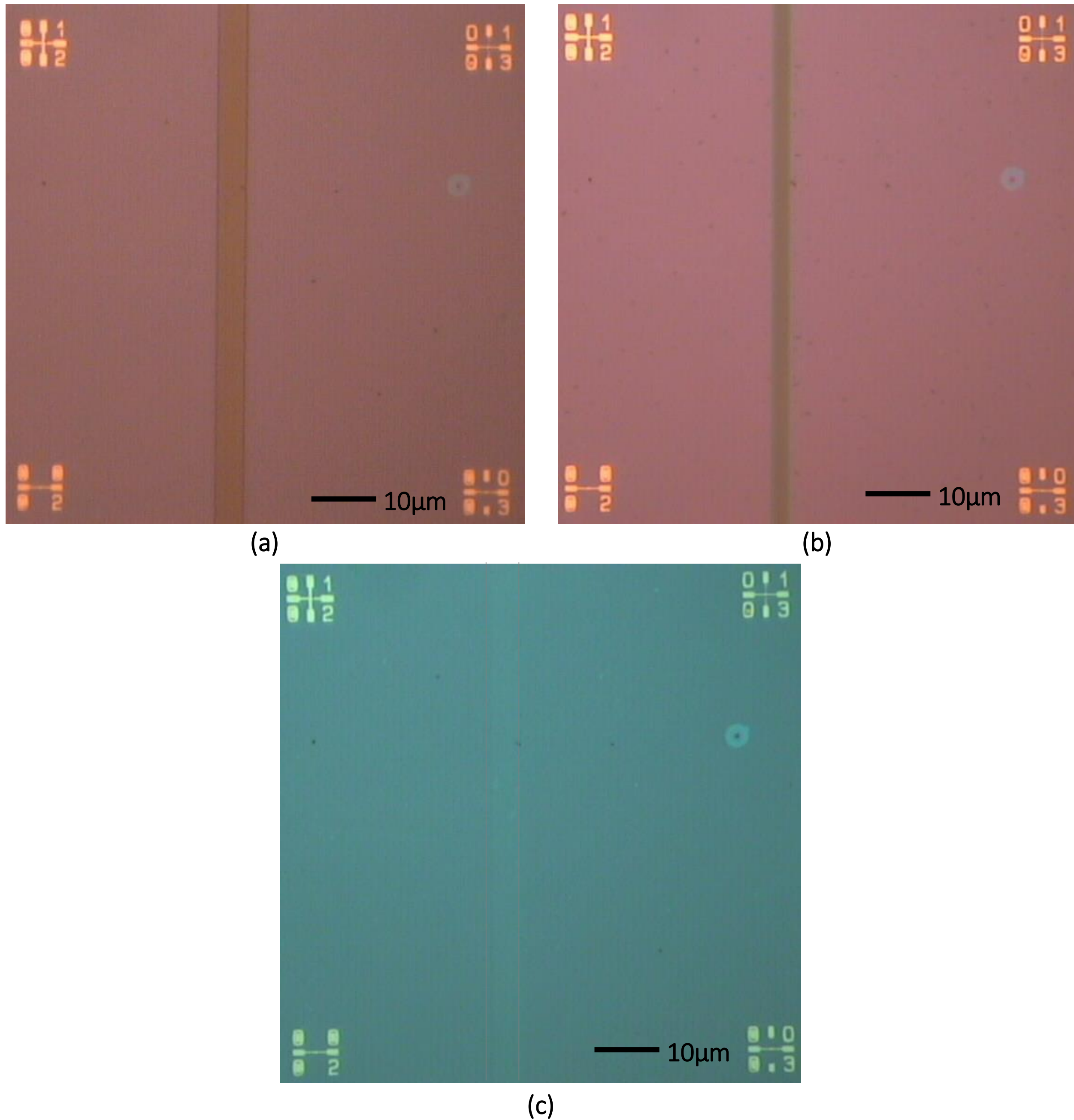

Figure 3.14 Graphene channel observed under optical microscope after different steps. (a) Graphene channel covered with PMMA after developing the exposed sample. (b) Graphene channel covered with PMMA after RIE. (c) Graphene channel after PMMA removal. Image (c) was taken with some light filter in optical microscope to have better contrast for graphene.

Final steps for the device fabrication were to make contacts and external connection for electrical characterisation of devices. For this, EBL process followed by metal deposition by electron beam evaporator was used. As resist for EBL process, two different compositions of PMMA were used.

First a layer with PMMA having 200k MW and diluted in 35% chlorobenzene solvent (low molecular weight) was spin coated followed by a layer of PMMA having 950k MW and diluted in 25% chlorobenzene solvent (higher molecular weight). For both layers spin coating was performed at 6500 rpm for 30 sec followed by baking on hot plate at 160 °C for 5 min. Here two different PMMA layers were used to help lift-off process after metal deposition. During exposure, the lower PMMA layer due to its low molecular weight will easily break in very small chains and because of that during development process it will create the undercut for the top resist. By this way the organic solvent can move to the PMMA layers after metal deposition and can dissolve it. After PMMA layers were coated, sample was moved to EBL for exposure. Then it was developed in developer solution for 90 sec and washed in isopropanol for 60 sec. Now there is a mask of PMMA, which can be used for contacts fabrication from metal deposited. In these samples we used 100 nm of gold as contacts, which was deposited using electron beam evaporation. During evaporation the chamber pressure was around 3.6 x 10^{-6} mbar, and the deposition rate was 0.5 Å/sec for first 20 nm and then 1 Å/sec for rest of the material. After metal deposition sample was placed in acetone for 4 hours for lift-off process and then rinsed with isopropanol. It was observed that before starting the measurement, if the samples were placed in NEP for 5-6 hours, it helps in removing residues of PMMA remained on the graphene channel, and better electrical performance was measured. So at last after NEP bath, the sample was washed with isopropanol.

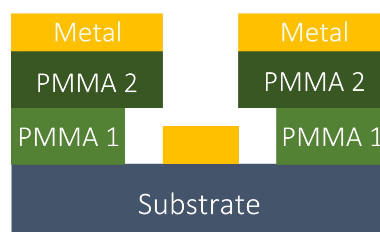

Figure 3.15 Different resist used to have undercut for easy lift-off after metal deposition.

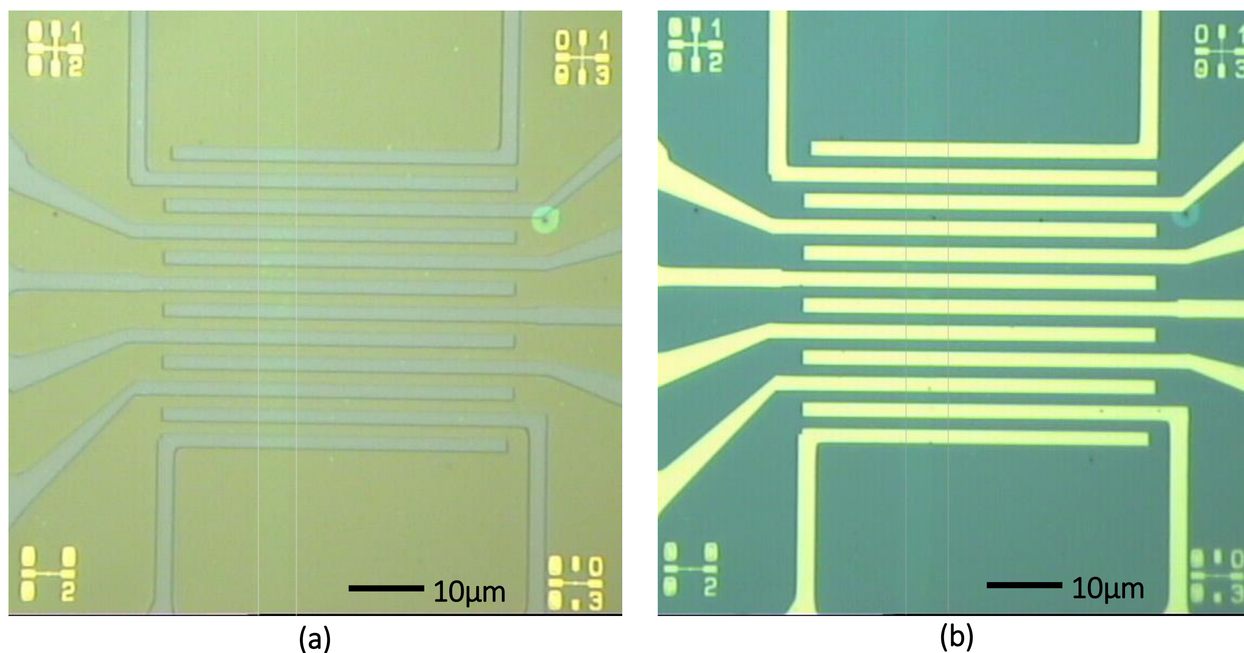

Figure 3.16 Optical microscope image of electrodes. (a) Image taken after exposed sample being developed, showing developed regions for metal deposition and graphene channel underneath. (b) Image showing electrodes after lift-off and graphene channel.

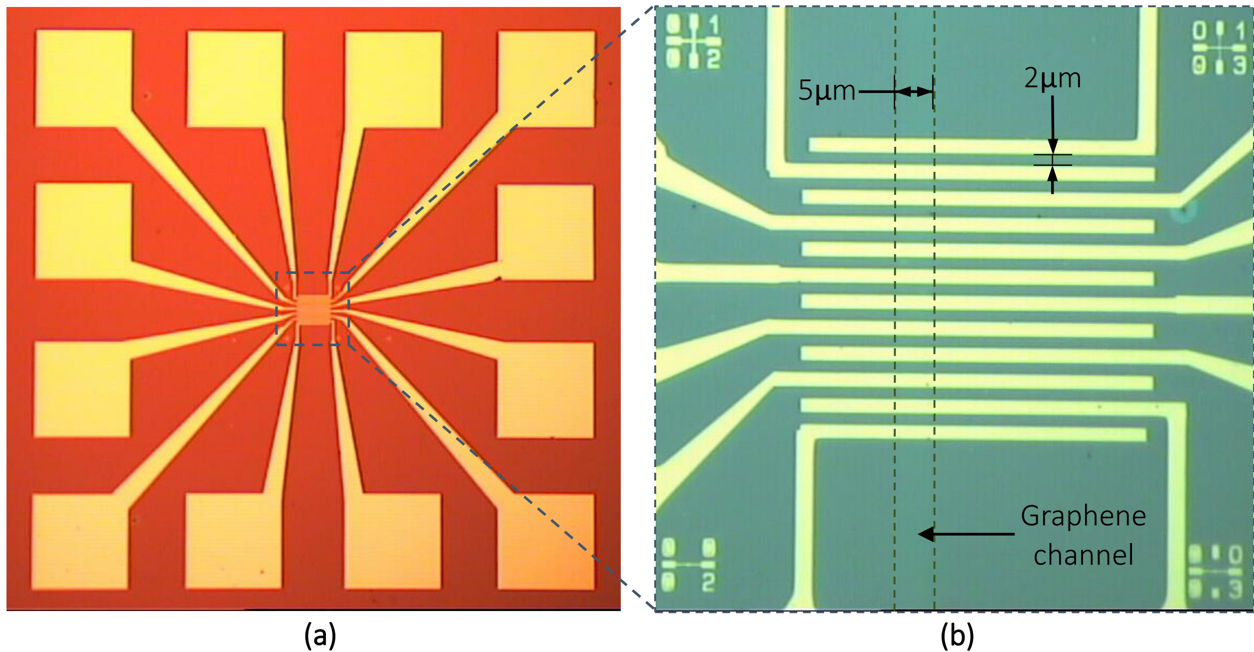

Figure 3.17 Optical microscope image of fabricated device structure. (a) Image showing entire device structure. Probes to connect device with external measuring units were placed on the square gold pads. (b) Optical microscope image showing different dimensions of the fabricated devices.

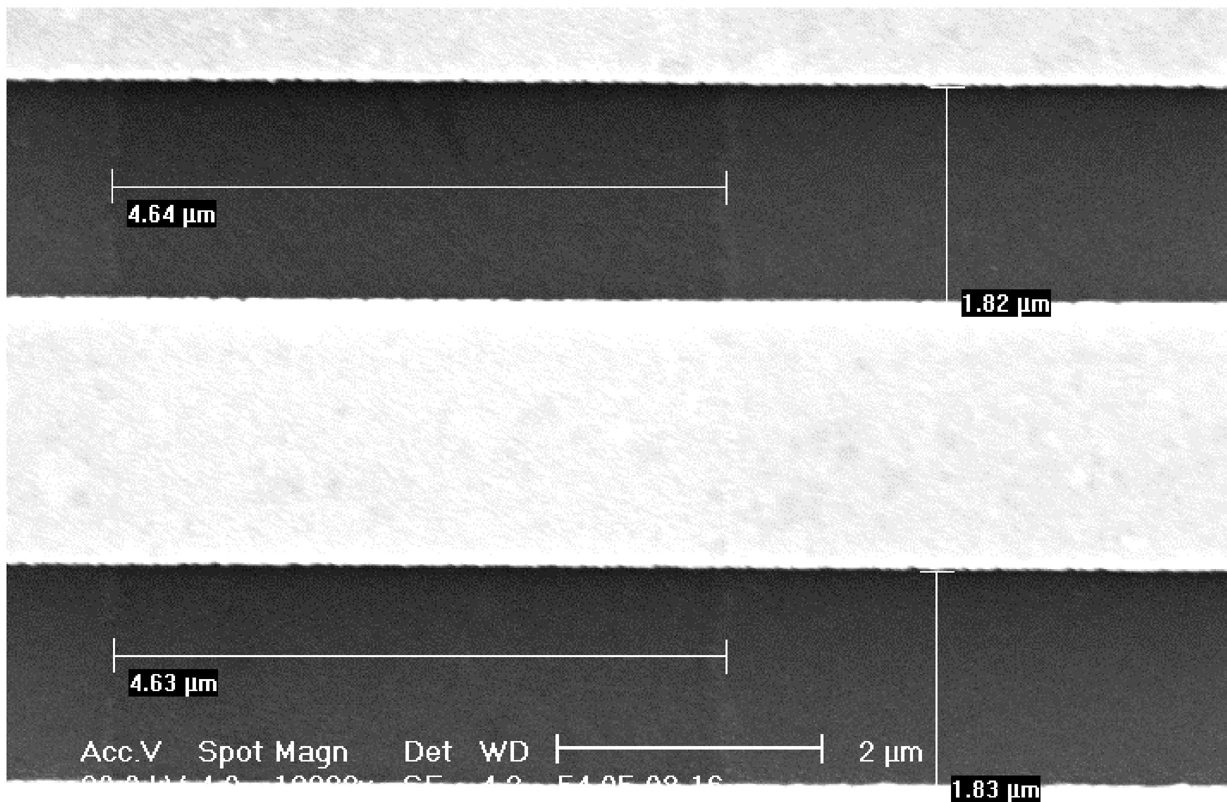

Figure 3.18 SEM image of the device, showing actual dimensions of the graphene channel.

In this work STO substrates with dimensions of 5 mm X 5 mm and 10 mm X 10 mm were used. For smaller substrate there were 9 such structures made while on the bigger substrate there were 36 structures prepared on a single chip. Entire structure for the devices is shown in Figure 3.17 (a). As such the dimensions mentioned in Figure 3.17 (b), are the designed dimensions, while actual dimensions were measured using SEM, shown in Figure 3.18. Change in dimensions is mainly because of the proximity effect, which makes the exposed area slightly larger than the design dimensions.

As the STO substrate used, does not have good electrical conductivity, but to make the device work in back gated configuration, it is required to have access to the LSMO layer (which has good electrical conductivity to be used as gate electrode) deposited between STO substrate and top STO layer. To do so, some scratches far from the devices and near the edges of the substrates were made. Then the substrate was glued on the Cu thin plate using silver paste, which was also placed over the scratches to make an electrical connection between the LSMO layer and the Cu plate. Ag paste was cured at 120 °C for 1 hour to evaporate the solvents and to have good bonding and conductivity. After this, sample is ready for electrical characterisations. Figure 3.19 shows the fabricated sample. Silver paste over the sample was on the made scratches to have contact with the LSMO layer.

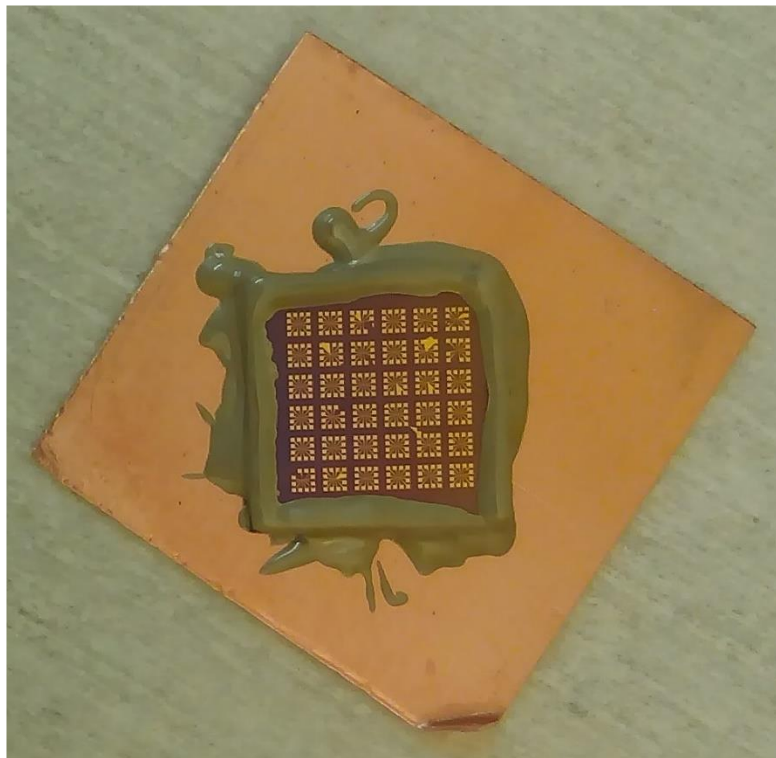

Figure 3.19 Image of one sample after all fabrication steps performed.

4 Electrical characterisation of GFETs

4.1 I-V characteristics of GFETs

4.1.1 Transfer characteristics of a GFET

4.1.2 Output characteristics of a GFET

4.1.3 Oxide dielectric constant

4.2 Results of I-V characterisation of GFETs

4.3 Complementary inverters

4.4 GFETs with other gate oxides

4 Electrical characterisation of GFETs

After the fabrication steps, the devices were characterised by a set of electrical tests on a micro-probe station. For all GFETs, transfer curves and output curves were measured in DC mode. Then using two GFETs a complementary inverter circuit was formed and for that DC and AC voltage gain was measured. For all the measurements, two source measurement units (SMU), Keithley 2611 - which are capable for both sourcing and measuring at the same time, were used. One of them is connected to back gate which is linked by a conductive mounting plate. The other one is connected to the electrodes through micro needle probes, which provide the voltage and at the same time measure the current flowing through channel. As graphene can adsorb some molecules from atmosphere – particularly water and also to avoid deposition of external particles on the chip during the measurements, a constant flux of nitrogen is blown over the surface of the chip. The SMUs were controlled by a custom-built LabView software, which also records the data during measurements. For inverter characterization one additional SMU was used to read the output voltage from the circuits.

This chapter includes a detailed description about electrical characterisation of GFETs. In section 4.1 theoretical explanations for the GFET's I-V performance are given. Section 4.2 includes results obtained from the measurements of the fabricated GFETs. In section 4.3 brief overview of complementary inverters and results obtained for the graphene inverters are included. In section 4.4, some other test samples made during this project work and a conclusion and some problems faced for making those samples with some possible solutions are discussed.

4.1 I-V characteristics of GFETs

Schematic structure of a back gated GFET, with a scheme of an electrical circuit used during measurement is shown in Figure 4.1. As described earlier in section 1.3, by applying an external electric field electrical conductivity of a material can be modulated. This effect is used in GFETs by placing an insulating material (gate oxide) between graphene and gate electrode, thus due to presence of this oxide an electrical field will be generated. This field will induce charges in the channel region. Depending on the strength of the created filed, which is a function of the applied gate voltage, charge carrier concentration in channel do vary. For graphene, as can be seen in the

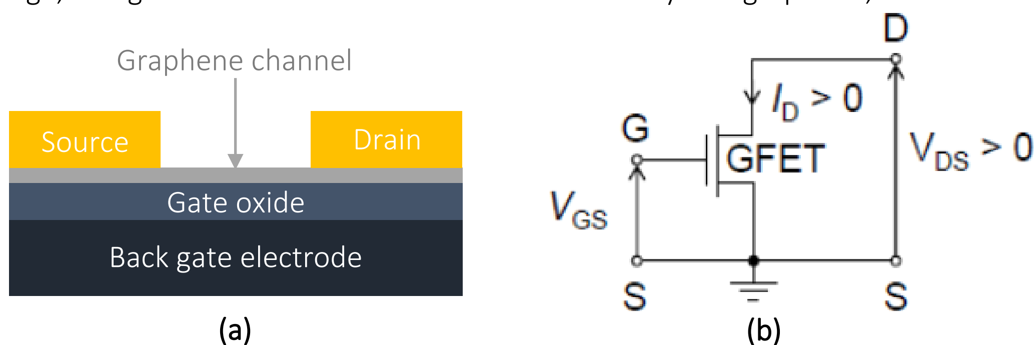

Figure 4.1 (a) Schematic representation of a back gated GFET. (b) Scheme of electrical circuit for GFET measurements, where S is source, D is drain and G is gate electrode.

Figure 1.8, the applied electric field will move the Fermi level up or down, based on the sign of the applied voltage. So based on the applied gate voltage the channel will behave as p- or n- type. The surplus of these charges created in the channel can be collected by applying a voltage difference between source and drain contacts.

For back gated GFETs, generally substrates are highly doped to make it good electric conductor, so that it can be used as gate electrode. Over which an insulating oxide is formed which acts as a gate oxide for FET. On this substrate graphene channel is made, and then on top of it two metal contacts are made which act as source and drain. This kind of simple structure of GFETs is shown in Figure 4.1 (a). So when the voltage is applied between the source and drain, a current will flow inside the graphene channel. This current can be tuned by applying or changing the gate voltage, which will affect the induced electrical field. In very simple case, while not considering any kind of resistance in the circuit except the channel resistance, the current flowing through the channel can be written as,

$$I_{\mathrm{D}} = \frac{V_{\mathrm{DS}}}{R_{Ch}} \tag{4.1}$$

where V_{DS} is the drain-source voltage and R_{Ch} is the channel resistance, which is a function of applied gate and drain voltage. Thus based on the applied bias to the gate and between source and drain the behaviour of GFETs do vary. For this work, transfer characteristics of GFETs were studied extensively, as from that the transconductance (g_m) value can be extracted (equation 2.2). Other than that, output characteristics of GFETs were also studied to understand the saturation behaviour of GFETs under different biasing conditions.

4.1.1 Transfer characteristics of a GFET

Starting with the very simple case, when $V_{DS} \approx 0$. Figure 4.2 shows the transfer curve for the p-doped graphene channel, for which the Fermi level is in the valance band. When positive bias is applied to the gate it will increase the concentration of electrons in the channel. Due to generation of these electrons, they will recombine with holes in the valance band and thus reduces the number of charge carriers in the channel. This affects the conductivity of the channel, reducing the current flowing through it. Current decreases till the V_{GS} reaches the V_{th} (threshold voltage, at which the Fermi energy reaches the Dirac point); at this point the valance band is completely filled and conduction band is completely empty, creating a system with minimum charge carriers. So when $V_{GS} = V_{th}$, the current flowing through the channel is at minimum. Further increase in V_{GS} will raise the Fermi level in graphene turning it into n- type channel. So further increase in the V_{GS} will increase number of electrons in the channel and thus increase the current passing through the channel. In this case when $V_{DS} \approx 0$, variation in the drain current is only because of the field effect created by applied gate voltage. Now when the potential is applied between source and drain, the

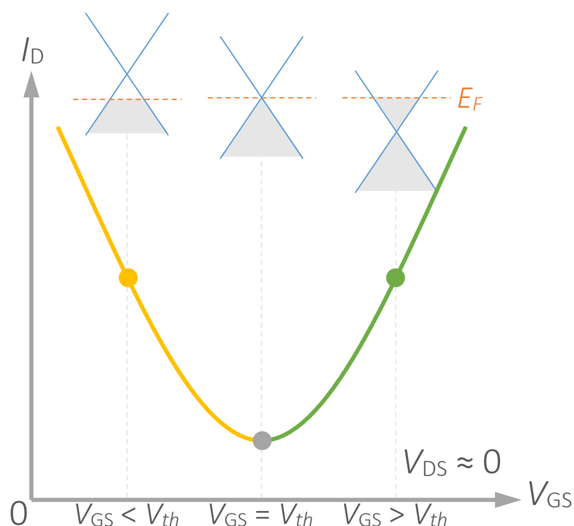

Figure 4.2 Transfer characteristic of a p-doped GFET for $V_{DS} \approx 0$. Minimum drain current is when $V_{GS} = V_{th}$ at Dirac point. On either side of the Dirac point, based on the applied gate voltage, Fermi level of graphene will change and results in different doping behavior.

potential distribution will change along the channel i.e., it will not be constant as before for $V_{DS} \approx 0$.

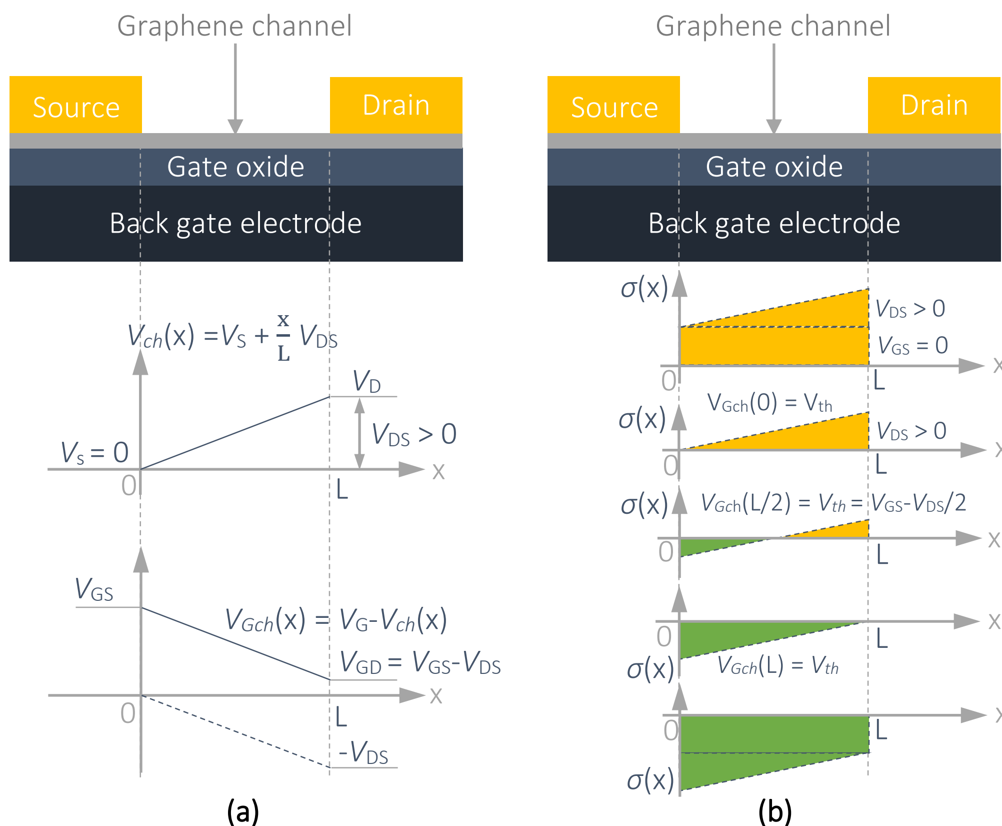

Figure 4.3 Voltage distribution and surface charge density in graphene channel. (a) Gradual approximation of potential variation along the channel, which depends on the applied V_{DS} and V_{GS}. (b) Increase in surface charge density due to non-zero V_{DS}, due to which higher V_{GS} is required to reach the Dirac point.

Variation in the channel potential from source to drain can be found from gradual approximation, according to which it can be written as,

$$V_{\mathrm{ch}}(\mathrm{x}) = V_{\mathrm{S}} + \frac{\mathrm{x}}{\mathrm{L}} V_{\mathrm{DS}} \tag{4.2}$$

where V_{ch} is the channel potential, x is the distance from the source and L is the gate length. Here V_{ch} increases from V_S to V_D, as moving from source towards drain. This is represented in Figure 4.3 (a).

For transfer characteristics V_{DS} is set to some fix voltage while the V_{GS} changes, and according to variation in V_{GS} there is change in I_D. Due to variation in V_{GS}, as mentioned earlier there will be a change in the charge concentration. But now as V_{DS} is also applied, it will affect the variation behaviour compared to the previous case. Figure 4.3 (b) shows the variation in the surface charge density σ, introduced due to applied voltages. Due to supply of V_{DS}, it will add further charges to the channel as can be seen in the Figure 4.3 (b), and the variation in σ along the channel is due to varying V_{ch}. Now due to this additional charges, even when V_{GS} becomes equal to V_{th} (for V_{DS}=0 condition), it will not be at the Dirac point. Instead, for this the Dirac point is shifted, which will be now at

$$V_{\mathrm{GS}} = V_{th} + \frac{V_{\mathrm{DS}}}{2} \tag{4.3}$$

After this point, further increase in V_{GS} will increase the electron concentration in the channel and thus the current will increase as in the previous case. Thus it can be concluded that the application of V_{DS} moves the Dirac point to higher or lower potential depending on the applied bias, but increase in the current can be observed in any situation due to increase in the charge concentration.

4.1.2 Output characteristics of a GFET

Output characteristic of a FET is to evaluate the effect of drain source voltage on the current flowing through the channel at constant applied gate voltage. This was discussed in section 2.4, and from that it is clear that for any biasing condition the GFETs do not have saturation regime. But they exhibit quasi-saturation, which is observable for very narrow window of V_{DS}, which is similar to standard transistor saturation. GFETs are required to operate in this region particularly when used in an inverter circuit, as to have large intrinsic gain ($G_{int} = g_m/g_{ds}$), as a consequence of small drain conductance (g_{ds}). As defined in the equation 2.3, g_{ds} is a slope of the output curve. This means that its value will be lower in saturation regime, and for GFETs in the quasi-saturation regime. To extract the best performance from the GFETs, it is necessary to choose particular biasing conditions both for gate and source-drain voltages. In next section the results obtained from the measurement of GFETs with ultrahigh-κ gate oxide samples are discussed.

4.1.3 Oxide dielectric constant

Properties of the oxide layer may vary based on the deposition methods and the quality of the material itself. It is always better to check the real properties of material used for samples. In this work also the actual dielectric constant of the gate oxide was measured, using LCR meter. The used arrangement of layers in the substrates makes it easy to measure the dielectric constant of the oxide. For measurement some of the pads, made for probe tip landing and which were not connected to any devices were used. Because of this configuration the oxide layer is sandwiched between two electrodes, and thus forms a parallel plate capacitor. Simply by measuring the capacitance of it, and the thickness of layer is already known to us, the dielectric constants can be found easily through simple calculation. The capacitance measured for this configuration was 290 pF, and the pad dimensions were 150 µm X 150 µm. From this the calculated dialectic constant is,

$$\kappa = \frac{C\ t}{\varepsilon_0\ A} = \frac{290\ 10^{-12}\ \text{x}\ 160\ 10^{-9}}{8.854\ 10^{-12}\ \text{x}\ (150\ 10^{-6})^2} = 233 \tag{4.4}$$

This value is lower than the κ value of 300 mentioned in the literature [66], but as mentioned, growth conditions and even the layout of devices have some influence on the property of material. In any case this value is much higher than oxides used as gate oxide in GFETs till now.

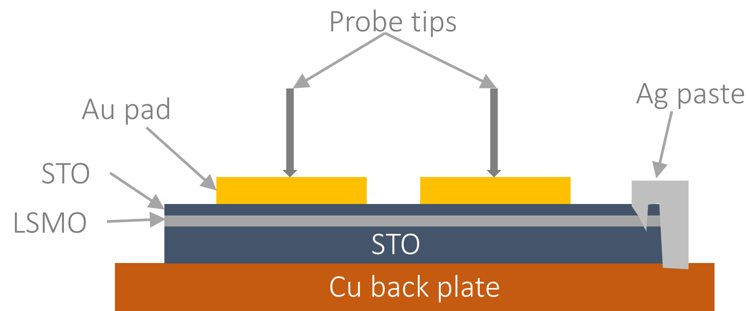

Figure 4.4 Schematic diagram of a sample for capacitance measurement. Here the capacitance was measured between one of the pads and the back gate.

4.2 Results of I-V characterisation of GFETs

In this work two types of devices were fabricated, one with gate channel length of 1 µm and other with 2 µm. For transfer curve measurements one of the SMUs was connected to the back gate, and it was set to sweep the gate voltage from -1 V to 2 V in 400 steps. The other SMU was connected to drain electrode, and was set to apply 0.1 V, 0.3 V, 0.7 V, 1 V, 1.5 V and 2 V. The same SMU was also used to record the drain current flowing through the channel. Throughout the measurement, gate leakage current was also measured by the SMU connected to gate, and for all devices the maximum leakage current observed was around 200 nA, which is acceptable as the drain current flowing through the channel was in the range of few mA. For 1 µm gate channel length devices, the maximum V_{DS} used was 1 V, as above that the Dirac point shifted too high that it was hard to perform measurements without damaging the devices.

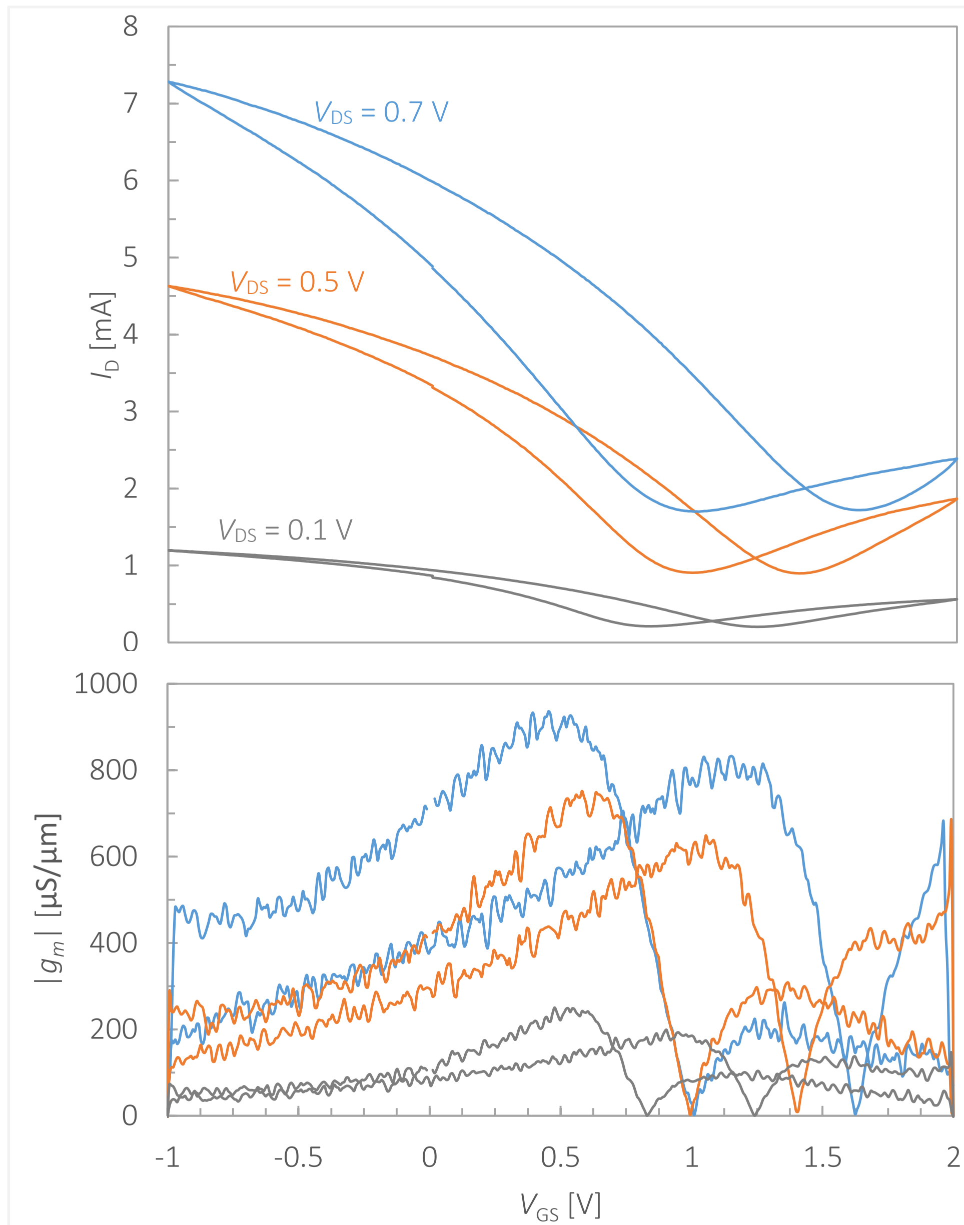

Figure 4.5 Transfer characteristics of a GFET. Graph on the top shows the transfer curves of a GFET. As the V_{DS} increases the Dirac voltage of a GFET shifts to higher values. As well as the curve moves up, meaning that I_D increases due larger number of carriers injected from the contacts at higher V_{DS}. The bottom graph shows the calculated transconductance (g_m) value from the above graphs. It shows the normalized values with respect to the channel width, to compare them with other GFETs with different channel width.

Figure 4.5 shows the transfer curves and calculated g_m values of one GFET. As predicted by theory, increasing the V_{DS} shifts the Dirac point to higher voltages, which can be observed in this figure (the upper graph in Figure 4.5). For all devices transfer curves were obtained and from them the g_m values were calculated (finding the slope of the curves). Then, those g_m values were normalised by gate channel width (as g_m has dependence on the channel width; equation 2.5), for ease to compare them with GFETs having different channel widths. Also from the same equation 2.5, it

can be predicted that the value of g_m also depends on the channel length and the applied V_{DS}. Therefore, a device with two times longer gate, should have the same performance when operated at twice the V_{DS} (considering all other parameters do not change with variation in gate length). Such dependence was observed during measurements, and is shown in Figure 4.6. Average maximum g_m obtained for all 1 µm gate length devices was about 400 µS/µm at V_{DS}=1 V, and the same was observed for 2 µm gate length devices at V_{DS}=2 V. Or other way around, it can be said that average g_m values for the 2 µm gate length devices at the same V_{DS} bias, was more or less half of that of the 1 µm gate length devices, as can be seen in Figure 4.6. The maximum g_m among all measured devices, was ~970 µS/µm for 1 µm gate length device at V_{DS}=0.7 V.

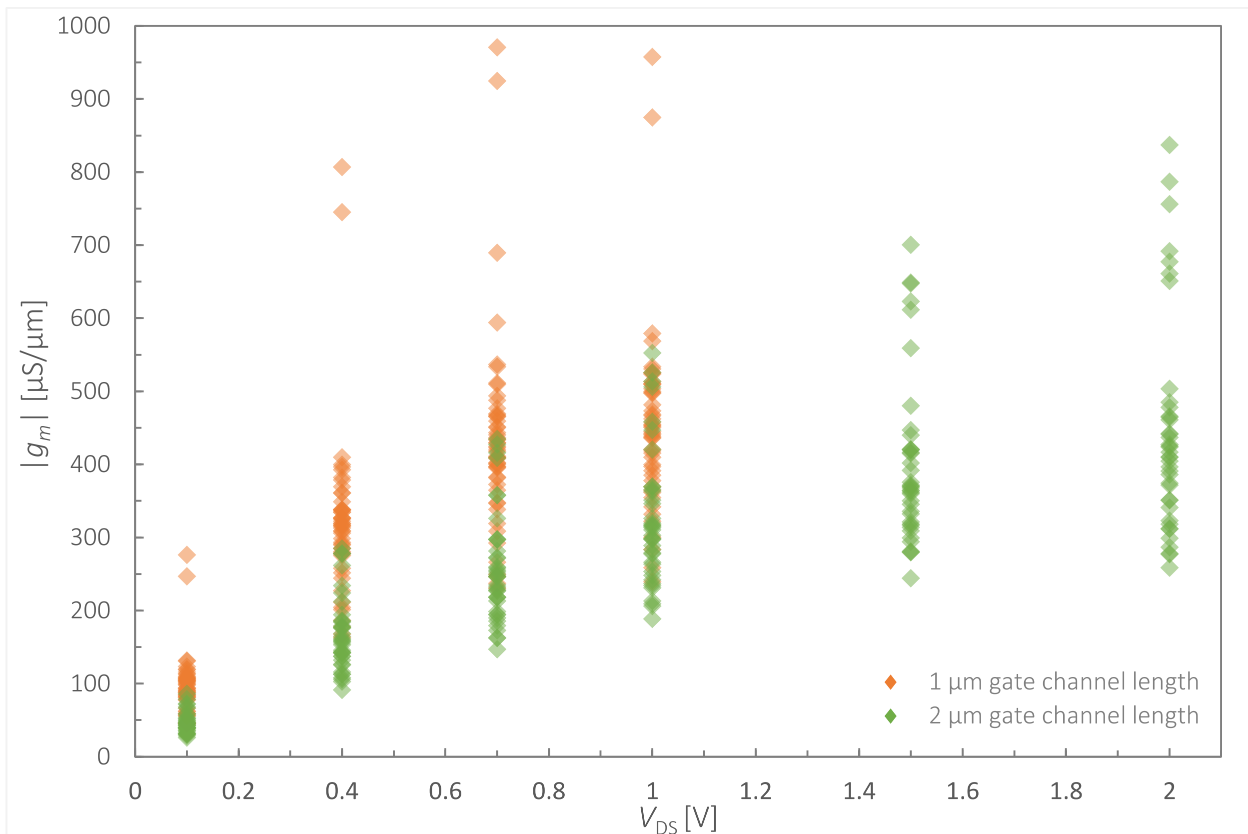

Figure 4.6 Measured transconductance values of different devices. All interesting results for g_m, from all the devices, are assembled in this graph. The orange marks represent data from the 1 µm gate length devices and the green marks are for 2 µm gate length devices. Roughly, for 2 µm gate length devices the required value of V_{DS} is twice to have the same performance as of 1 µm gate length devices.

For output curve measurements SMUs were connected in the same way as for the transfer curve, but only the biasing was changed. In this case the SMU connected to the back gate was set to apply gate voltage from 0 V to 2 V with an increment of 0.4 V while the SMU connected to drain was set to sweep V_{DS} from 0 V to 2 V in 400 steps. And in another measurement, applied V_{GS} was set from 0 V to -2 V with steps of 0.4 V and V_{DS} sweep from 0 V to -2 V. To prevent high potential across the gate oxides, which might damage the oxide layer, the output curves were measured

only in a single quadrant at a time, as at some part total potential across the oxide may get higher than the breakdown voltage of the gate oxide, as shown in Figure 4.7.

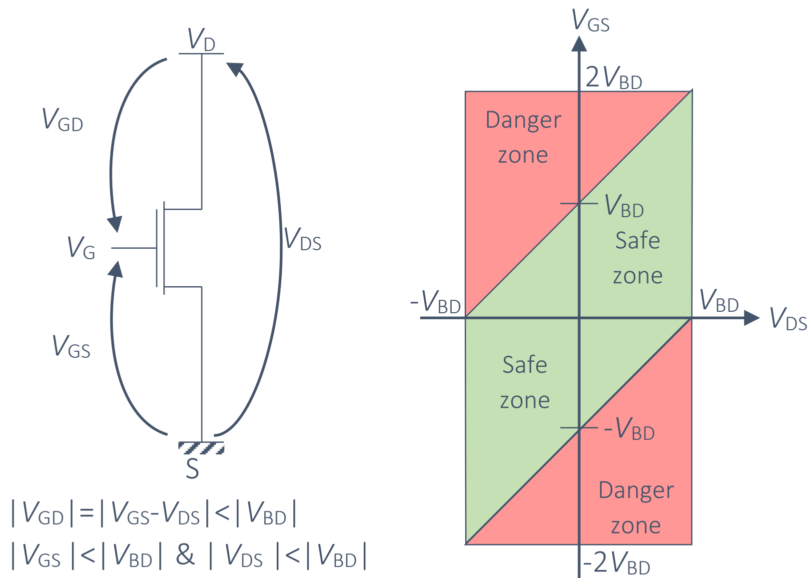

Figure 4.7 Schematic representation of a safe region to operate the GFETs without active oxide breakdown. V_{BD} is the breakdown voltage of the gate oxide layer. To prevent any damage to a device it is recommended to operate device in the safe zone shown.

For most of the devices the output curves were measured in both basing conditions; positive and negative. For positive biasing (both V_{GS} and V_{DS} positive), the output curves were almost the same as predicted by the theory. While for negative biasing it showed somewhat different nature. Figure 4.8 shows different output curves for measured GFETs. The one on the top is showing part of the measured curve, so that the peculiar characteristic of GFET can be observed. As mentioned in the theoretical part, based on the applied V_{GS} and V_{DS} the behaviour of the GFET will change. For V_{GS} = 0 V the channel is not influenced by the gate potential, so the current flowing through is only due to V_{DS}, this is shown by green line in Figure 4.8. When V_{GS} is applied it will start to increase the surface charge concentration, so now the effect of applied V_{DS} can be seen. As for the previous cases it is likely possible that the Fermi level of graphene remains either only in the valance band or only in the conduction band. If there is no transition of Fermi level from one band to other, there would not be quasi-saturation regime. So from the measurement data it can be seen that for V_{GS} > 0.8 V, quasi-saturation regime starts appearing. And then on increasing the V_{GS} shows increase in the current, and due to fact that the Dirac point shifts to the right so the saturation regime also shifts with it.

For negative bias of V_{GS} and V_{DS}, the measured output curves were not the same as in the previous case, this is shown in Figure 4.8 lower right graph. There is no particular quasi-saturation regime

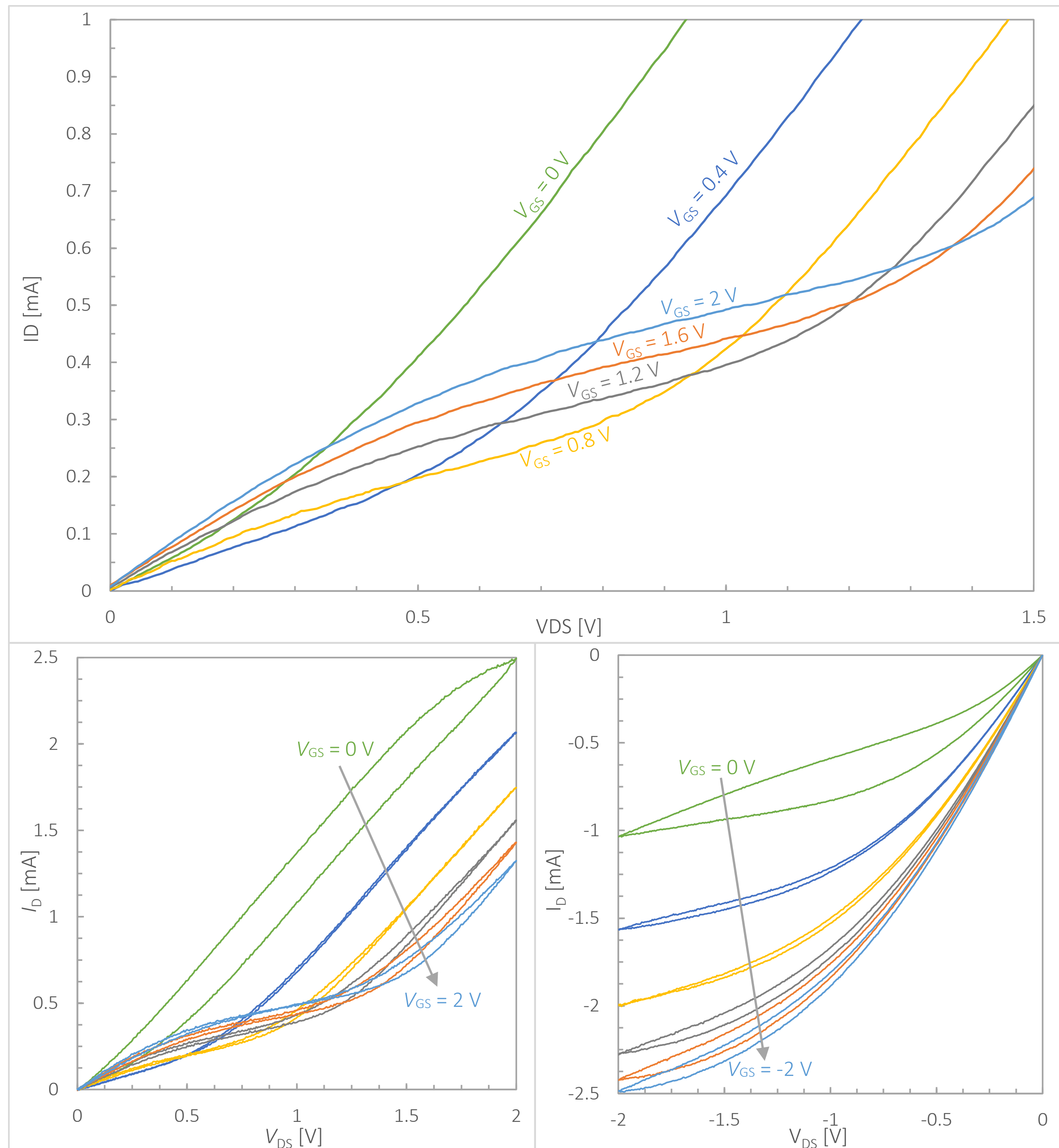

Figure 4.8 Output curves of one GFET. Graph on the top shows the typical behavior of GFETs; it contains values only for the down sweep. In this graph, effect of V_{GS} and V_{DS} on the quasi saturation regime can be seen. Graph at lower left shows the output characteristics of the device for positive V_{DS} and positive V_{GS}, here V_{GS} was increased with an increment of 0.4 V from 0 V to 2 V. Graph at lower right is for the output curve of a GFET operated for negative V_{DS} and negative V_{GS}. In this case V_{GS} was decreased with a decrement of 0.4 V from 0 V to -2 V.

observed. Which means that the Dirac point is already crossed or it is too far, that it would not show up during the measurements. In any cases, it is not advisable to start measurement with

positive V_{DS} and negative V_{GS} biasing, or to push further the V_{DS} bias to check whether the quasi-saturation regime appears or not. In both cases some part of the oxide and as such channel itself will be under high potential difference, which may cause damage to the device. This happened during measurements of some devices, in which we tried to observe the saturation regime. Overall to conclude, it is possible to have some quasi-saturation regime for fabricated GFETs, above some particular values of V_{GS} for positive bias of V_{DS}. To get good results from the devices it is advisable to operate in this region.

4.3 Complementary inverters

Inverters can be considered as a real electronics application of GFETs, done during this work, which is basically a building block for many electronic circuits. When two different GFETs are used; each at the opposite doping state, the entire circuit should work as a logic NOT gate, meaning the output signal should have 180° of phase change with respect to input signal. Here for complementary inverters, channel with opposite doping is a must, so for CMOS it is required to make two different channels with the opposite doping, while for graphene its ambipolar property can be used for such an application. In case of graphene it becomes quite simple to realized such a circuit over a single channel, just a proper biasing is required, such that one of the GFETs works in a p-doped state while other in n-doped state.

Figure 4.9 shows a schematic circuit diagram of a graphene inverter. Graphene complementary inverter can be made by connecting two GFETs with a common gate on a single channel of graphene. For this work, as all the devices were made with a common back gate, any two GFETs connected in series can be used to make an inverter. To have a good inverter performance it is required that the two GFETs used should have the Dirac point very close to each other, best condition will be having the same Dirac point for both the GFETs. This is important because GFETs cannot be turn off due to its ambipolarity, so if two GFETs have different transfer characteristics, either one of them will over control the entire system and will result in poor inverter performance.

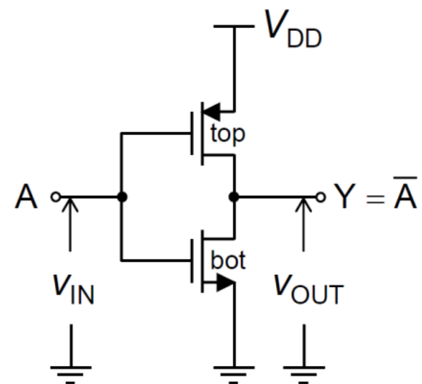

Figure 4.9 Schematic inverter circuit using GFETs.

When there is no V_{DD} applied to the circuit, the only applied bias is V_{IN} to the common gate for both the GFETs, which makes transfer curves for both of them similar, as shown in Figure 4.10 (left drack blue curve). When $V_{DD} > 0$ V is applied to the circuit it will change the Fermi levels in both GFETs, and it can be set in such a way that the top GFET become p-doped and bottom one n-doped. Once the V_{DD} is fixed to a certain value, V_{IN} can be applied to inverter. To explain the operation of a graphene inverter five different points are selected for different values of V_{IN}, as shown in Figure 4.10.

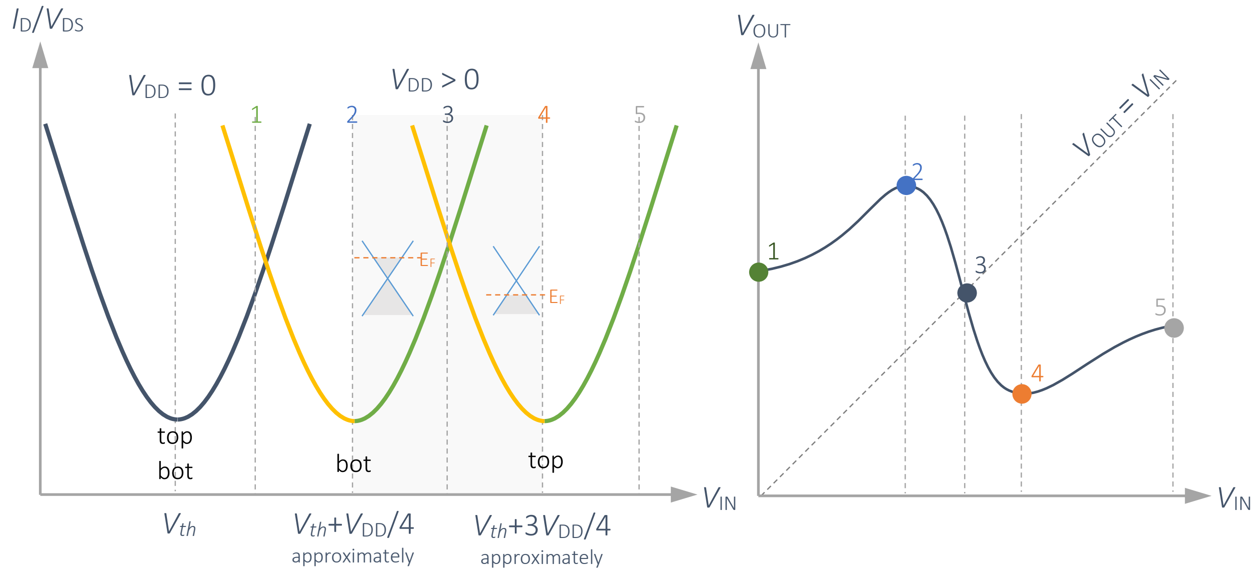

Figure 4.10 Transfer characteristics of two GFETs used in an inverter circuit, and voltage transfer characteristics of a graphene inverter.

At point 1, as the applied V_{IN} is small, both GFETs are in the p-type regime, with the top GFET being more conductive. At point 2, V_{IN} is high enough that the bottom GFET reaches to Dirac point, which makes it least conductive, thus making the bottom GFET like in the off-state. Due to this V_{OUT} becomes higher. Same is true for point 4, when due to V_{IN} the top GFET reaches to Dirac point. But in this case as the V_{DD} is connected via top GFET, most of the potential drops across it due to its higher resistance and thus we have lower V_{OUT}. At point 5, again both the GFETs are far from the Dirac points, with the bottom GFET being more conductive.

At point 3, both GFETs are at same condition but in the opposite doping region. Bottom GFET is in n-doped state and top GFET in p-doped state. Assuming that the electrons and holes have the same properties in graphene, this makes both GFTEs with the same conductivity. The region between points 2 and 4 is of real interest for inverter application, because in this the region inverter switches from one state to the other. For example, if considering point 3, even there is very small change in the V_{IN}, it will induce a big variation in V_{OUT}. This property of inverter is generally described by voltage gain, defined as the variation of the output voltage as a function of the input voltage.

$$A_V = \frac{\mathrm{d}V_{\mathrm{OUT}}}{\mathrm{d}V_{\mathrm{IN}}} \tag{4.5}$$

For electronic devices, it is required that A_V is higher than one so that there is no loss of signals from one stage to the next. It should be noted that as the GFETs cannot be fully switch-offed, the graphene inverters will consume power throughout its operation, and this also means that the output voltage is limited to a smaller range. After theoretical overview of graphene inverts, some results obtained during measurements of graphene inverters is discussed in the following paragraphs. For graphene inverters, both DC and AC characterisations were performed.

For DC voltage transfer characteristics of graphene inverters, three SMUs were used. One of the SMUs was connected to the back gate – as V_{IN}, and it was set to sweep V_{IN} from -1 V to 3 V in 400 steps. The other one was connected to the drain electrode of one of the GFET – as V_{DD}, and was set to apply 0.5 V, 1 V, 1.5 V, 2 V and 2.5 V, fix voltages one after other. And the last SMU was used to read the V_{OUT} from the common electrode of the two GFETs.

Figure 4.11 shows the measured DC voltage transfer curves, and the calculated DC voltage gain based on the equation 4.5. Transfer behaviour is same as predicted by the theory, the only difference here is the large hysteresis. This happens due to nature of the substrate itself. STO is a weak ferroelectric material so it has some surface dipoles which acts as charge traps. Nevertheless, the measured voltage transfer curves were very smooth, which indicates good quality of graphene inverters. The maximum DC voltage gain measured was 4.8 at V_{DD}=2.5 V and for 2 µm gate length. For 1 µm gate length devices maximum DC gain obtained was about 1.6, which is too low compared to other devices. Some of the possible reasons for poor performance are not having good GFETs with the same Dirac point and no quasi-saturation regime. Also, reducing the gate length may introduce some short channel effects, as actual channel length of the fabricated devices was in the range of 650 nm not 1 µm (this was measured using SEM). As the inverters were characterised after few days of fabrication, after characterising all GFETs, it is possible that as measurements were done in ambient conditions the chips were contaminated.

As shown for the GFETs characterisation (Figure 4.6), all the measured inverter's DC gain is compiled in a single graph, shown in Figure 4.12. It is pretty interesting to look to understand the poor behaviour of 1 µm gate length devices. As it can be seen for V_{DD}=1.5 V, the average A_V is higher compared to V_{DD}=2 V for these devices. This indicates that the fabricated GFETs were differing from one to other, or they did not operate in the quasi-saturation regime. Because these are the two possible reasons for deterioration of A_V with increasing V_{DD}, it is possible that V_{DD} makes the two GFETs to work in same region of doping or already saturate them that, there is no possibility to have the lowest value of drain-conductance.

DC voltage transfer curve is helpful to understand and to predict performance of graphene inverters, but the calculated A_V cannot be considered reliable value. As it is just mathematical derivative of the curve, and maximum value is for just a single point. This might overestimate the actual performance of inverters for AC signals. So to confirm the performance of graphene inverters, AC measurements were also performed on selected devices, which had a good DC gain.

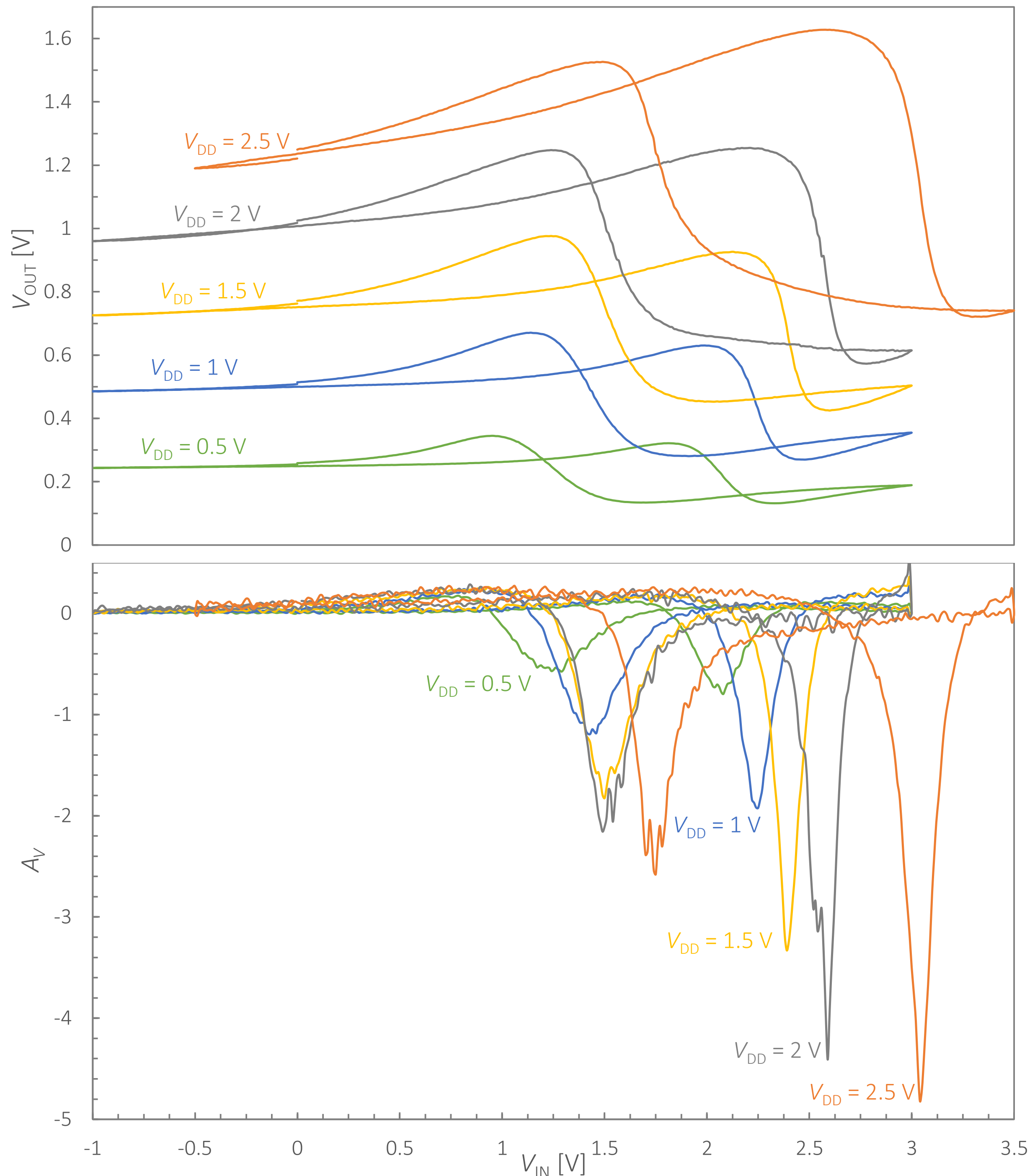

Figure 4.11 Voltage transfer characteristics of a graphene inverter. Graph on the top shows the measured voltage transfer curve. Increase in V_{DD} moves the curve to higher values both in V_{IN} and V_{OUT}. The bottom graph shows the calculated voltage gain (A_V) from the above graph. The gain increases with V_{DD}.

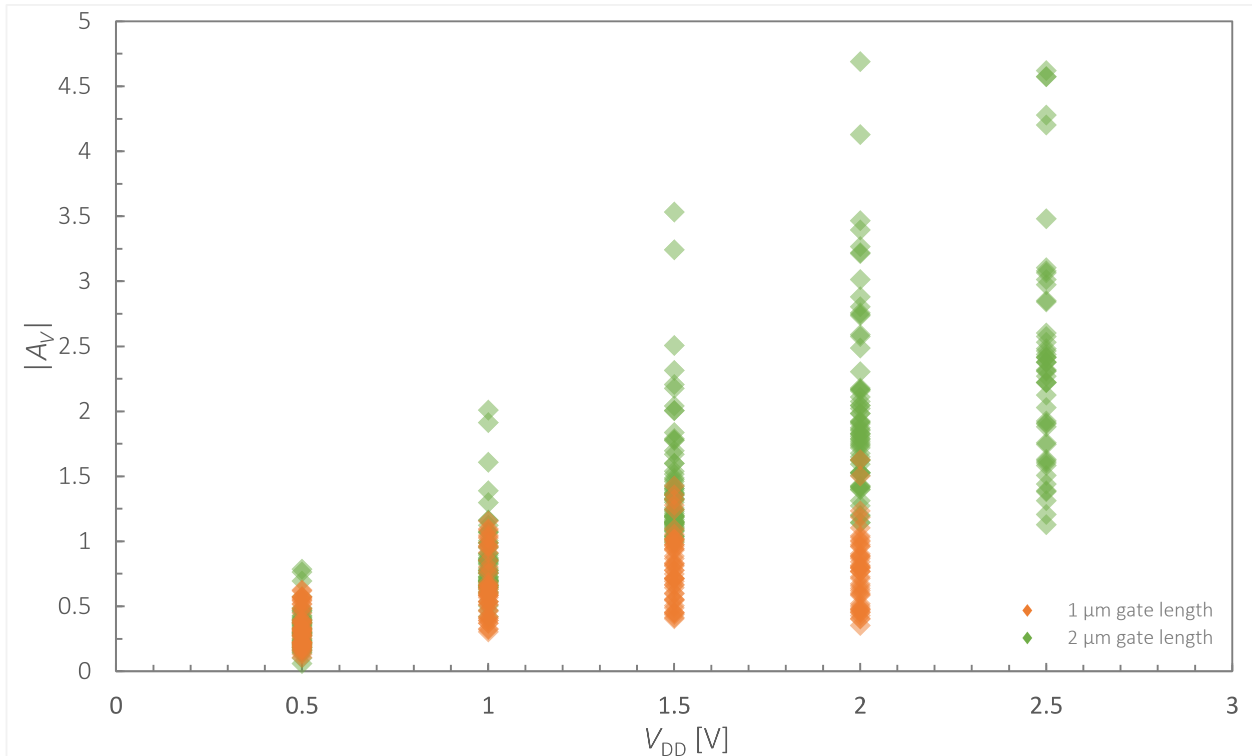

Figure 4.12 Measured voltage gains for different devices. All interesting results for A_V, from all the devices, are assembled in this graph. The orange marks represent data from the 1 µm gate length devices and the green marks are for 2 µm gate length devices. 1 µm gate length devices did not have gain as good as 2 µm gate length devices.

For AC characterisation a sinusoidal voltage was applied to the gate - V_{IN}, around point 3 shown in Figure 4.10 (this point refers as Q point – maximum gain point in DC characterization); the output inverted sinusoidal signal was then measured by a scope connected to the common drain of the

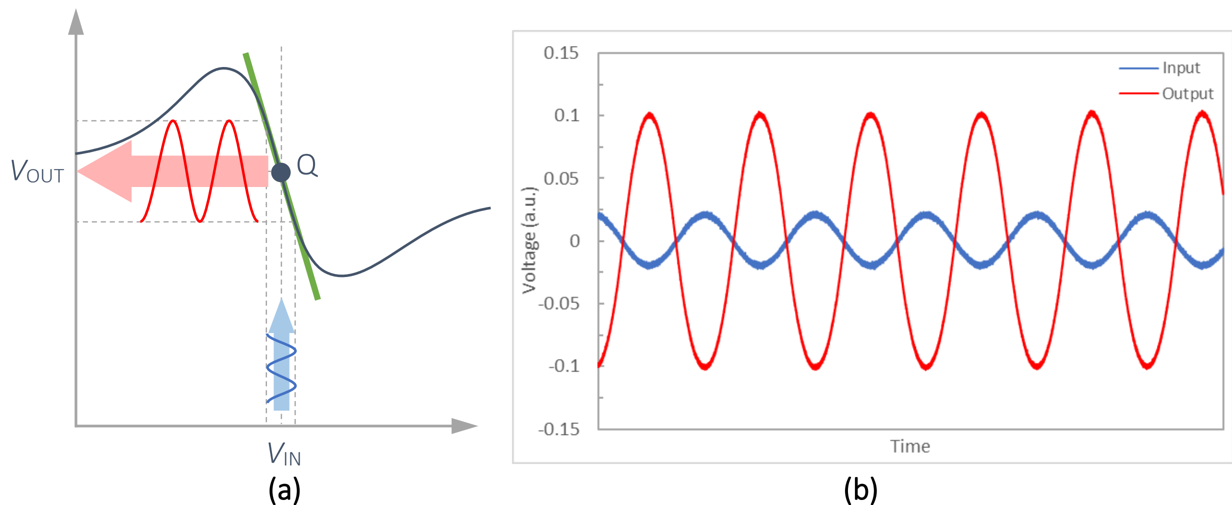

Figure 4.13 AC characteristics of graphene inverters. (a) Scheme for AC signal transfer characteristics of graphene inverters. (b) Measured AC characteristics. Signals are plotted without offset for representation, measured AC voltage gain is 4.5 for V_{DD}=2.5 V.

two GFETs. In this case, the voltage gain is straight forwardly calculated as the ratio of the amplitudes of the two signals. Figure 4.13 (a) shows schematically AC signal transformation in graphene inverters. By this way measured voltage gain is more precise than that of DC characterisation, and gives a maximum voltage gain of 4.5 for the same device at same V_{DD} as used for the DC characterisation, shown in Figure 4.13 (b). Besides this, for some devices further AC characterisations were done at higher V_{DD}, and maximum AC voltage gain of 5.1 was measured for 3.5 V of V_{DD} for 2 µm gate length devices. Still in AC characterisation also, 1 µm gate length devices had poor performance and maximum gain of 1.7 was measured for V_{DD}=2 V.

4.4 GFETs with other gate oxides

During this work, some experiments with other high-κ oxides were also done, to make GFETs using them. Ti and Hf oxides have high dielectric constant, about 80 and 25 respectively. We tried to make some devices using them as gate oxide. Already they have been used in our group for realising GFETs, but they all had different layouts. So results obtained from those devices cannot be compared with the results from the STO samples. To compare the performance improvement using different oxides, it is required that they all should be made with same device layout.

As the STO samples were back gated, we tried to make some samples with Ti and Hf oxides as gate insulator with back gated configuration. So for that we took standard SiO_2/Si substrates, and covered it with 20 nm of Ti followed by 100 nm of Au on it, thus making a gate electrode. Over that on one sample Ti (60 nm thick) and on other sample Hf (50 nm thick) were deposited in 1 mm x 1 mm square regions. We let them oxidise naturally. For Ti we allowed the samples to oxidise for 20 days, while for Hf it was 2 days. As in both cases native oxide forms within fraction of a second, to make sure that the samples do have sufficient time to grow somewhat thicker oxide layers we let it on its own for a longer time period. After that, as in case of the STO samples, first graphene was transferred over them and then graphene channel was defined using RIE, followed by electrode fabrication – 50 nm thick Au electrodes.

After device fabrication on native titanium oxide, we tried to perform electrical characterisation on that sample. Unfortunately, all devices were shorted with each other, not due to fabrication problems, but due to device layout itself. In those devices, entire electrode with very large pads do have gate electrode beneath – just a thin native oxide layer was there in-between top electrodes and gate electrode. This thin layer of native oxide cannot act as an insulator between two highly conductive electrodes and it is likely possible that there might be some cracks in the oxide layer through which electrodes were shorted. For this reason, we do not have any data on these devices. For Hf, we faced another problem with oxidation. Just before graphene transfer, we quickly inspected the samples under SEM to check whether there was any defect on surface, and we observed very smooth surface without any defect. But after graphene transfer the sample was completely destroyed, having cracks and small patches over entire surface of substrate, shown in Figure 4.14 (b). So for that also we could not perform any measurements.

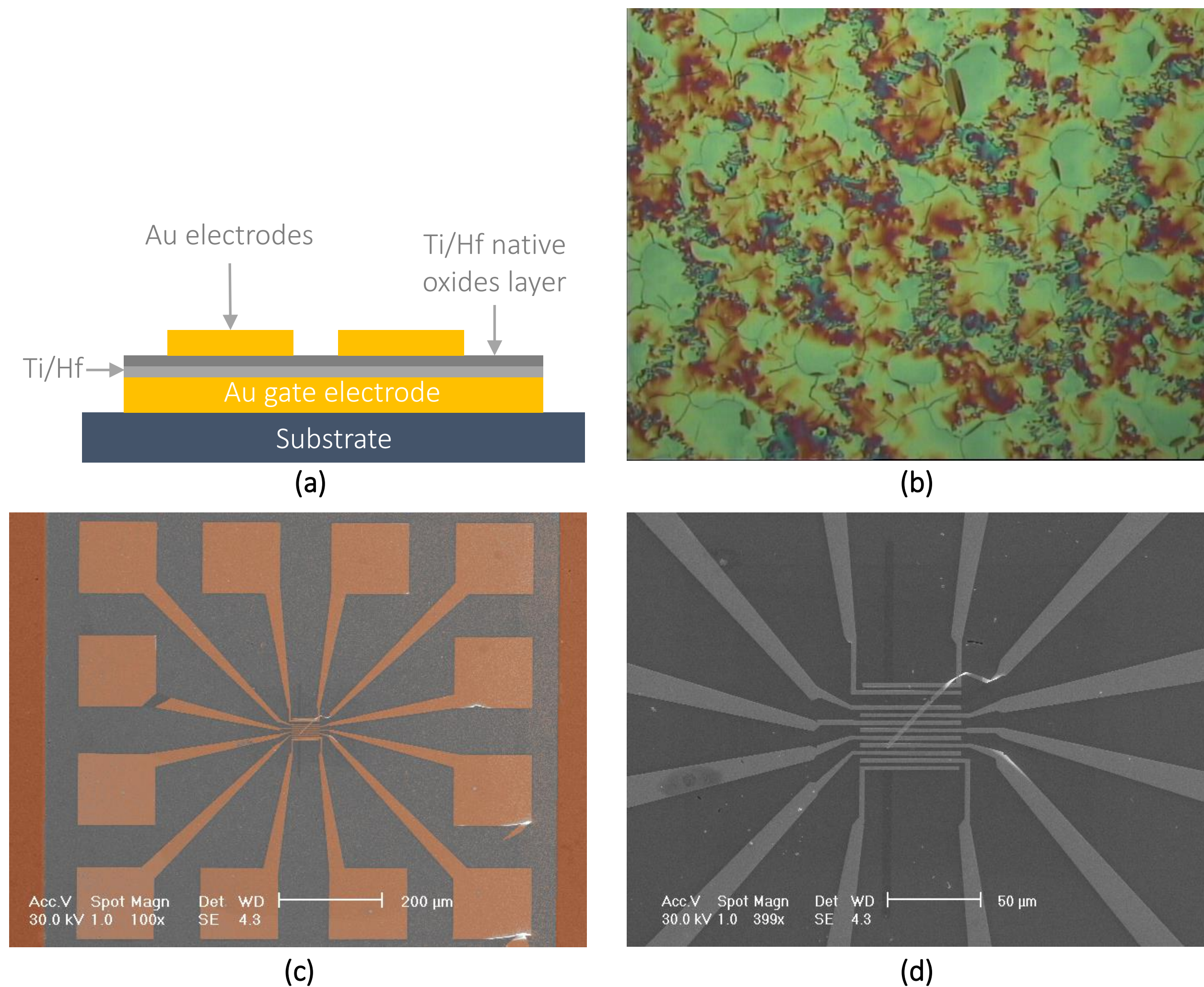

Figure 4.14 Ti and Hf native oxide samples. (a) Schematic representation of the device cross section. (b) Optical microscope image of graphene over HfO_x. The entire surface of sample was full of cracks and patches as can be seen in the image. (c) and (d) SEM images of TiO_x sample fabricated device. (c) SEM image of Ti sample device showing entire device structure. Dark orange region on both the sides of the image, is the back gate Au electrode. Gray part of image is the deposited Ti over Au back gate electrode. Light orange above Ti are the top electrodes (false color – edited image). (d) SEM image showing graphene channel over TiO_x gate oxide.

So different device layout for back gated configuration can be made. Gate electrode and Ti and Hf should only be deposited beneath the graphene channel, in that way the problem of large leakage or shorts between electrodes can be prevented. For HfO_x deposition different methods can be used, like atomic layer deposition (ALD), or some rigorous investigation is required to understand native oxide formation for Hf in ambient condition. As such both of the things are out of the scope of this work, so further investigation on them were not done.

5 Conclusions and prospective

5 Conclusions and prospective

Graphene field effect transistors with ultrahigh-κ gate oxide were fabricated during this thesis work. Epitaxially grown STO was used as gate oxide for all functional GFETs measured. Two problems were persistent for all fabricated GFETs. First, hysteresis was evident, in all DC characterisation tests, mainly due to property of STO and STO/LSMO stack. Second, at sub-micron gate length (around 0.7 µm), devices were having poor voltage gain and even the number of devices with good GFET characteristics were very few.

On the other side, transferred CVD grown graphene was not having uniformity form sample to sample, as electrical performance of the fabricated GFETs were different for each of the samples. As for all samples, except batch of graphene, everything was same. The reason for variation of the results should be graphene's non-reproducibility. Nevertheless, a typical trend for GFETs characteristics was observed in all analysed samples. Good experimental agreement with theoretical predictions for effect of gate oxide on the performance of GFETs was demonstrated. In this work the gate oxide thickness used was around 160 nm, and from the capacitance measurements calculated relative dielectric constant of the material was around 230. This makes gate capacitance per unit area around 1.44 μFcm^{-2} which is similar to the native alumina commonly used in our group. Indeed, the obtained results from these samples were quite comparable with devices made using alumina as top gate oxide in our group. Some remarkable results were obtained during experiments, e.g., g_m > 970 µS/µm and voltage gain above 5 were measured in AC characterisation.

This work was to evaluate the compatibility of STO as gate oxide in GFETs. It turns out that there is a chance to implement such an oxide in GFETs, but still some further work is required to investigate the acceptable minimum thickness of it. In addition to that, to use such GFETs in electronics, it is required that the STO should be used as top gate or should be made as an individual back gate for each of the devices rather having a common back gate for all. This second issue of individual gate is quite tricky with STO, as epitaxy is only possible at high temperature which is not compatible with graphene. With other methods to have a thick oxide with the same composition is bit harder, so lot more efforts are required to make it feasible. Contrary, other high-κ materials can also be studied, particularly TiO_2 and HfO_2, for their application in GFETs.

To conclude this report, it is clear that in order to have reliable, consistent high performance devices, both the graphene and the gate oxide needs to be optimized. Standardization of process for large-area, uniform and defect free graphene transfer on any substrate, to eliminating performance variations from sample to sample, is required to be done. And at the same time, some methods to implement high-κ materials in GFETs, to improve device performance, need to be investigated. Presently high-κ materials are centre of attention among the researchers working in microelectronics, so there is hope that this work might also help in realising GFETs with high-κ gate oxides.

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