Accelerating Physical Verification Productivity for Advanced Node Designs with IC Validator

Authors

Ron Duncan
Sr. Manager Applications
Engineering, Synopsys

Introduction

Applications such as deep-learning, autonomous driving vehicles, and mobility on 5G networks fuel the need for continuous advancements in IC integration. Growing design complexity, pressure on design cycle time, process advancements and increasing verification requirements are driving the need for faster, more efficient physical verification flows. The current state-of-the-art FinFET processes at 7nm and 5nm are complex feats of engineering. As has been the 'law' for some time, IC manufacturers can fit more and more transistors into the lithography reticle limit. For example, at 16nm, a typical 80 mm2 die has approximately 2 billion transistors, while at 5nm the same size die has over 12 billion transistors. Foundries utilize complicated front-end-of-line layer stacks and deploy multi-patterning lithography on many masks. This means more and more masks are required for advanced processes.
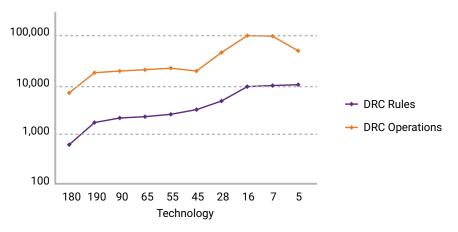

Figure 1: Increasing DRC complexity

The increase in density, plus the added number and complexity of process layers means that as designers migrate from older nodes to 7nm and 5nm physical verification has the potential to be more and more of a bottleneck for tapeout. Expect complaints such as:

- "Physical verification runs take too long for us to do overnight runs."
- "Physical verification takes too many resources."
- "DRC runs (particularly on early/dirty designs) are difficult to debug."

Productivity Improvements for Physical Verification

Here are three approaches to improve physical verification productivity:

- Run early and "clean as you go" during the IP and block-level design
- Run full chip verification efficiently to rapidly converge on a clean design that is ready for tapeout
- Run on more CPU resources to shorten signoff runs

Seamless verification during IP and block level design

"Cleaning as you go" is a concept that can streamline many of life's processes (think: washing dishes as you cook). Running DRC at each stage as you build your design is a simple, yet obvious way to avoid last-minute surprises that might impact your ability to hit the tapeout date. IC Validator's Fusion Technology™ integrates advanced flows, such as design rule checking (DRC), layout versus schematic checking (LVS), timing-aware fill, programmable electrical rule checking (PERC) with automatic place and route and custom design.

After analog and custom layout creation, designers typically find that complicated layouts and DRC rules make it difficult to converge on a DRC-clean design. IC Validator provides the ability to do a fast DRC check that covers all signoff checks in a small design, or a window of a larger design. Designers can:

- Run with all qualified foundry runsets and all technology nodes
- Run only the foundry rules that are of interest. For example: metal spacing violations
- Run on only the area within the view window

No longer does the design-then-check-then-fix loop take several minutes or several hours. Now, the layout tool sends the data within the view window to a streamlined IC Validator Live DRC engine. The signoff DRC checks are executed in a few seconds and any resulting violations can be viewed in an error viewer window within the layout editor tool and fixed immediately. Designers create the layout, run DRC checks, view violations and, fix them - all in one environment, and in just a few seconds.

IC Validator supports full interoperability for job execution, layout error shape probing, schematic cross probing within Synopsys Custom Compiler™ and Cadence® Virtuoso®.
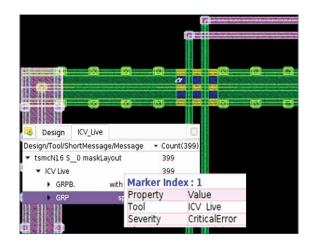

Figure 2: Live DRC checking for custom design flows

Early and efficient verification on the full design to rapidly converge on a clean design that is ready for tapeout

IC Validator Explorer DRC is designed to rapidly assess the status of a full chip design and give useful and actionable feedback to fix problems. Today's large chips consist of hundreds of blocks, such as place and route blocks, analog cells, memory, third party IP, and I/O cells. While each may have been verified independently as they were designed, when complied into the full chip, there are often high-level problems, such as missing blockages, block placement errors, pad ring misalignment, or block revision control issues that must be identified and fixed. A handful of high-level issues are often exhibited as an unworkable number of low-level DRC violations. It's common for a top-level designer run to encounter billions of DRC errors the first time the chip is compiled and run. This first "dirty" run may take multiple days on hundreds of cores to complete in a traditional DRC tool, as it brute-forces it's way through detailed over-analysis. Obviously, this could cause the tapeout team to waste weeks of compute time at the very end of the tapeout cycle.

IC Validator Explorer DRC automatically runs fundamental rules from the foundry runset and additional methodology to rapidly asses the health of the design. If the design is relatively clean, IC Validator continues progressively towards completing all required DRC signoff checks.

Explorer DRC brings a dramatic change in compute efficiency on dirty designs versus the traditional flow: five times faster runtime with five times few cores used.

In practice, this means that typical full-chip 7nm designs can be run using Explorer DRC in several hours with 16 or 32 cores, even when dirty. The Explorer DRC enables tapeout engineers to do an overnight run to detect fundamental design problems and begin fixing them immediately. IC Validator includes an error heatmap for rapid and intuitive visual topological assessment of your design. Within minutes, designers can often identify the macro-problems to fix (such as overlaps), instead of getting stuck in the weeds of billions of errors. The heatmap shows hot areas (where there are many violations) in red, progressing to cool areas (with relatively few violation) in blue. Often, as in the example below, designers immediately recognize where errors correspond to problems with specific blocks, such as overlaps or incorrect fill.
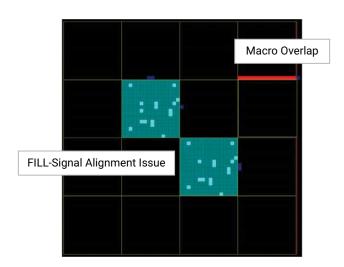

Figure 3: DRC heatmap highlighting error locations, density, and severity

Run verification on more resources to shorten signoff runs

As tapeout deadlines near, tapeout engineers often need to reserve a large number of cores to ensure that final verification jobs have enough compute power to complete as quickly as they can. The compute requirements to tape out the largest FinFET chips are straining the IT infrastructure of many companies.

The key to IC Validator's ability to efficiently distribute a job across thousands of cores is its unparalleled scheduler that initializes and controls the process. The scheduler queues commands that will run on each core to optimize file locality with the check sequence. During the run it intelligently estimates and balances the memory needs across cores while minimizing peak disk usage. It dynamically monitors the load on each core and adjusts the system to improve core and memory utilization.That's great when everything is working well, but what about when a job is run using a thousand cores on a heterogenous collection of hosts and disks connected by a network with real-world latency? IC Validator has fault-tolerant abilities to detect and recover from unexpected host reboots, network and socket failures, machine crashes or disk space limitations.

Beyond the automation of the scheduler, IC Validator enables the user to manually change job resources during the run. Elastic CPU Management allows the user to start a job with a few cores, then add cores on-the-fly to accelerate the job execution. On a typical compute farm, a job requesting a few hundred cores might have to wait indefinitely to start until they all become available. Instead, a tapeout engineer can start a 200 or 300 core DRC run with, say 16 available cores and automatically add the rest as they become available.

With such an efficient and scalable physical verification system you can get nearly any runtime you want. Want a faster run? Simply distribute across more cores. But what if your company's farm just doesn't have 1000 cores available for you to accelerate your job as you would like? Look to the cloud.

IC Validator is proven "cloud-ready" physical signoff solution and has been deployed on the cloud for production tapeouts. The chart below shows how the runtime of a production 7nm design can be scaled down to less than a day by deploying more cores on the Amazon Web Services cloud.
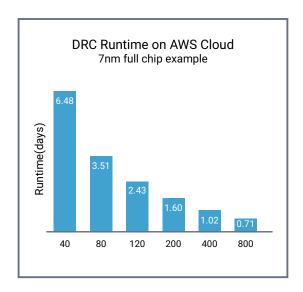
DRC Runtime on AWS Cloud
7nm full chip example

Cores	Runtime (days)
40	6.48
80	3.51
120	2.43
200	1.60
400	1.02
800	0.71

Figure 4: DRC runtime on AWS Cloud example

IC Validator for Tapeout Productivity

Design engineers will always want more performance from their tools to be able to meet tapeout schedules. IC Validator delivers productivity to accelerate physical verification time during IP and block-level design phases through to full-chip runs.

To learn more about physical verification using IC Validator go to: www.synopsys.com/icvalidator

SYNOPSYS®
Silicon to Software™