Synopsys coreTools

IP Based Design and Verification

Overview

The Synopsys family of coreTools is a comprehensive set of intellectual property (IP) packaging and integration tools for use in a knowledge-based design and verification flow. The tools enable designers to realize maximum productivity gains when using IP in their desing. By using an IP-based design and verification flow with IP packaged for assembly, the risk configuration, and subsystem integration errors is virtually eliminated, and designers have seen over a 60% reduction in SoC or platform design time and achieve the highest QoR in the implementation of the design.

The coreTool family includes:
coreBuilder™ – a robust packaging tool that allows designers to capture the knowledge and design intent of the IP and provide graphical or command based configuration menus for the IP. It supports the packaging of all the different model views of the IP needed engineering teams. This reduces IP support costs, improves quality and IP packaged with coreBuilder is fully compliant with the IP-XACT specification.

coreAssembler™– an open IP assembly tool that automatically generates the interconnect and configured RTL, as well as documenting the block and system configuration details and design testbench. When combined with coreBuilder, entire subsystems can be packaged as coreKits enabling the easy creation configurable market targeted platforms. In addition to assembly and configuration designers are able to generate a starting testbench configured for the design so they can begin to validate there design. coreAssembler also will generate the IP-XACT XML for the design.

coreConsultant™– the utility package for configuring, implementing and validating individual IP blocks packaged with coreBuilder. coreConsultant will also generate the IP-XACT XML for the IP block.

Features

- Intuitive graphical or script-based environment
- Built-in interfaces to Synopsys tools, including:
  - Design Compiler®
  - Physical Compiler®
  - Power Compiler®
  - TetraMAX®
  - PrimeTime®
  - Formality®
  - VCS®
- Automatic testbench generation with DesignWare VIP for AMBA and AXI which supports VMM and/or traditional testbenches
- Supports mixed-language HDL designs
- Flexible TCL interface for tool customization
- Knowledge-based assembly of IP blocks
- Full IP-XACT support including TGI with automatic XML generation

Benefits

- Full support for packaging, integrating, and assembling IP
- Allows packaging of IP at multiple levels of abstraction, including:
  - RTL
  - Instruction set models
  - Transaction level models
  - Bus functional models
  - Verification test suites
  - Hard macros
- Automatic assembly of pre-designed IP blocks reduces design time
- Reduces design integration and support costs

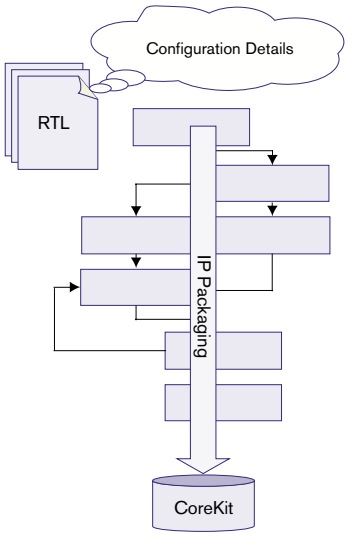

Figure 1. IP Capture with coreBuilder.

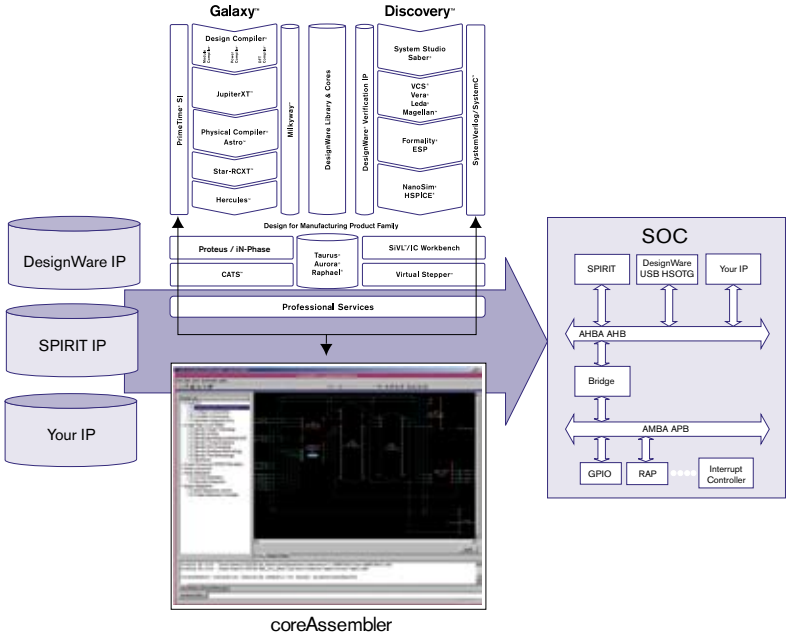

Figure 2. Using coreAssembler with coreBuilder for packaging IP-based design platforms and IP integration.

coreBuilder

The coreBuilder tool is language-independent, which enables the packaging of IP blocks with a step-by-step process. This ensures that all of the design requirements have been followed, allowing the easy enforcement of an IP quality flow. Additionally, the design intent is captured, bringing the detailed knowledge of the IP to the designers' desktop. IP packaged with coreBuilder can be easily configured and integrated in the SoC. Figure 1 shows the IP capture flow with coreBuilder. coreBuilder not only provides the environment to capture all of the files related to the IP block, but also allows the IP designer to capture the IP intent as well. IP packaged with coreBuilder is fully compliant with the IP-XACT specification.

coreAssembler

The coreAssembler tool has an intuitive graphic or command based interface that speeds the designer through the assembly, configuration, and implementation of an IP-based design. The coreAssembler tool also provides the infrastructure for building a complete SoC design and verification environment.

coreAssembler uses a knowledge-based design and verification flow that automates the tedious task of connecting, configuring and verifying all of the IP components in the SoC. This eliminates the risk of assembly and configuration errors by automatically generating the configured RTL and with the interface to the Galaxy™ platform implementation scripts are generated based on the designers intent helping to ensure highest QoR with significant reductions in design time. IP-XACT XML is also generated from coreAssembler.

In addition to integrating packaged IP into the design, coreAssembler allows the easy integration of new, unpackaged IP or IP compliant with the IP-XACT specification. With the open TCL interface, designers can easily include design flow customizations into the coreAssembler environment.

coreBuilder + coreAssembler

coreBuilder combines with coreAssembler to provide designers with an open and customizable environment for the creation of IP-based subsystems as well as product design platforms. IP that has been packaged with coreBuilder can easily be included with controlled configuration options targeted at specific market applications into design platforms assembled with coreAssembler.

In addition to the ability to include packaged IP, new design specific IP can be easily integrated into the design platform.

Figure 2 shows how coreAssembler integrates IP into a design platform.

coreConsultant

coreConsultant guides an IP integrator through the configuration, verification, and implementation of a single core packaged with coreBuilder into a coreKit and generates the IP-XACT XML. coreConsultant includes the graphic and command line options for use along with built-in interfaces to the Discovery and Galaxy platforms speeding the implementation and verification of an IP core.

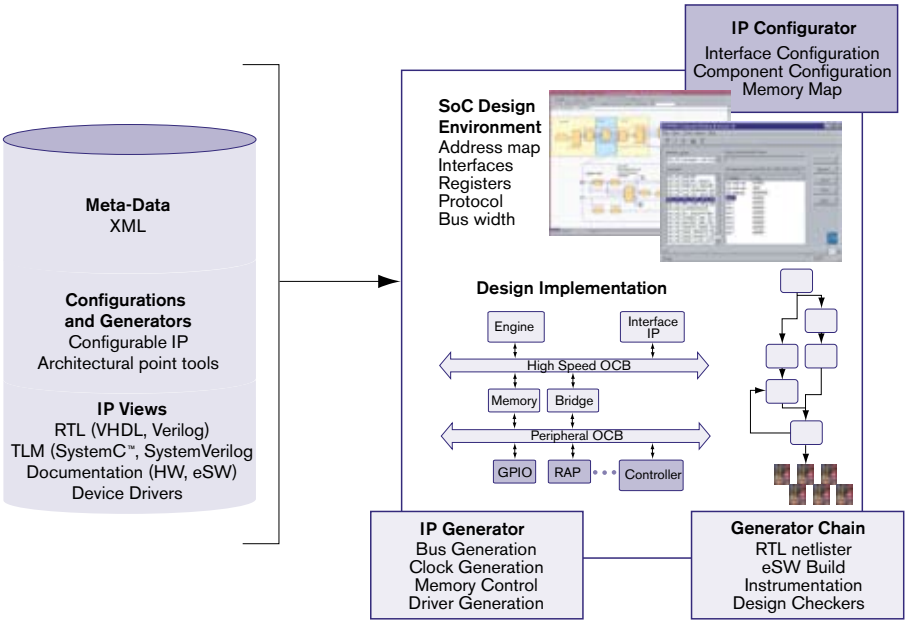

Figure 3. SPIRIT Schema and Generator Interface.

IP-XACT Support

The Synopsys suite of IP reuse tools have been and continue to be used in the development and testing of the IP-XACT specification. IP packaged with coreBuilder can be used in any IP-XACT compliant SoC design tool. Designs, platforms or subsystems implemented in coreAssembler can include components that are IP-XACT compliant into the subsystem

Supported Platforms and Simulators

Solaris, HP, and Linux

Verilog Simulators

Synopsys VCS

Cadence NC-Verilog®

MTI ModelSim-Verilog

VHDL Simulators

Synopsys VCS MX

Cadence NC-VHDL

MTI ModelSim-VHDL

For a complete directory of Synopsys IP visit: www.synopsys.com/ipdirectory

For more information on DesignWare IP, visit www.synopsys.com/designware-ip

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