

Voodoo: Memory Tagging, Authenticated Encryption, and Error Correction through MAGIC

Lukas Lamster Martin Unterguggenberger David Schrammel Stefan Mangard August 16, 2024

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Achieving System Security





Activate Security!

Achieving System Security



That's not how it works! Activate Security!





Security Building Blocks



🗂 Data Encryption















Our Approach



We create a combined primitive!



• Combine AE and error correction



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- $T = E_{\mathcal{K}} \left(D + \sum_{i=1}^{n} C_i \cdot H^i \right)$



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- Correct up to *T_{th}* bits in one *N*-bit block



From CPU: M_1 M_2 M_n Г E_D E_D E_D $\cdot H^2$ $\cdot H^n$ Eĸ ·Н DRAM: C_1 C_{2} C.

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The MAGIC is in the H

Impose conditions on Hamming weights of $HW(e \cdot H^i)$ for all errors *e*. The faulted block is found using the Hamming weight of $S \cdot H^{-i}$.



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How can we include memory tagging into MAGIC?

? Can we just replace the authenticated data D with a memory tag M_T ?

$$T = E_{\mathcal{K}}\left(\mathbf{D} + \sum_{i=1}^{n} C_{i} \cdot H^{i}\right) \to T = E_{\mathcal{K}}\left(\mathbf{M}_{\mathcal{T}} + \sum_{i=1}^{n} C_{i} \cdot H^{i}\right)$$



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$$T = E_{K} \left(D + \sum_{i=1}^{n} C_{i} \cdot H^{i} \right) \rightarrow T = E_{K} \left(M_{T} + \sum_{i=1}^{n} C_{i} \cdot H^{i} \right)$$

Can we ...
7 Detect Mismatches? Correct Errors? Read Tags?

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Detecting Tag Mismatches

$$S = M_T + \sum_{i=1}^n C_i \cdot H^i +$$
$$M'_T + \sum_{i=1}^n C'_i \cdot H^i =$$
$$M_T + M'_T = e_t$$

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Detecting Tag Mismatches

• Assume $C_i = C'_i$ for all blocks





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- Syndrome only depends on $e_t = M_T + M'_T$
- What values can *e*_t assume?
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We cannot distinguish tag mismatches from errors

Tag errors can look like correctable errors \rightarrow Miscorrection and Data Corruption.



• Access with $M'_T = 0$

$$S = M_T + \sum_{i=1}^n C_i \cdot H^i +$$
$$0 + \sum_{i=1}^n C'_i \cdot H^i = M_T$$



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- $e_t = M_T + e_j \cdot H^j$

$$5 = M_T + \sum_{i=1}^n C_i \cdot H^i + 0 + \sum_{i=1}^n \tilde{C}'_i \cdot H^i = M_T$$

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- $e_t = M_T + e_j \cdot H^j$
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- $e_t = M_T + e_j \cdot H^j$
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We cannot reliably read tags in the presence of errors

Data errors will not be detected and the read operation will yield a faulty tag.

$$5 = M_T + \sum_{i=1}^n C_i \cdot H^i + 0 + \sum_{i=1}^n C_i' \cdot H^i = M_T$$



Takeaway: A naïve encoding is not suitable!

- **F** Tag errors are not clearly identifiable
- \checkmark Miscorrection and data corruption is possible
- Reading tags only works without data errors



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We can solve these issues!

We present three encodings for M_T that circumvent these problems.

- I Check Pattern Encoding
- 🔒 Encrypted Tag Encoding
- ᢥ Bounded Hamming Weight Encoding



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Design - Check Pattern Encoding

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- Tags are small, we do not need $[0, 1]^N$ tag space.
- Fix upper bits of tag to certain <u>pattern</u> P.
- Check if upper N X bits are 0 in S
- P always cancels out
- Upper bits '0' \rightarrow (likely) tag mismatch





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Check Pattern Encoding never miscorrects due to a tag mismatch. Guaranteed to identify tag errors. Some correctable errors may be treated as uncorrectable. No data corruption from tag errors!

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 \P Select tags to have Hamming weight below T_{th}

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? No aliasing and no miscorrection possible



- \mathbf{P} Select tags to have Hamming weight below T_{th}
- **?** No aliasing and no miscorrection possible
- Limit M_T s.t. $HW(e_t) < T_{th}$
- No S will have $HW(S) \leq T_{th}$
- Tag errors are uniquely identifiable

 $egin{aligned} |\mathcal{M}_{\mathcal{T}}| &= \sum_{t=0}^{\lfloor T_{th}/2
floor} inom{N}{t} \ HW(M_{\mathcal{T}}) &\leq \lfloor T_{th}/2
floor \ HW(M_{\mathcal{T}}+e_{j}H^{j}) &> \lfloor T_{th}/2
floor +1 \end{aligned}$



- \P Select tags to have Hamming weight below T_{th}
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floor + 1$

Bounded Hamming Weight Encoding allows for fully deterministic tagging. No aliasing possible. Smaller tag space than other encodings.

Table 1: ● deterministic tagging O impossible configuration

Architecture	Tag Bits	f-Bounded		f-Pattern		f-Encrypt	
	per 64 B	N=64	N=128	N=64	N =128	N=64	N =128
CHERI ISA (256)	2-bit	•	•	0	0	2^{-57}	2^{-120}
CHERI ISA (128)	4-bit	•	•	0	0	2^{-57}	2^{-120}
SPARC ADI	4-bit	•	•	0	0	2^{-57}	2^{-120}
DIFT Q ,M-Machine () ,	8-bit	•	•	2 ⁻⁶³	0	2^{-52}	2^{-119}
HDFI ,Shakti-T							
Model 1 A 🎔 / B 🔍	15-bit	•	•	2^{-49}	2^{-128}	2^{-48}	2^{-109}
MTE) , Mondrian Q	16-bit	0	•	2^{-48}	2^{-123}	2^{-47}	2^{-109}
SPEAR-VQ	24-bit	0	•	2^{-40}	2^{-106}	2^{-37}	2^{-103}
lowRISC Q , 🍑	32-bit	0	•	2^{-32}	2 ⁻⁹⁶	2^{-31}	2^{-95}
Model 2 A V / BQ	36-bit	0	•	2^{-28}	2^{-92}	2^{-26}	2^{-91}

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Evaluation - Single-Block Error Correction

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• We cannot test Voodoo on real hardware.

Model DRAM faults in Monte Carlo simulation [2].

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Voodoo offers strong single-block error correction

We can correct up to 99% of single-block faults. We find an optimum at $T_{th} = 19$.

Evaluation - Multi-Block Error Detection

How well do we perform with multi-block faults?Model multi-block faults in Monte Carlo simulation.

Evaluation - Multi-Block Error Detection

How well do we perform with multi-block faults?

Model multi-block faults in Monte Carlo simulation.



Voodoo has a low miscorrection rate

Multi-block faults are <u>most likely correctly identified</u> as uncorrectable. Miscorrection happens if exactly one wrong error location indicator is found.







T Combine auth. encryption, ECC, and memory tagging

> Up to 36 tag bits per cache line

Strong single-block error correction

Q Strong multi-block error detection



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